National Semiconductor

400044

LS/S/TTL Logic

Databook

Contains former Fairchild products
and consolidation information

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Charlie Sporck

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

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Charlie Sporck

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

LS/S/TTL Logic Databook

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Section 1

Introduction to Bipolar Logic

Section 1—Introduction to Bipolar Logic

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Guide to Bipolar Logic Device Families

Since the introduction of the first saturating logic bipolar integrated circuit family (DM54/DM74), there have been many developments in the process and manufacturing technologies as well as circuit design techniques which have produced new generations (families) of bipolar logic devices. Each generation had advantages and disadvantages over the previous generations. Today National provides seven bipolar logic families.

TTL	(DM54/DM74)
Low Power TTL	(54L)
Low Power Schottky	(DM54LS/DM74LS)
Advanced Low Power Schottky	(DM54ALS/DM74ALS)
Schottky	(DM54S/DM74S)
Advanced Schottky	(DM54AS/DM74AS)
FAST	(54F/74F)

TTL LOGIC (DM54/DM74) and (54xx)

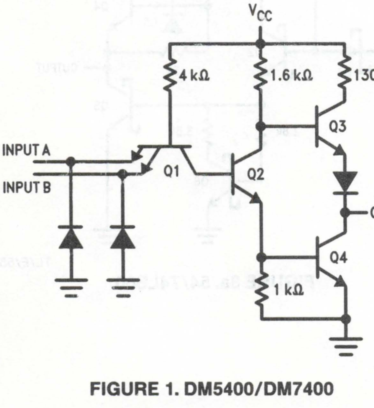
TTL logic was the first saturating logic integrated circuit family introduced, thus setting the standard for all the future families. It offers a combination of speed, power consumption, output source and sink capabilities suitable for most applications. This family offers the greatest variety of logic functions. The basic gate (see *Figure 1*) features a multiple-emitter input configuration for fast switching speeds, active pull-up output to provide a low driving source impedance which also improves noise margin and device speed. Typical device power dissipation is 10 mW per gate and the typical propagation delay is 10 ns when driving a 15 pF/400Ω load.

LOW POWER TTL (DM54L)

The low power family has essentially the same circuit configuration as the TTL devices. The resistor values, however, are increased by nearly tenfold, which results in tremendous reduction of power dissipation to less than 1/10 of the TTL family. Because of this reduction of power, the device speed is sacrificed. The propagation delays are increased threefold. These devices have a typical power dissipation of 1 mW per gate and typical propagation delay of 33 ns, making this family ideal for applications where power consumption and heat dissipation are the critical parameters.

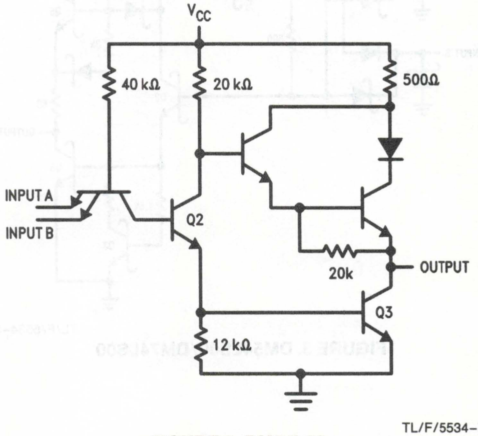
LOW POWER SCHOTTKY (DM54LS/DM74LS and 54LS)

The low power Schottky family features a combined fivefold reduction in current and power when compared to the TTL family. Gold doping commonly used in the TTL devices reduces switching times at the expense of current gain. The LS process overcomes this limitation by using a surface barrier diode (Schottky diode) in the baker clamp configuration between the base and collector junction of the transistor. In this way, the transistor is never fully saturated and recovers quickly when base drive is interrupted. Using shallower diffusion and soft-saturating Schottky diode clamped transistors, higher current gains and faster turn-on times are obtained. The National LS circuits and a majority of the former Fairchild LS circuits do not use the multi-emitter inputs. They use diode-transistor inputs which are faster and give increased input breakdown voltage; the input threshold is ~0.1V lower than TTL. A few of the former Fairchild LS circuits use the traditional emitter inputs and thus have input breakdown ratings of 5.5V. These circuits are the open-collector gate types 'LS03, 'LS05, 'LS22 and 'LS136; flip-flop types 'LS74, 'LS109, 'LS112 and 'LS113; and the clock inputs of the 'LS490. Another commonly used input is the vertical substrate PNP transistor. In addition to fast switching, it exhibits very high impedance at both the high and low input states, and the transistor's current gain (β) significantly reduces input loading and provides better output performance. The output structure is also modified with a Darlington transistor pair to increase speed and improve drive capability. An active pull-down transistor (Q3) is incorporated to



TL/F/5534-1

FIGURE 1. DM5400/DM7400



TL/F/5534-7

FIGURE 2. DM54L00

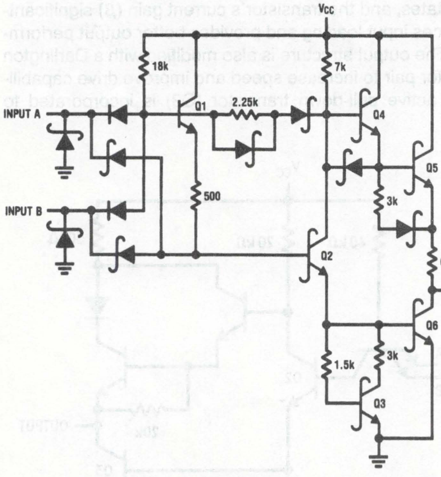
yield a symmetrical transfer characteristic (squaring network). This family achieves circuit performance exceeding the standard TTL family at fractions of its power consumption. The typical device power dissipation is 2 mW per gate and typical propagation delay is 10 ns while driving a 15 pF/ 2 kΩ load.

SCHOTTKY (DM54S/DM74S)

This family features the high switching speed of unsaturated bipolar emitter-coupled logic, but consumes more power than standard TTL devices. To achieve this high speed, the Schottky barrier diode is incorporated as a clamp to divert the excess base current and to prevent the transistor from reaching deep saturation. The Schottky gate input and internal circuitry resemble the standard TTL gate except the resistor values are about one-half the TTL value. The output section has a Darlington transistor pair for pull-up and an active pull-down squaring network. This family has power dissipation of 20 mW per gate and propagation delays three times as fast as TTL devices with the average time of 3 ns while driving 15 pF/280Ω load.

ADVANCED LOW POWER SCHOTTKY (DM54ALS/DM74ALS)

The advanced low power Schottky family is one of the most advanced TTL families. It delivers twice the data handling efficiency and still provides up to 50% reduction in power consumption compared to the LS family. This is possible because of a new fabrication process where components are isolated by a selectively grown thick-oxide rather than the P-N junction used in conventional processes. This refined process, coupled with improved circuit design techniques, yields smaller component geometries, shallower diffusions, and lower junction capacitances. This enables the devices to have increased f_T in excess of 5 GHz and improved switching speeds by a factor of two, while offering much lower operating currents.



TL/F/5534-3

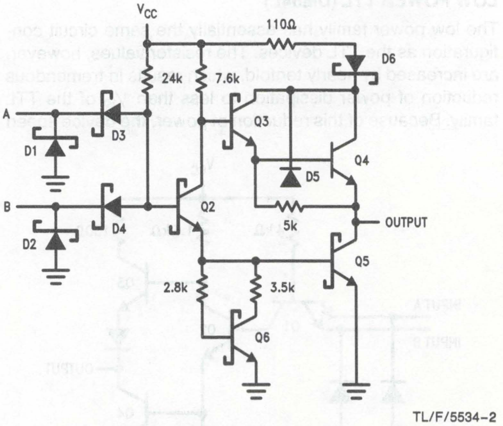
FIGURE 3. DM54LS00/DM74LS00

In addition to the pin-to-pin compatibility of the ALS family, a large number of MSI and LSI functions are introduced in the high density 24-pin 300 mil DIP. These devices offer the designers greater cost effectiveness with the advantages of reduced component count, reduced circuit board real-estate, increased functional capabilities per device and improved speed-power perfomance.

The basic ALS gate schematic is quite similar to the LS gate. It consists of either the PNP transistor or the diode inputs, Darlington transistor pair pull-up and active pull-down (squaring network) at the output. Since the shallower diffusions and thinner oxides will cause ALS devices to be more susceptible to damage from electro-static discharge, additional protection via a base-emitter shorted transistor is included at the input for rapid discharge of high voltage static electricity. Furthermore, the inputs and outputs are clamped by Schottky diodes to prevent them from swinging excessively below ground level. A buried N+ guard ring around all input and output structures prevents crosstalk. The ALS family has a typical power dissipation of 1 mW per gate and typical propagation delay time of 4 ns into a 50 pF/2 kΩ load.

ADVANCED SCHOTTKY (DM54AS/DM74AS)

This family of devices is designed to meet the needs of the system designers who require the ultimate in speed. Utilizing Schottky barrier diode clamped transistors with shallower diffusions and advanced oxide-isolation fabrication techniques, the AS family achieves the fastest propagation delay that bipolar technology can offer. The AS family has virtually the same circuit configuration as the ALS family. It has PNP transistor or diode inputs with electrostatic protection base-emitter shorted transistors. The output totem-pole consists of a Darlington pair transistor pull-up and an active



TL/F/5534-2

FIGURE 3a. 54/74LS00

pull-down squaring network. The inputs and outputs are Schottky clamped to attenuate critical transmission line reflections. In addition, the circuit contains the "Miller Killer" network at the output section to improve output rise time and reduce power consumption during switching at high repetition rates. The AS family yields typical power dissipation of 7 mW per gate and propagation delay time of 1.5 ns when driving a 50 pF/2 kΩ load.

FAST® TECHNOLOGY

FAST (Fairchild Advanced Schottky TTL) circuits are made with the advanced isoplanar II process, which produces transistors with very high, well-controlled switching speeds, extremely small parasitic capacitances and f_T in excess of 5 GHz. Isoplanar is an established National process, used for years in the manufacture of bipolar memories. CMOS, subnanosecond ECL and I^3L^{TM} (Isoplanar Integrated Injection Logic) LSI devices.

In the isoplanar process, components are isolated by a selectively grown thick oxide rather than the p^+ isolation region used in the planar process. Since this oxide needs no separation from the base-collector regions, component and chip sizes are substantially reduced. The base and emitter ends terminate in the oxide wall; masks can thus overlap the device area into the isolation oxide. This overlap feature eliminates the extremely close tolerances normally required for base and emitter masking, and the standard photolithographic processes can be used.

SELECTING A FAMILY

Two factors shoud be considered when choosing a logic family for application, speed and power consumption. New logic families were created to improve the speed or lower the power consumption of the previous families. The following tables rate each family.

Speed		Power Consumption	
Fastest	AS/F	Low	L
	S		ALS
↓	ALS	↓	LS
	LS		F
	TTL		AS
	L		TTL
Slowest		High	S

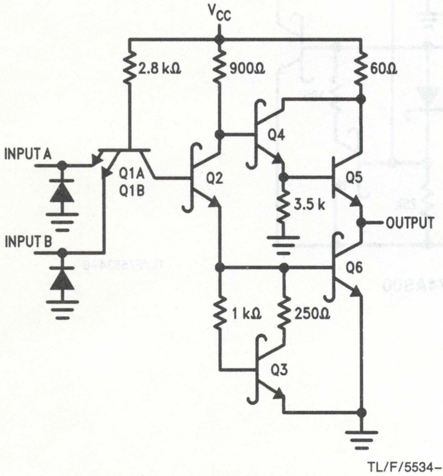


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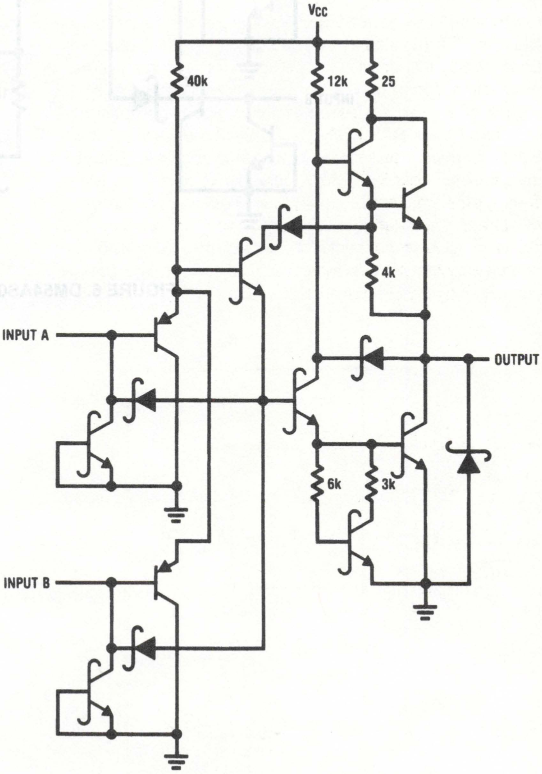
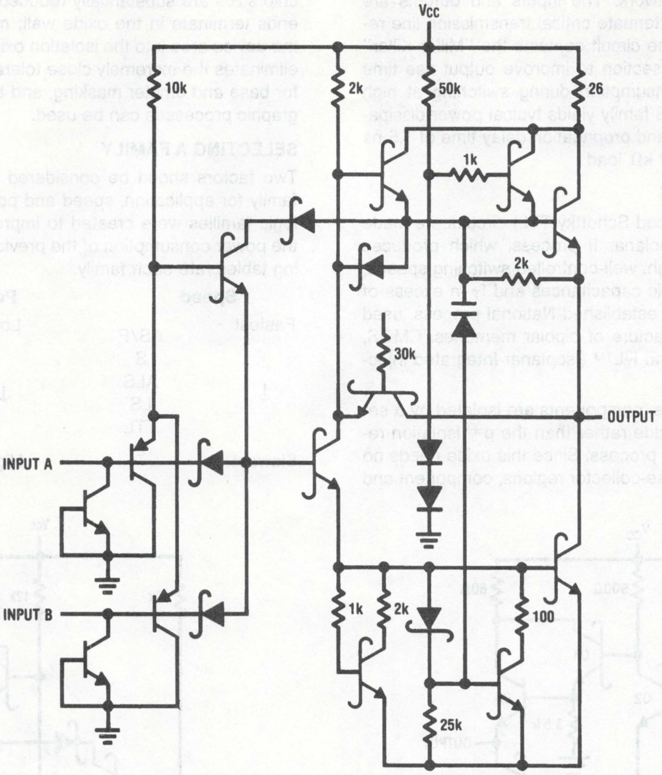
FIGURE 4. DM54S00/DM74S00



TL/F/5534-5

FIGURE 5. DM54ALS00/DM74ALS00


VCC
10k
2k
50k
26
1k
2k
30k
OUTPUT
INPUT A
INPUT B
1k
2k
100
25k

TL/F/5534–6

FIGURE 6. DM54AS00/DM74AS00

National Semiconductor

Consolidation of National Semiconductor and Fairchild Semiconductor

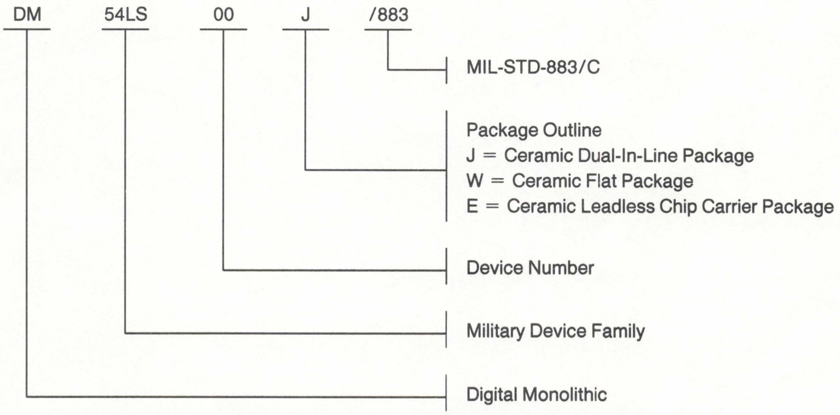
The combination of National Semiconductor and Fairchild Semiconductor provides the largest selection of Bipolar Logic Devices available anywhere. Recognizing that two of the major product lines overlap—Low Power Schottky and Standard TTL—both the Mil/Aero and Commercial products were consolidated so as to have the least impact on their customers.

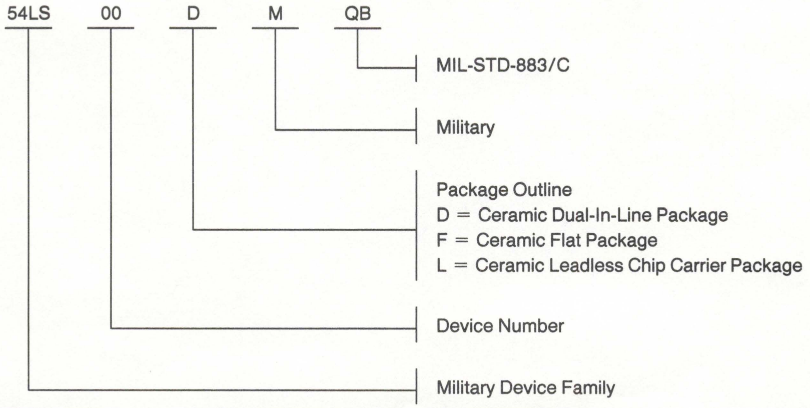
Military/Aerospace Products

All of the Mil/Aero MIL-STD-883 devices were maintained for both National and Fairchild. In other words, the same mask set, fab processes and electrical tests and specifications were continued for all devices previously made by Fairchild Semiconductor as well as National Semiconductor, whether there was duplication of a device or not. For example, the QUAD 2-INPUT NAND Gates, DM54LS00 and 54LS00 are both available. The former's performance is described by RET's (Reliability Electrical Test specifications); and the latter's by a Table I. This is done to prevent considerable inconvenience to our customers who would have had to modify their Source Control Drawings were a change made to the device or its name.

While the datasheets in this databook do not describe the full performance of the Mil/Aero devices, the Table I and/or the RET's do, and may be obtained through your local Field Sales Offices or Representatives.

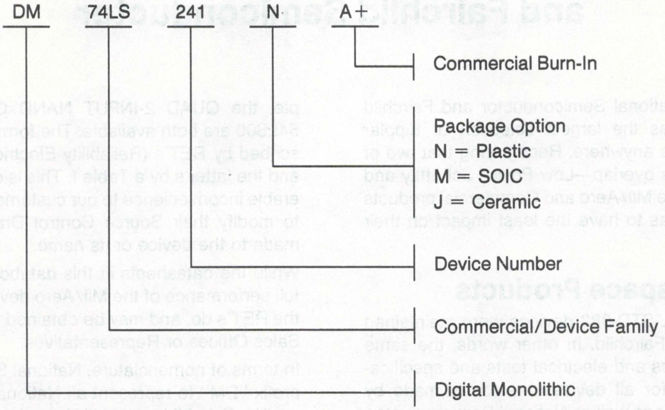
In terms of nomenclature, National Semiconductor uses the prefix "DM" to represent all National-origin Mil/Aero devices. The Fairchild-origin Mil/Aero devices uses no "DM" prefix. Ordering information is included as well.


DM
54LS
00
J
/883
MIL-STD-883/C
Package Outline
J = Ceramic Dual-In-Line Package
W = Ceramic Flat Package
E = Ceramic Leadless Chip Carrier Package
Device Number
Military Device Family
Digital Monolithic


54LS
00
D
M
QB
MIL-STD-883/C
Military
Package Outline
D = Ceramic Dual-In-Line Package
F = Ceramic Flat Package
L = Ceramic Leadless Chip Carrier Package
Device Number
Military Device Family

Commercial Products

The majority of products in the Low Power Schottky, Schottky and TTL logic families produced by National and Fairchild are nearly identical in performance and considerably overlap in portfolio size. All of the sole source functions were retained after the consolidation to minimize the impact to our customers. Fairchild devices that remain in the logic family portfolios are now designated by the National nomenclature. Where a Fairchild device was named 74LS373PC, it will now be referenced to as a DM74LS373N. Please refer to the ordering format below.


DM
74LS
241
N
A+
Commercial Burn-In
Package Option
N = Plastic
M = SOIC
J = Ceramic
Device Number
Commercial/Device Family
Digital Monolithic

IC Device Testing

Understanding the intent and practice of IC device testing is vital to insuring both the quality and proper usage of integrated circuits. All National Semiconductor data sheets list the AC and DC parameters with min and/or max limits, along with forcing functions. Understanding when a part fails the limit, and which forcing functions are really tighter, is critical when determining if an IC device is good or bad.

All of National's databook parameters are defined and guaranteed for "worst-case testing." Input loading currents (fan-in) are tested at the input and V_{CC} levels that most increase that loading, while the output drive capability (fan-out) is tested at the input and V_{CC} levels that most decrease that capability. I_{CC} is tested with the input conditions and V_{CC} level that yield the greatest I_{CC} value, and V_{CLAMP} is tested such that the negative voltage is maximized for the given clamp current. The fan-in and fan-out specs are contained in the I_{IH}, I_{OH}, I_{IL} and I_{OL} values. To guarantee these fan-in and fan-out limits at 10, the I_{OL} must be at least 10 times the I_{IL} and the I_{OH} must be at least 10 times the I_{IH}. Be aware that the fan-in and fan-out specifications are valid only within a given device family. The standard input loading and output drives are shown in Table I.

Notice that the I_{OL} is at least 10 times the I_{IL} and that the I_{OH} is greater than 10 times the I_{IH}. Also notice that these are "standard" drive and load currents for single sink outputs and inputs. Certain devices may have multiple load inputs where the input line goes to several input structures and has, say, 2 or 3 times the normal I_{IL} and I_{IH} loading.

Certain other devices will have "triple sink" outputs that can drive 3 times the standard I_{OL} and I_{OH} currents. These devices are generally bus drivers, or drivers intended to drive highly capacitive loads. Finally, there are certain devices that have PNP inputs that reduce the I_{IL} loading to typically $-200\ \mu A$, thus allowing an increased DC fan-in of 20. One must therefore be careful when interfacing many different types of devices, even in the same family, and not simply go the "fan-out of 10" rule.

When dealing with any kind of device specification, it is important to note that there exists a *pair* of test conditions that define that test: the forcing function and the limit. Forcing functions appear under the column labeled "Conditions" and define the external operating constraints placed upon the device tested. The actual test limit defines how well the device responds to these constraints. For example, take the parameter $V_{OH(min)}$ for the DM74LS00. It is tested at $V_{CC(min)} = 4.75V$ commercial, using an $I_{OH} = -400\ \mu A$. If we required an $I_{OH} = -800\ \mu A$, this would be a "tighter" test, as the output voltage drops with increased I_{OH}. Hence, a device that would pass the $-800\ \mu A$ I_{OH} would also pass the $-400\ \mu A$ I_{OH}, but not necessarily the other way around. Futhermore, V_{OH} tracks with V_{CC}, which is why $V_{CC(min)}$ is the worst-case testing, and not $V_{CC(max)}$. Finally, forcing inputs to threshold represents the most difficult testing because this puts those inputs as close as possible to the actual switching point and guarantees that the device will meet the V_{IH}/V_{IL} spec.

TABLE I. Fan-In/Fan-Out

Device Family	Input Loading	Output Drive
TTL	$I_{IL} = -1.6$ mA $I_{IH} = 40\ \mu A$	$I_{OL} = 16$ mA $I_{OH} = -400\ \mu A$
Low Power Schottky	$I_{IL} = -400\ \mu A$ $I_{IH} = 20\ \mu A$	$I_{OL} = 4$ mA (Mil) $I_{OL} = 8$ mA (Com) $I_{OH} = -400\ \mu A$
Schottky	$I_{IL} = -2$ mA $I_{IH} = 50\ \mu A$	$I_{OL} = 20$ mA $I_{OH} = -1$ mA

Tables II and III show the "direction" of the looser/tighter testing for most common DC parameters. Notice that one can tighten either the forcing function or the limit, or both. Tightening either one is sufficient to insure a tighter test. Also notice the difference between max and min limits. For I_{OS} (double-ended limits), even though −20 mA is more positive than −100 mA, and is mathematically the max limit, the magnitude of the number is the determining factor when deciding which is the max limit. The negative sign simply implies the direction that the current is going, with a negative current leaving the device, and a positive current entering the device. Table II shows the direction of tighter forcing functions, while Table III shows the direction of tighter limits.

TABLE II. Looser/Tighter Forcing Functions Example: DM74LS00

Condition	Test	Looser	Nominal	Tighter	Units
I_{IK}	V_{IK}	−17	−18	−19	mA
I_{OH}	V_{OH}	−350	−400	−450	μA
I_{OL}	V_{OL}	3	4	5	mA
V_I	I_I	6.5	7	7.5	V
V_{IH}	I_{IH}	2.6	2.7	2.8	V
V_{IL}	I_{IL}	0.5	0.4	0.3	V
V_O	I_{OS}	0.1	0.0	−0.1	V
V_{CC}	I_{CC}	5.0	5.5	6.0	V

TABLE III. Looser/Tighter Test Limits Example: DM74LS00

Parameter	Looser	Nominal	Tighter	Units
$V_{IH(min)}$	2.1	2.0	1.9	V
$V_{IL(max)}$	0.7	0.8	0.9	V
$V_{IK(max)}$	−1.6	−1.5	−1.4	V
$V_{OH(min)}$	2.6	2.7	2.8	V
$V_{OL(max)}$	0.6	0.5	0.4	V
$I_{I(min)}$	6.5	7.0	7.5	V
$I_{IH(max)}$	50	40	30	μA
$I_{IL(max)}$	−450	−400	−390	μA
$I_{OS(max)}$	−110	−100	−90	mA
$I_{OS(min)}$	−10	−20	−30	mA
$I_{CCH(max)}$	1.7	1.6	1.5	mA
$I_{CCL(max)}$	4.5	4.4	4.3	mA

Following are the test set-ups that are used to test the DC parametrics. In each case, the gate connection, equivalent circuit schematic and resultant voltage/current plot are shown.

The indicated graphs are typical of LS products and are similiar to other bipolar logic families. The schematics shown are for single inversion devices and represent generalized circuits.

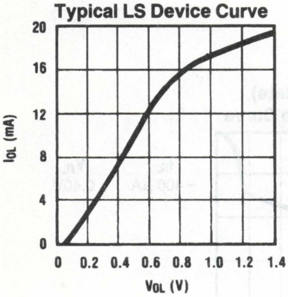
OUTPUT VOLTAGE LOW LEVEL (V_{OL})

Both inputs are connected to logic "1" values (assuming an inverting gate) and forced at the V_{IH} specs. V_{CC} minimum is used, and I_{OL} is forced on the output. The resulting V_{OL} is measured. For typical LS products, the military and commercial test points are indicated on the V_{OL} vs I_{OL} graph. In each case, the device must not exceed the V_{OL} spec when the I_{OL} current is being forced.

OUTPUT VOLTAGE HIGH LEVEL (V_{OH})

One input is tied high (any value above 2.0V) and the other input is forced at the V_{IL} threshold (assuming a single inversion gate). The minimum V_{CC} value is used. Each input is tested independently and the I_{OH} current is forced. The resulting V_{OH} is measured. The V_{OH} vs I_{OH} graph shows the military and commercial V_{OH}/I_{OH} test points for standard LS products.

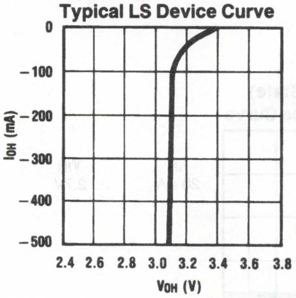
V_{OL} vs I_{OL}
Typical LS Device Curve



	I_{OL}	V_{OL}
Mil:	4.0 mA	0.40V
Com:	8.0 mA	0.50V

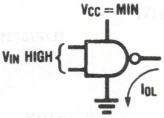
TL/F/6731-1

V_{OH} vs I_{OH}
Typical LS Device Curve

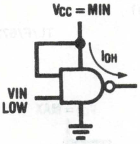


	I_{OH}	V_{OH}
Mil:	−400 μA	2.5V
Com:	−400 μA	2.7V

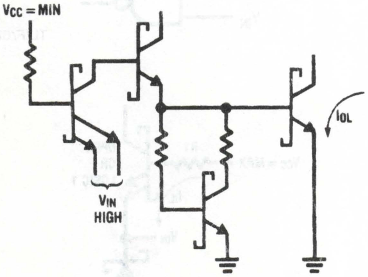
TL/F/6731-2



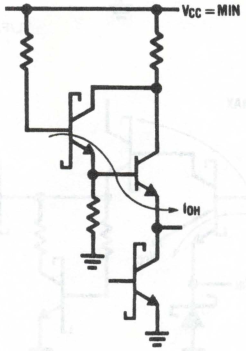
TL/F/6731-3



TL/F/6731-4



TL/F/6731-5



TL/F/6731-6

INPUT CURRENT HIGH LEVEL (I_{IH})

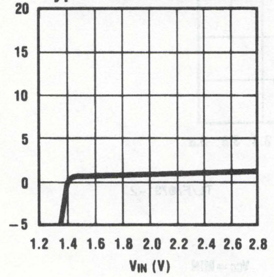
I_{IH} tests the input leakage in the high state. For MET, diode, and PNP input, the test set-up consists of all inputs except the one under test tied high (greater than V_{IH}). The remaining input has the V_{IH} value forced upon it, and the resultant I_{IH} is measured. This test checks for emitter-to-collector inverse transistor action for MET inputs, and reverse bias leakage for diode and PNP inputs.

For MET inputs, there is also an additional set-up for I_{IH} testing that checks for emitter-to-emitter transistor action. This is done with all the other inputs tied to ground.

MAXIMUM INPUT CURRENT (I_I)

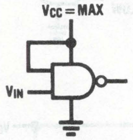
I_I or BV_{IN} testing is the same as the emitter-to-collector leakage test (I_{IH}) and guarantees that the input will not pass more than the specified current at the stated specification (100 µA at 7V for LS).

I_{IN} vs V_{IN} (High State)
Typical LS Device Curve

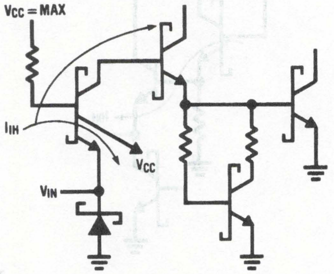


I_{IH}	V_{IH}
20 µA	2.7V

TL/F/6731-7



TL/F/6731-9



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INPUT CURRENT LOW LEVEL (I_{IL})

One input at a time is tested with the other inputs tied to a solid "1" value. V_{CC} is set to the maximum value and the V_{IL} value is forced. I_{IL} is then measured.

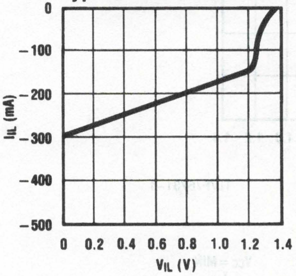
$$I_{IL} = \frac{[V_{CC} - (V_{IL} + V_{BE})]}{R1} \quad \text{Standard Inputs}$$

$$I_{IL} = \frac{[V_{CC} - (V_{IL} + V_{SH})]}{R1} \quad \text{Diode Inputs}$$

$$I_{IL} = \frac{[V_{CC} - (V_{IL} + V_{BE})]}{R1 \times \beta} \quad \text{PNP Inputs}$$

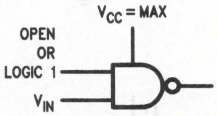
I_{IL} is intended to measure the value of the base pull-up resistor on the input, and to guarantee the maximum input load an IC presents.

I_{IN} vs V_{IN} (Low State)
Typical LS Device Curve

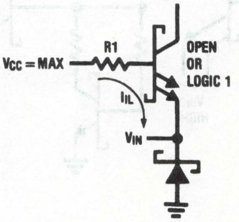


I_{IL}	V_{IL}
−400 µA	0.40V

TL/F/6731-8



TL/F/6731-10



TL/F/6731-12

OUTPUT SHORT CIRCUIT CURRENT (I_{OS})

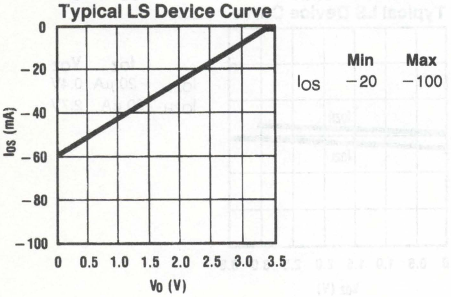
I_{OS} is measured with $V_{CC(max)}$ and the 0V forced on the output while it is in the high state. The resultant current is measured. The purpose of this is to check the I_{OS} resistor that forms the Darlington's collector pull-up. This parameter is important as it reflects both the maximum current the device will draw and the maximum drive it will provide when it is switching from low to high.

Caution must be taken when measuring TTL, LS and S outputs as the power dissipated on the die will be substantial. I_{OS} shorts should not be maintained in excess of one second or damage to the device may result.

SUPPLY CURRENT HIGH LEVEL (I_{CCH}) AND SUPPLY CURRENT LOW LEVEL (I_{CCL})

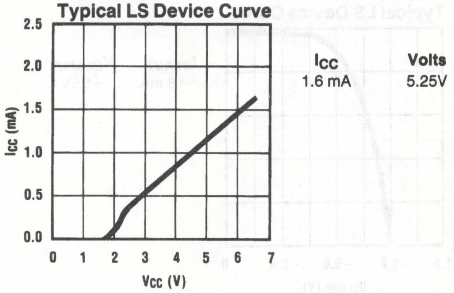
Both I_{CCH} and I_{CCL} are tested using the V_{CC} maximum value. The inputs are set to the values necessary to achieve the output in the desired state. All outputs are left open, neither sourcing nor sinking current. The goal of this test is to guarantee the maximum quiescent operating power that the device will draw.

V_O vs I_{OS}
Typical LS Device Curve

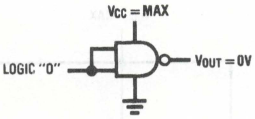


TL/F/6731–13

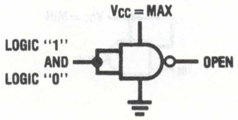
I_{CCL} vs V_{CC}
Typical LS Device Curve



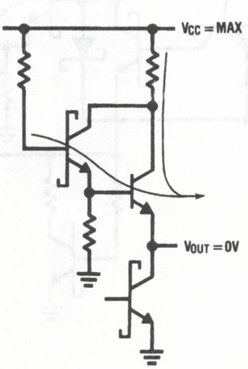
TL/F/6731–14



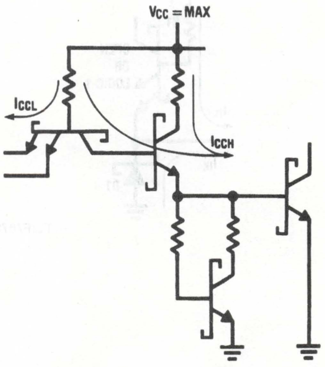
TL/F/6731–15



TL/F/6731–16



TL/F/6731–17



TL/F/6731–18

INPUT CLAMP VOLTAGE (V_{IC} OR V_{IK})

$V_{CLAMP}(V_{IK})$ is measured with all but one input tied high and the I_{IK} current forced on the remaining input. V_{CC} is set to the minimum and the V_{IK} voltage is measured.

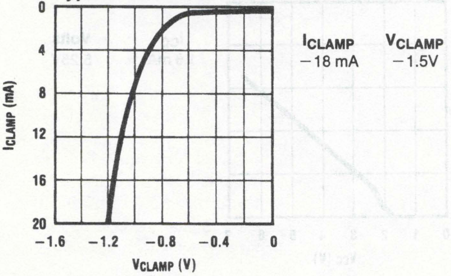
OUTPUT TRI-STATE CURRENT HIGH LEVEL (I_{OZH}) AND OUTPUT TRI-STATE CURRENT LOW LEVEL (I_{OZL})

TRI-STATE® I_{SINK} and I_{SOURCE} are measured with the output control input tied to the appropriate threshold value (usually V_{IL} = 0.8V) and with $V_{CC(max)}$. This is to insure that the output will have the greatest drive capability and the TRI-STATE control can effectively "turn off" the output under these conditions.

TRI-STATE I_{SINK}: Output is set in the high state and then TRI-STATE mode. V_{OZL} = 0.4V is then applied. The current drawn out of the device is then measured.

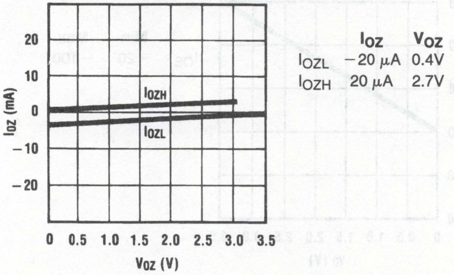
TRI-STATE I_{SOURCE}: Output is set in the low state and then TRI-STATE mode. V_{OZH} = 2.7V is then applied. The current drawn into the device is then measured.

V_{CLAMP} vs I_{CLAMP}
Typical LS Device Curve

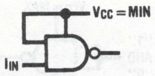


TL/F/6731-19

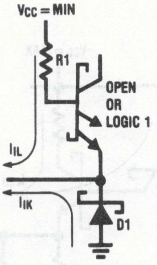
I_{OZH} vs V_{OZH}
(TRI-STATE I_{SOURCE}),
I_{OZL} vs V_{OZL}
(TRI-STATE I_{SINK})
Typical LS Device Curve



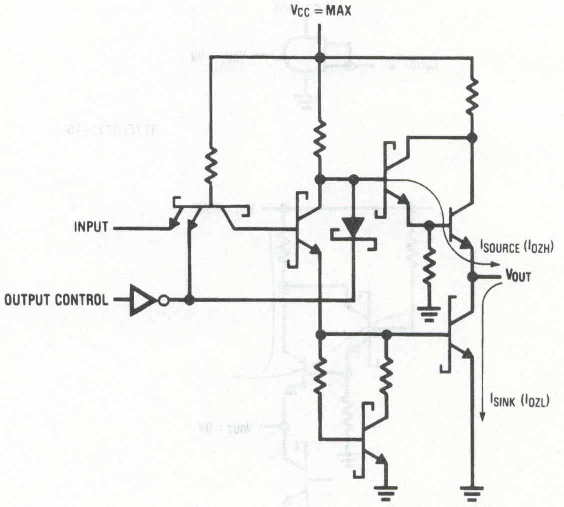
TL/F/6731-20



TL/F/6731-21



TL/F/6731-22

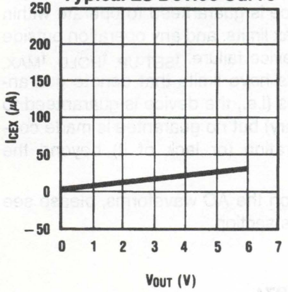


TL/F/6731-23

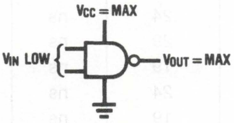
HIGH LEVEL OUTPUT CURRENT (OPEN-COLLECTOR DEVICES ONLY)

I_{CEX} is tested with the output in the high state. V_{CC} is set to 5.0V and the specified voltage (5.5V for LS) is applied to the output. The inputs are at the threshold values (0.8V and 2.0V, depending upon the logic to put output in the high state) and the resulting I_{CEX} leakage current is measured.

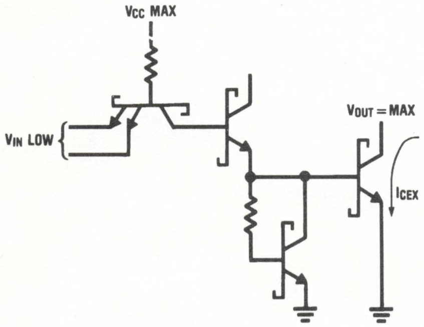
I_{CEX} vs V_{OUT}
(Open-Collector Device)
Typical LS Device Curve



TL/F/6731-24



TL/F/6731-25



TL/F/6731-26

AC SWITCHING CHARACTERISTICS

The AC switching characteristics are generally measured in units of time (commonly in nanoseconds), and define how long it takes for the signal to propagate from the input to the output. The definitions used in determining the pass/fail status of each limit are not the same for AC as they are for DC. The distinction lies in the fact that for DC operation there exists one characteristic V-I curve on which the device must operate. Devices are good if they operate on the correct side of the limit, and bad if they operate on the wrong side of the limit. When dealing with certain AC parameters (f_{MAX}, $t_{SET\text{-}UP}$, t_{HOLD}, $t_{RELEASE}$, t_{PW}), the device can, and usually does, operate on both sides of the databook limit. The limit really implies a boundary that all devices are guaranteed to exceed. Depending upon the parameter, the device will either operate at all values above and some below the limit, or it will operate at all values below and some above the limit. In each case, the device is only guaranteed to operate for all values on one side of the limit. Although the device will also operate beyond the limit, it is not guaranteed to. Furthermore, device operation beyond the limit is not considered a failure. For instance, take the f_{MAX} parameter with a min limit of 25 MHz. All devices are guaranteed to operate at all frequencies below 25 MHz and will operate in excess of 25 MHz, although this is not guaranteed. Now, take the example of $t_{SET\text{-}UP}$ with a minimum limit of 25 ns. All of the devices are guaranteed to operate with a set-up time of 25 ns and longer, and will operate with set-up times below 25 ns, although this is not guaranteed either. Be aware that both of these specifications are listed in the minimum column in the databook, but the interpretation of what is failing differs significantly.

Propagation delays (called prop delays and denoted by the symbols t_{PHL} and t_{PLH}) are specified as maximum limits, and guarantee the maximum time one must wait to insure that the correct data has appeared at the device's output. Each propagation delay is specified from one input to one output only.

Input set-up and hold times (including $t_{RELEASE}$) specify how long one input must be stable at a particular logic level prior to an action occurring at another input. For example, take the DM54/74LS74 positive-edge-triggered D flip-flop. The "set-up 1" specification defines how long a logic "1" must be present *and* stable at the DATA input prior to the positive edge of the CLOCK to insure that the device will recognize that data as a "1". There also exists a "hold 1" specification which specifies how long a logic "1" must be held after the active edge of CLOCK for the device to recognize that logic "1". Both the set-up and hold times must always be met or the device will not necessarily bring in the proper data. Set-up times are generally positive, while hold times may be either positive or negative, usually negative. The meaning of a negative hold time is that the data may be removed from the input prior to the active edge of CLOCK, and the CLOCK will still bring in the desired data. Set-up and hold times are specified as minimum values, since this defines the minimum time data must be stable prior to any change at the CLOCK input. Removing the data sooner than the minimum time may cause improper action on the part of the device.

$t_{RELEASE}$ is specified on devices where there is an input that must be set inactive prior to the active edge of CLOCK. Such inputs are usually overriding inputs like CLEAR and PRESET. With CLEAR active, it will prevent the device from switching on the CLOCK signal. $t_{RELEASE}$ is defined as the time it takes for the CLEAR input to "release" the device for clocking action, and is specified as a minimum. This represents the maximum delay required between CLEAR going inactive and the active edge of CLOCK to insure proper device operation.

All devices that have a CLOCK input also have a specification that defines the maximum speed that the CLOCK can be driven, called f_{MAX}. This specification is defined as a minimum specification and states that all of the devices will be able to operate at frequencies up to 25 MHz. For the DM54/74LS74 with an f_{MAX} of 25 MHz, all of the devices are guaranteed to operate at all clock frequencies, up to and including 25 MHz. Although no devices are guaranteed to operate above f_{MAX} (only below it), most devices will operate beyond the maximum specification. The minimum limit does *not* state that the device will not operate below f_{MAX} or that any devices that do are bad, but rather that all the devices will operate up to the limit.

Table IV shows the direction of the tighter testing for the more common AC parameters. All prop dealys (those AC parameters that have the symbols t_{PLH} or t_{PHL}) have simple min/max limits. The device is guaranteed to operate within the bounds of the min/max limits, and any operation outside these limits denotes a device failure. $t_{SET\text{-}UP}$, t_{HOLD}, f_{MAX}, and $t_{RELEASE}$ parameters have limits that denote guaranteed operation boundaries (i.e., the device is guaranteed to operate up to the boundary) but no guarantee is made concerning the device operation (or lack of it) beyond the boundary.

For detailed information on the AC waveforms, please see the test waveforms in this section.

TABLE IV. Looser/Tighter AC Test Limits Example: DM74LS74

Test	From	Looser	Nominal	Tighter	Units
$f_{max(min)}$		24	25	26	MHz
$t_{PLH(max)}$	CLR, PRE, CLK	26	25	24	ns
$t_{PHL(max)}$	CLR, PRE, CLK	31	30	29	ns
$t_{W(min)}$	CLOCK HIGH	21	20	19	ns
$t_{W(min)}$	PRE, CLR LOW	26	25	24	ns
$t_{SET\text{-}UP(min)}$	DATA HIGH	21	20	19	ns
$t_{SET\text{-}UP(min)}$	DATA LOW	21	20	19	ns
$t_{HOLD(min)}$	All DATA	1	0	−1	ns

National Semiconductor

Functional Index

Arithmetic Operators

Function/Description		Type	Technology								No. of Bits	No. of Pins
			STD TTL		L		S		LS			
			54	74	54	74	54	74	54	74		
Adder/Binary 4-Bit with Fast Carry		'83	X						X	X	4	16
		'283	X	X			X	X	X	X	4	16
ALU with Carry Look Ahead		'181	X				X	X	X	X	4	24
		'381						X			4	20
		93S41						X			4	24
Binary to BCD Converter		'185		X							6	16
BCD to Binary Converter		'184		X							6	16
Lookahead Carry Generator		'182					X	X				16
Multiplier/Twos Complement		93S43						X			4×2	24
9-Bit Parity Generator/Checker		'180	X	X							9	14
		'280					X	X			9	14
		93S62						X			9	14
12-Bit Parity Generator/Checker		9348	X								12	16
Comparator	4-Bit Magnitude with Expander	'85	X	X					X	X	4	16
	5-Bit Magnitude	9324	X	X	X						5	16
	Hi-Speed 6-Bit Identity with Expander	93S46						X			6	16
	Hi-Speed 6-Bit Identity with OC*	93S47						X			6	16
	6-Bit Unified Bus with OC*	7136	X								6	16
	6-Bit Magnitude with OC*	7160	X								6	16
	10-Bit Magnitude with OC*	7130	X								10	24
6-Bit Binary Rate Multiplier		'97	X	X							64	16

*OC : Open Collector

Counters

Function/Description	Type	Technology								Up/Down	Clock Edge	No. of Pins
		STD TTL		L		S		LS				
		54	74	54	74	54	74	54	74			
4-Bit Binary Counter	'93	X	X	X					X		↓	14
	'293								X		↓	14
Synchronous Modulo 64-Bit Rate Multiplier	'97	X	X								↑	16
Asynchronous Decade Counter	'90	X	X					X	X		↓	14
Synchronous 4-Bit Binary Counter with Asynchronous Clear	'161	X	X			X	X	X	X		↑	16
Synchronous Presettable BCD Decade Counter	'160	X						X	X		↑	16
Synchronous 4-Bit Binary Counter with Synchronous Clear	'163	X	X			X	X	X	X		↑	16
Synchronous Presettable BCD Decade Counter	'162							X	X		↑	16
Synchronous Bidirectional BCD Decade Counter	'168							X		X	↑	16
Synchronous 4-Bit Up/Down Binary Counter	'169							X	X	X	↑	16
Synchronous Up/Down Decade Counter with Mode Control	'190							X	X	X	↑	16
Synchronous 4-Bit Up/Down Binary Counter with Mode Control	'191	X	X					X	X	X	↑	16
Synchronous 4-Bit Up/Down Binary Counter with Dual Clock	'193	X						X	X	X	↑	16
Asynchronous Presettable Decade Counter	'196								X		↓	14
Asynchronous Presettable Binary Counter	'197		X						X		↓	14
BCD Decade Counter/4-Bit Binary Counter	9310			X							↑	16
	9316	X	X	X							↑	16
TRI-STATE® Programmable 4-Bit Binary Counter	7556	X									↑	16
Decade Counter with Separate Up/Down Clocks	'192							X	X	X	↑	16
Decade Counter	'290								X		↓	14
Dual Decade (Bi-Quinary) Counter	'390								X		↓	16
Dual 4-Bit Binary Counter	'393								X		↓	14
Dual Decade Counter	'490							X	X		↓	16

Decoders/Demultiplexers

Function/Description	Type	Technology								Address Input	Active Low Enable	Active Low Outputs	No. of Pins
		STD TTL		L		S		LS					
		54	74	54	74	54	74	54	74				
Dual 1 of 4	9321	X	X	X						2+2	1+1	4+4	16
	'139					X	X	X	X	2+1	1+1	4+4	16
	'155	X	X					X	X	2	2+1	4+4	16
	'156							X	X	2	2+1	4+4	16
1 of 8	9301	X	X		X					3	1	8	16
	'45	X	X							3	1	8	16
	'42	X	X					X	X	3	1	8	16
	'138					X	X	X	X	3	2	8	16
	'145	X	X							3	1	8	16
1 of 10	9301	X	X	X						4 (BCD)		10	16
	'45	X	X							4 (BCD)		10	16
	'42	X	X					X	X	4 (BCD)		10	16
	'145	X	X							4 (BCD)		10	16
1 of 16	9311	X	X							4	2	16	24
	'154	X	X					X	X	4	2	16	24
8 to 3-Line Priority Encoder	9318	X	X							8			16
	'148	X								8			16

Display Decoders/Drivers

Function/Description	Type	Technology								Active Hi/Low	Ripple Blanking	No. of Pins
		STD TTL		L		S		LS				
		54	74	54	74	54	74	54	74			
1 of 10 Driver (OC*)	'45	X	X							L		16
	'145	X	X							L		16
BCD to 7-Seg Decoder/Driver (OC*)	'46		X							L	X	16
	'47	X	X					X	X	L	X	16
	'49							X		H	X	14
	'247							X	X	L	X	16
	'249							X	X	H	X	16
	'347							X	X	L	X	16
	'447							X	X	L	X	16
BCD to 7-Seg Decoder/Driver	'48							X	X	H	X	16
	'248							X	X	H	X	16
	9370		X							L	X	16
	9374		X							L	X	16
	9368		X							H	X	16

*OC : Open Collector

Flip Flops—Single & Dual

Function/Description	Type	Technology								Inputs	Clock Edge	Direct Set	Direct Clear	No. of Pins
		STD TTL		L		S		LS						
		54	74	54	74	54	74	54	74					
Dual JK	'73	X	X	X				X	X	J, K	╲		X	14
	'76	X	X							J, K	╲	X	X	16
	'107	X						X	X	J, K	╲		X	14
	'109	X					X	X	X	J, K̄	╱	X	X	16
	'112					X	X	X	X	J, K	╲	X	X	16
	'113					X	X	X		J, K	╲	X*		14
	'114							X		J, K	╲	X	X	14
	'72			X						J, K	╲	X	X	14
Dual D	'74	X	X	X		X	X	X	X	D	╱	X	X	14

*Does not apply to LS.

Flip Flops—Multiple

Function/Description	Type	Technology								Data Inputs	Clock Inputs	Broadside Pinout	TRI-STATE Output	No. of Pins
		STD TTL		L		S		LS						
		54	74	54	74	54	74	54	74					
4-Bit D Flip Flop	'175	X	X			X	X	X	X	4×D	╱			16
6-Bit D Flip Flop	'174	X	X			X	X	X	X	6×D	╱		X	16
8-Bit D Flip Flop	'374					X	X	X	X	8×D	╱		X	20
	'377							X	X	8×D	╱			20
	'534								X	8×D	╱		X	20
	'574								X	8×D	╱	X	X	20
	'564								X	8×D	╱	X		20
	'373					X	X	X	X	8×D	╱		X	20
8-Bit Multiple Port Register	9338	X	X	X						1×D	L			16
Quad 2-Port Register	'298	X						X	X	2×4×D	╲			16

Gates

Function/Description		Type	Technology								No. of Pins
			STD TTL		L		S		LS		
			54	74	54	74	54	74	54	74	
NAND	Quad 2-Input NAND	'00	X	X	X		X	X	X	X	14
	Quad 2-Input NAND with OC*	'01	X	X							14
		'03	X	X				X	X	X	14
	Triple 3-Input NAND	'10	X	X	X		X	X	X	X	14
	Triple 3-Input NAND with OC*	'12							X	X	14
	Dual 4-Input Schmitt Trigger	'13							X	X	14
	Dual 4-Input NAND	'20	X	X			X	X	X	X	14
	Dual 4-Input NAND with OC*	'22							X	X	14
	8-Input NAND Gate	'30	X	X			X	X	X	X	14
	Quad 2-Input Schmitt Trigger NAND	'132	X	X				X	X	X	14
	13-Input NAND	'133					X	X	X	X	16
NOR	Quad 2-Input NOR	'02	X	X	X		X	X	X	X	14
	Dual 4-Input NOR with Strobe	'25	X	X							14
	Triple 3-Input NOR	'27		X					X	X	14
	Dual 5-Input NOR	'260							X	X	14
AND	Quad 2-Input AND	'08	X	X			X	X	X	X	14
	Quad 2-Input AND with OC*	'09	X	X				X	X	X	14
	Triple 3-Input AND	'11		X			X	X	X	X	14
	Triple 3-Input AND with OC*	'15							X	X	14
	Dual 4-Input AND	'21							X	X	14
Exclusive-OR	Quad Ex-OR	'86	X	X			X	X	X	X	14
	Quad 2-Input Ex-OR with OC*	'136							X	X	14
OR	Quad 2-Input OR/	'32	X	X			X	X	X	X	14
Exclusive-NOR	4-Bit Quad Ex-NOR with OC*	9386		X							14
	Quad 2-Input Ex-NOR with OC*	'266							X	X	14
AND OR Gates Invert	Expandable Dual 2-Wide 2-Input	'50		X							14
	Dual 2-Wide 2-Input	'51	X	X				X	X	X	14
	4-Wide 2-Input	'54							X	X	14
	2-Wide 4-Input	'55							X	X	14
	4-Wide	'64					X	X			14
Inverters	Hex Inverters	'04	X	X	X		X	X	X	X	14
	Hex Inverter with OC*	'05	X	X				X	X	X	14
	Hex Schmitt Trigger Inverter	'14	X	X					X	X	14

*OC : Open Collector

Latches

Function	Type	Technology								Data Inputs	Enable Inputs (Level)	TRI-STATE Outputs	No. of Pins
		STD TTL		L		S		LS					
		54	74	54	74	54	74	54	74				
4-Bit D Latch	'75	X	X					X	X	4×D	2(H)		16
	'375							X	X	4×D	2(H)		16
Dual 4-Bit D Latch	9308	X	X	X						8×D	2×2 AND		24
4-Bit D Latch	9314	X	X	X						4×D	1(L)		16
8-Bit D Latch	'373					X	X	X	X	8×D*	1(H)	X	20
	'533								X	8×D	1(H)	X	20
	'563								X	8×D	1(H)	X	20
	'573								X	8×D	1(L)	X	20
8-Bit Addressable Latch	9334	X	X	X						1×D	1(L)		16
	'259							X	X	1×D	1(L)		16
Dual 4-Bit Addressable Latch	'256							X	X	8×D	2(L)		16
4-Bit RS Latch	'279	X	X					X	X	$4\times(\overline{R}\,\overline{S})$			16

*"D" only for SKY.

Line and Bus Drivers/Transceivers/Receivers

Function/Description	Type	Technology								No. of Pins
		STD TTL		L		S		LS		
		54	74	54	74	54	74	54	74	
Quad 2 NAND Buffer	'37	X	X					X	X	14
Quad 2 NAND Buffer with OC*	'26	X	X					X	X	14
	'38	X	X					X	X	14
	'39		X							14
	'96101		X							14
Dual 4 NAND Buffer	'40	X	X			X	X	X	X	14
	'140					X	X			14
Quad 2 NOR Buffer	'28							X	X	14
Quad 2 NOR Buffer with OC*	'33							X	X	14
Quad TRI-STATE Buffer	'125	X	X					X	X	14
	'126							X	X	14
Hex Buffer/Driver with High Voltage OC*	'07	X	X							14
	'17	X	X							14
Hex Inverting Buffer/Driver with High Voltage OC*	'06	X	X							14
	'16	X	X							14
Hex TRI-STATE Buffer/Bus Driver	'365	X						X	X	16
	'367	X						X	X	16
Hex Inverting TRI-STATE Buffer/Bus Driver	'368	X						X	X	16
	'366							X	X	16
Octal Buffer/Line Driver with TRI-STATE Outputs	'540								X	20
Octal TRI-STATE Buffer/Bus Driver	'465								X	20
	'467								X	20
Octal TRI-STATE Inverting Buffer/Bus Driver	'466								X	20
	'468								X	20
Octal TRI-STATE Buffer/Line Driver/Line Receiver	'241					X	X	X	X	20
	'244					X	X	X	X	20
Octal TRI-STATE Inverting Buffer/Line Driver/Line Receiver	'240					X	X	X	X	20
	'243								X	14
Octal TRI-STATE Bus Transceiver	'245							X	X	20
	'645								X	20

*OC: Open Collector

Monostables (One-Shots)

Function/Description	Type	Technology								No. of Inputs		Resettable	Min Output (t_W) ns	No. of Pins
		STD TTL		L		S		LS						
		54	74	54	74	54	74	54	74	Pos.	Neg.			
Single Retriggerable	9601	X	X							2	2		50	14
	'122	X	X							2	2	X	45	14
	'122								X	2	2		40	14
Single Non-Retriggerable	'121	X	X							1	2		40	14
Dual Retriggerable	9602	X	X	X						1	1	X	72	16
	96S02						X			1	1	X	27	16
	96LS02							X	X	1	1	X	35	16
	'123	X	X							1	1	X	45	16
	'123								X	1	1	X	40	16
Dual Non-Retriggerable	'221								X	1	1	X	40	16

Multiplexers

Function/Description	Type	Technology								Enable Inputs	True Outputs	Complementary Outputs	No. of Pins
		STD TTL		L		S		LS					
		54	74	54	74	54	74	54	74				
Quad 2-Input	9322	X	X	X						1	X		16
	'157	X	X			X	X	X	X	1	X		16
	'158					X	X	X	X	1		X	16
	'257					X	X	X	X	1	TRI-STATE		16
	'258					X	X	X	X	1		TRI-STATE	16
	'298	X						X	X	Clocked	X		16
Dual 4-Input	'153	X	X			X	X	X	X	2	X		16
	'253					X	X	X	X	2	TRI-STATE		16
	'352							X	X	2		X	16
	'353							X	X	2		TRI-STATE	16
	9309	X	X	X							X	X	16
8-Input	'151	X	X			X	X	X	X	1	X	X	16
	'251					X	X	X	X	1	TRI-STATE	TRI-STATE	16
	'152							X				X	14
	9312	X	X	X						1	X	X	16
Quad 2-Input TRI-STATE	7123	X								1	X		16
16-Input	'150	X	X							1		X	24

Registers

Function/Description	Type	Technology								No. of Bits	Serial Entry	Parallel Entry No. of Bits	Clock Edge	No. of Pins
		STD TTL		L		S		LS						
		54	74	54	74	54	74	54	74					
Parallel In/Parallel Out Shift Right	9300	X	X	X			X			4	J, $\overline{K}$	4S	_/‾	16
	'95	X	X	X				X	X	4	D	4S	‾_	14
	'195					X	X	X	X	4	J, $\overline{K}$	4S	_/‾	16
Parallel In/Parallel Out Shift Right (TRI-STATE)	'295							X	X	4	D	4S	‾_	14
	'395							X	X	4	D	4S	‾_	16
Parallel In/Parallel Out Bidirectional	'194	X				X	X	X	X	4	DR, DL	4S	_/‾	16
Quad D	'173	X	X					X	X	4		4S	_/‾	16
	'379							X	X	4		4S	_/‾	16
Quad 2 Port Register	'298	X						X	X	4		2 D (Mux)	‾_	16
Parallel D Register	'378							X	X	6		6S	_/‾	16
Multiport Register	9338	X	X							8	D		_/‾	16
Serial/Parallel In, Parallel, Serial Out, Shift Right	'322							X	X	8	2D	8S	_/‾	20
Serial In/Parallel Out, Shift Right	'164	X	X					X	X	8	2D		_/‾	14
Parallel/Serial In, Serial Out, Shift Right	'165	X	X					X	X	8	D	8A	_/‾	16
	'166	X							X	8	D	8S	_/‾	16
Successive Approx. Register	'502							X	X	8	D		_/‾	16
	'503							X	X	8	D		_/‾	16
	2503	X								8	D		_/‾	16
Parallel In/Parallel Out Bidirectional (TRI-STATE)	'299						X	X	X	8	DR, DL	8S	_/‾	20
	'323							X	X	8	DR, DL	8S	_/‾	20
Serial In/Serial Out, Shift Right	9328	X	X	X						2×8	2×2 D Mux		_/‾	16
Octal D Register	'273							X	X	8		8S	_/‾	20
Register File (OC*)	'170	X	X					X	X	4×4		4A	‾_	16
Register File (TRI-STATE)	'670							X	X	4×4		4A	‾_	16
8-Bit Shift Register (TRI-STATE)	'952								X	8			_/‾	18
	'962								X	8			_/‾	18
Data Selector/Storage Register	'98			X						4		2 D (Mux)	‾_	16

*S = Synchronous, A = Asynchronous, OC : Open Collector

Glossary of Terms

DC Operating Conditions and Characteristics

GENERAL DEFINITIONS

I: Current is the flow of electric charge from one potential to another through a conductor. The unit of measure is the Ampere, or Amp, abbreviated A. One Amp is equal to the current flowing through one ohm of resistance when one volt is applied across that resistance. Common units found in the semiconductor industry are the milliampere, abbreviated mA, equal to 0.001A and the microampere, abbreviated μA, equal to 0.000001A. Negative current is defined as current flowing out of a device terminal and positive current is defined as current flowing into a device terminal.

V: Voltage, or the electromotive force which causes current to flow through a conductor. One Ampere of current flowing through one ohm of resistance develops a potential difference of one volt across that resistance. The unit of measure is the Volt, abbreviated V, and a common unit is the millivolt, abbreviated mV, equal to 0.001V.

INPUT CURRENT PARAMETERS

I_I Maximum High Level Input Current: Current flowing into an input when that input has the maximum voltage specified for the family applied to it. This test is used to guarantee the minimum reverse breakdown voltage of the input structure.

I_{IH} High Level Input Current: The current flowing into an input when that input has a high level voltage equal to the minimum high level output voltage specified for the family. This test is used to check the emitter-to-emitter leakage and the inverse transistor action of a multi-emitter transistor input, the input leakage of a diode, PNP transistor, or C-B short type of input, and to guarantee the fan-in specified for the family.

I_{IK} Input Clamp Current: The current flowing out of an input when that input is pulled below ground. This test is used to guarantee the integrity of the input clamp diode. The input clamp diode is used to limit the voltage swings on the input by clamping the negative excursions to a level equal to one diode drop below ground. This serves to reduce ringing on an incoming signal. Pulling the input below ground for an extended length of time can cause parasitic transistor action to occur between adjacent tanks on the die which can cause erroneous data to occur on the outputs of the device. To prevent this, voltages on the inputs during operation (other than high speed ringing) should be limited to no more than 0.5V below ground at all times.

I_{IL} Low Level Input Current: The current flowing out of an input when a low level voltage equal to the maximum low level output voltage specified for the family is applied to the input. This test is used to check the input pullup resistor on an MET or a diode input and to guarantee the specified fan-in of the family.

I_T+ Current at Positive-Going Threshold Point: The current flowing out of a transition-operated (Schmitt trigger) input when a voltage equal to the positive going threshold voltage is applied to the input.

I_T- Current at Negative-Going Threshold Point: The current flowing out of a transition-operated (Schmitt trigger) input when a voltage equal to the negative going threshold voltage is applied to the input.

OUTPUT CURRENT PARAMETERS

I_{CEX} Output Leakage Current: The current flowing into an open collector output when input conditions have been applied that, according to the product specification, will cause the output to be in the logic high state. This test checks the reverse breakdown of the output transistor.

I_O(off) Off-State Output Current: The current flowing into an output with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state.

NOTE: This parameter is usually specified for open collector outputs intended to drive devices other than logic circuits, such as displays. Any leakage current applied to a display may cuase the display to be activated.

I_{OH} High Level Output Current: The current flowing out of an output with input conditions applied that, according to the product specification, will establish a logic high level at the output. This test guarantees the current sourcing (drive) capability of the output and the fan-out specified for the family.

I_{OL} Low Level Output Current: The current flowing into an output with input conditions applied that, according to the product specification, will establish a logic low level at the output. This test guarantees the current sinking capability of the output and the fan-out specified for the family.

I_{OS} Output Short-Circuit Current: The current out of an output when that output is shorted to ground, or another specified potential, with input conditions applied that, according to the product specification, will establish a logic high level at the output.

I_{OZ} High-Impedance State Output Current: These tests guarantee that the device will not excessively load a bus line when the device output is put into the TRI-STATE® mode.

I_{OZH} (or I_{SINK}): The current flowing into an output with input conditions applied to the output control pin such that the output is in the high impedance state and input conditions applied to the other inputs that, according to the product specification, will establish a logic low level at the output.

I_{OZL}(or I_{SOURCE}): The current flowing out of an output with input conditions applied to the output control pin such that the output is in the high impedance state and input conditions applied to the other inputs that, according to the product specification, will establish a logic high level at the output.

SUPPLY CURRENT PARAMETERS

I_{CCH} Supply Current (outputs in the high state): The current flowing into the V_{CC} terminal of a device with input conditions applied that, according to the product specification, will establish a logic high level at the output(s).

I_{CCL} Supply Current (outputs in the low state): The current flowing into the V_{CC} terminal of a device with input conditions applied that, according to the product specification, will establish a logic low level at the output(s).

DC Operating Conditions and Characteristics (Continued)

I_{CCZ} Supply Current (outputs in the high-impedance state): The current flowing into the V_{CC} terminal of a device with input conditions applied that, according to the product specification, will establish a high impedance state at the output.

INPUT VOLTAGE PARAMETERS

BV_{IN} Input Breakdown Voltage: The maximum voltage that the device is guaranteed to be able to withstand without exceeding the maximum input current specification.

V_F Input Forward Voltage: The voltage applied to the input of a device that causes the input structure to become forward biased; usually equal to the maximum output low voltage specified for the family.

V_{IH} High Level Input Voltage: The minimum positive voltage level that can be applied to an input terminal of a device and be recognized as a logic high level.

V_{IK} Input Clamp Voltage: The input clamp voltage specification checks the quality of the input diode whose purpose is to damp out ringing. This is not intended to be an operating condition and if this voltage is allowed to persist for any length of time, parasitic transistor action will occur between adjacent geometry tanks and circuit performance will be degraded, in some cases to the point of failure.

V_{IL} Low Level Input Voltage: The maximum positive voltage level that can be applied to an input terminal of a device and be recognized as a logic low level.

V_R Input Reverse Voltage: The voltage applied to an input of a device that causes the input structure to become reverse biased; usually equal to the minimum high level output voltage specified for the family.

V_{T+} Positive-Going Threshold Voltage: The voltage level at a transition-operated (Schmitt trigger) input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} Negative-Going Threshold Voltage: The voltage level at a transition-operated (Schmitt trigger) input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

OUTPUT VOLTAGE PARAMETERS

V_{OH} High Level Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

V_{OL} Low Level Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

$V_{O(off)}$ Off-State Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state.

NOTE: This characteristic is usually specified only for outputs without internal pull-up elements intended for driving devices other than logic circuits.

$V_{O(on)}$ On-State Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will cause the output switching element to be in the on state.

NOTE: This characteristic is usually specified only for outputs without internal pull-up elements intended for driving devices other than logic circuits.

AC Operating Conditions and Characteristics

INPUT PARAMETERS

f_{MAX} Maximum Clock Frequency: The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic levels at the output with input conditions established that should cause changes of output logic level in accordance with the specification. Unless otherwise specified, this test is performed with no restrictions on input rise and fall times or duty cycle.

NOTE: A minimum value is specified that is the highest frequency at which all devices are guaranteed to function correctly.

t_H Hold Time: The interval during which a signal must be maintained at a given data input after an active transition at another given input.

NOTE: A minimum value is specified that is the smallest time interval above which all devices are guaranteed to function correctly.

t_W Pulse Width: The time interval between specified voltage reference points on the leading and trailing edges of a pulse waveform.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.

t_{REC} Recovery Time: The time interval needed to switch a memory-type device from a write mode to a read mode and to obtain valid data signals at the output.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the device is guaranteed.

t_{REL} Release Time: The time interval between one control input going inactive and another input going active after which the inactive input no longer has any influence on the device operation.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.

t_S Set-Up Time: The time interval during which a stable signal must be maintained at a specified input terminal before an active transition at another specified input terminal.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.

t_R Rise Time: The time interval between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from a defined low level to a defined high level. Common defined levels are from 10% of the signal amplitude to 90% of the signal amplitude.

t_F Fall Time: The time interval between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from a defined high level to a defined low level. Common defined levels are from 90% of the signal amplitude to 10% of the signal amplitude.

OUTPUT PARAMETERS

t_{PZH} Output Enable Time to a High Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from a high impedance (off) state to the defined high state.

t_{PZL} Output Enable Time to a Low Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from a high impedance (off) state to the defined low state.

t_{PHZ} Output Disable Time from a High Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from the defined high state to the high impedance (off) state .

t_{PLZ} Output Disable Time from a Low Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from the defined low state to the high impedance (off) state .

t_{WOUT} Output Pulse Width: The time interval between specified voltage reference points on the leading and trailing edges of an output waveform.

NOTE: This is usually only specified for monostable elements.

t_{PLH} Propagation Time, Low to High: The time between the specified voltage reference points on the input and output waveforms with the output changing from a low logic level to a high logic level.

t_{PHL} Propagation Delay, High to Low: The time between the specified voltage reference points on the input and output waveforms with the output changing from a high logic level to a low logic level.

t_{TLH}, t_r Transition Time, or Rise Time: The time interval between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from a defined low level to a defined high level. Common defined levels are from 10% of the signal amplitude to 90% of the signal amplitude, or from 0.6V to 2.6V.

t_{THL}, t_f Transition Time, or Fall Time: The time interval between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from a defined high level to a defined low level. Common defined levels are from 90% of the signal amplitude to 10% of the signal amplitude, or from 2.6V to 0.6V.

Note A: All AC Specifications are for one output switching at a time.

EXPLANATION OF DEVICE FUNCTIONS

Circuit Complexity

SSI: Small Scale Integration; the lowest level of complexity in integrated circuits.

MSI: Medium Scale Integration; small subsystems integrated into a single microcircuit.

LSI: Large Scale Integration; large subsystems or small systems integrated into a single microcircuit.

FUNCTIONAL DESCRIPTIONS

Buffer: A logic gate with high output drive capability, or fanout. Buffers are used where a single circuit must drive a large number of loads.

Comparator: A logic circuit that will compare two separate input signals and produce an output based on that comparison. A simple comparator is the Exclusive-NOR gate, which produces a high level output only when its two inputs are identical.

Counter: A logic circuit that counts the number of input pulses it receives. Counters can be used for frequency division, counting, and sequencing digital operations. Common counter configurations are Binary, where the device counts from 0 to 15 and Decade, where the device counts from 0 to 9.

AC Operating Conditions and Characteristics (Continued)

Data Selector/Multiplexer: A logic circuit that will select one of several input signals and feed that signal onto a common bus line. It can be thought of as a multipole, multiposition switch with each switch pole representing one output and each switch position representing one input.

Decoder/Demultiplexer: A logic circuit that is the complement of the Data Selector/Multiplexer; that is, this circuit takes an input signal and feeds it to any one of several output lines depending on the information placed on its steering, or control, inputs.

Driver: Same as Buffer, above.

Flip-Flop: A logic circuit that is used to store information. A flip-flop is called "bistable" since it has two stable states.

Gate: The basic building block of all logic circuits; an element whose output is a Boolean function of its inputs. The basic functions are the AND, OR, and NOT. By combining these functions, NAND, NOR, and Exclusive-OR and Exclusive-NOR gates are built.

Latch: A bistable element that latches, or holds, data which is present at its input at the time the Enable input goes to its inactive state. When the Enable input is active, the data, present at the input, is passed directly to the output, similar to the operation of a gate.

One-Shot: Monostable multivibrator; a flip-flop that only has one stable state. When triggered by an input transient, it flips to its unstable state for a time period determined by an external R-C network connected to its timing inputs, and then returns to its stable state.

Shift Register: A series of flip-flops in which the data signal is shifted out of one flip-flop and into the succeeding flip-flop during an active transition on the clock input.

Transceiver: A logic circuit that can transmit data onto a bus line and receive data off of the bus line using the same terminal as an input and output. The direction of signal flow is determined by logic levels present at a Direction Control input.

OTHER TERMS

Asynchronous: A mode of operation that does not require any specific timing relationship between different control inputs.

Open Collector: Output configuration that has no internal pullup. This configuration enables outputs that are connected together (wired-OR) to assume opposite states without incurring damage.

Schmitt Trigger: An input configuration that has a different threshold point depending on whether the input signal is rising or falling. This is especially useful in electrically noisy environments.

Synchronous: A mode of operation where specific timing requirements must be met between control inputs before an indicated action can occur.

Totem Pole: An output configuration that contains an internal pullup structure, usually a transistor pullup allowing higher output drive capability than is available with open collector outputs.

TRI-STATE: A registered trademark for a circuit configuration in which the device can be switched 'off' during which time the output presents a very high impedance to the bus it is connected to. This allows multiple outputs to be connected to a bus line while only one output drives the line, the other outputs being switched into their high impedance states.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in the function tables found in NSC data sheets:

H = high logic level (steady state)
L = low logic level (steady state)
↑ = transition from low to high logic level
↓ = transition from high to low logic level
X = irrelevant (any level, including transitions)
Z = off (high impedance) state of a TRI-STATE output
a . . . h = the level of steady state inputs at inputs A through H respectively
Q_0 = the level of Q before the indicated steady state input conditions were established
$\overline{Q}_0$ = complement of Q_0 or level of Q before the indicated steady state input conditons were established
Q_n = level of Q before the most recent active transition indicated by ↑ or ↓
⎍ = one high level pulse
⊔ = one low level pulse
toggle = each output changes to the complement of its previous level on each active transition indicated by ↑ or ↓

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect on the output. If the output is shown as a pulse, ⎍ or ⊔, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. As an example, *Figure 1* is the function table for a 4-bit bidirectional universal shift register, similar to the DM54LS194.

The first line of the table represents "asynchronous" clearing of the register and indicates that if CLEAR is low, all four outputs will be reset low regardless of the states of the other inputs. In the succeeding lines, CLEAR is inactive (high) and consequently has no effect.

AC Operating Conditions and Characteristics (Continued)

The second line indicates that so long as the CLOCK input remains low (while CLEAR is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of CLEAR high and CLOCK low was established. Since on all the other lines of the table only the rising edge of the CLOCK is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the CLOCK remains high or on the high-to-low transition of the CLOCK.

The third line of the table represents "synchronous" parallel loading of the register and indicates that if S1 and S0 are both high, then regardless of the levels at the SERIAL inputs, the data present at A will transfer to QA, the data present at B will transfer to QB, and so forth, following a low-to-high transition on CLOCK.

The fourth and fifth lines represent the "synchronous" loading of high and low level data, respectively, from the SHIFT RIGHT SERIAL input and the shifting one bit to the right of previously entered data; data previously at QA is now at QB, data previously at QB and QC is now at QC and QD respectively, and the data previously at QD has been shifted out of the register. This entry of data and shifting takes place on the low-to-high level transition of CLOCK when S1 is low and S0 is high and as shown, the levels at the PARALLEL inputs, A through D, have no effect.

The sixth and seventh lines represent the "synchronous" loading of high and low level data respectively, from the SHIFT LEFT SERIAL input and the shifting one bit to the left of previously entered data; data previously at QD is now at QC, data previously at QC and QB is now at QB and QA respectively, and the data previously at QA has been shifted out of the register. This entry of serial data and shifting to the left takes place on the low-to-high level transition of CLOCK when S1 is high and S0 is low and as seen, the levels at the PARALLEL inputs, A through D, have no effect.

The last line indicates that so long as both MODE inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady state combination of CLEAR high and both MODE inputs low was established.

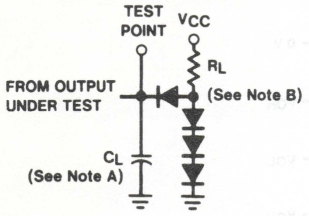
Clear	Inputs									Outputs			
	Mode		Clock	Serial		Parallel							
	S1	S0		Left	Right	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

FIGURE 1. Function Table

DM54/74, 54S/74S Test Waveforms

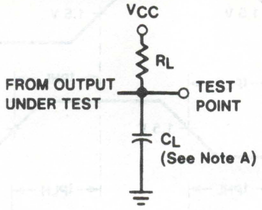
Parameter Measurement Information

Load Circuit for Bi-State Totem-Pole Outputs


TEST POINT
VCC
RL
FROM OUTPUT UNDER TEST
(See Note B)
CL
(See Note A)

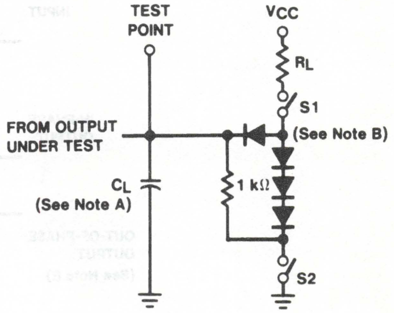
TL/X/0003-1

Load Circuit for Open-Collector Outputs


VCC
RL
FROM OUTPUT UNDER TEST
TEST POINT
CL
(See Note A)

TL/X/0003-2

Load Circuit for TRI-STATE® Outputs

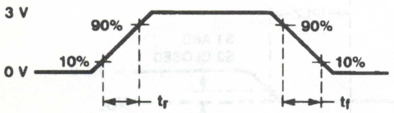

TEST POINT
VCC
RL
S1
(See Note B)
FROM OUTPUT UNDER TEST
1 kΩ
CL
(See Note A)
S2

TL/X/0003-3

Note A: C_L includes probe and jig capacitance.

Note B: All diodes are 1N916 or 1N3064.

Input Waveform


3 V
0 V
90%
10%
90%
10%
tr
tf

TL/X/0003-4

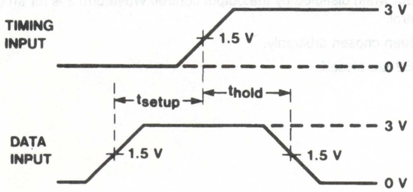
54/74 $t_r \le 7$ ns; $t_f \le 7$ ns

54S/74S $t_r \le 2.5$ ns, $t_f \le 2.5$ ns

Generator: $Z_{OUT} \approx 50\Omega$

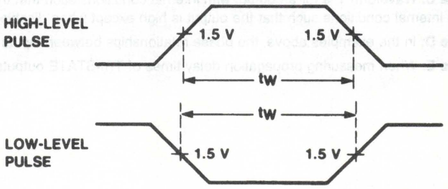
PRR ≤ 1 MHz

Voltage Waveforms Setup and Hold Times


TIMING INPUT
3 V
1.5 V
0 V
tsetup
thold
DATA INPUT
3 V
1.5 V
1.5 V
0 V

TL/X/0003-5

Voltage Waveforms Pulse Widths

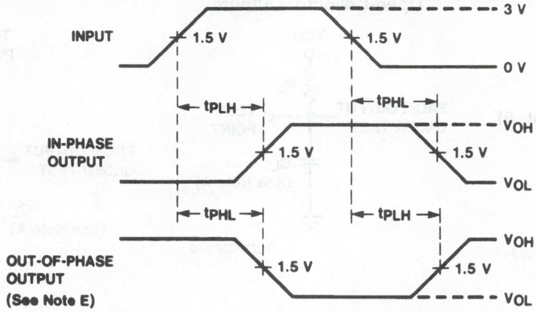

HIGH-LEVEL PULSE
1.5 V
1.5 V
tw
LOW-LEVEL PULSE
tw
1.5 V
1.5 V

TL/X/0003-6

DM54/74, 54S/74S Test Waveforms (Continued)

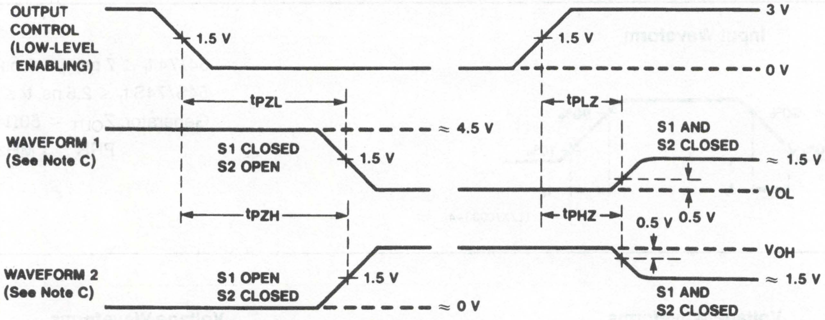
Parameter Measurement Information (Continued)

Voltage Waveforms Propagation Delay Times


INPUT
1.5 V
1.5 V
3 V
0 V
tPLH
tPHL
IN-PHASE OUTPUT
1.5 V
1.5 V
VOH
VOL
tPHL
tPLH
OUT-OF-PHASE OUTPUT (See Note E)
1.5 V
1.5 V
VOH
VOL

TL/X/0003-7

Voltage Waveforms Enable and Disable Times, TRI-STATE Outputs


OUTPUT CONTROL (LOW-LEVEL ENABLING)
1.5 V
1.5 V
3 V
0 V
tPZL
tPLZ
WAVEFORM 1 (See Note C)
≈ 4.5 V
S1 CLOSED S2 OPEN
1.5 V
S1 AND S2 CLOSED
≈ 1.5 V
VOL
tPZH
tPHZ
0.5 V
0.5 V
VOH
WAVEFORM 2 (See Note C)
S1 OPEN S2 CLOSED
1.5 V
≈ 0 V
≈ 1.5 V
S1 AND S2 CLOSED

TL/X/0003-8

Note C: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

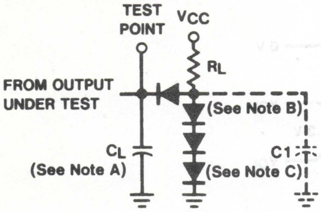
Note D: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Note E: When measuring propagation delay times of TRI-STATE outputs, switches S1 and S2 are closed.

DM54L/DM54LS/74LS Test Waveforms

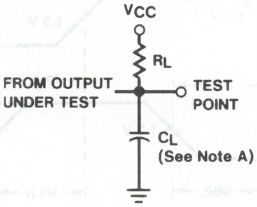
Parameter Measurement Information

Load Circuit for Bi-State Totem-Pole Outputs


TEST POINT
VCC
RL
FROM OUTPUT UNDER TEST
(See Note B)
CL
(See Note A)
C1
(See Note C)

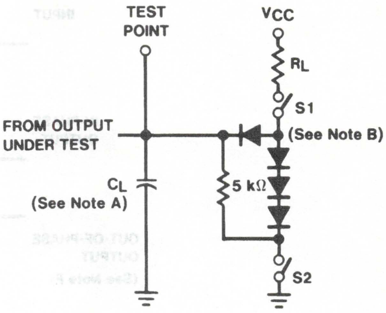
TL/X/0003-9

Load Circuit for Open-Collector Outputs


VCC
RL
FROM OUTPUT UNDER TEST
TEST POINT
CL
(See Note A)

TL/X/0003-10

TRI-STATE Outputs


TEST POINT
VCC
RL
S1
(See Note B)
FROM OUTPUT UNDER TEST
CL
(See Note A)
5 kΩ
S2

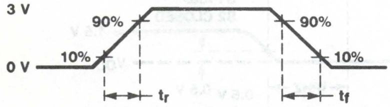
TL/X/0003-11

Note A: C_L includes probe and jig capacitance.

Note B: All diodes are 1N916 or 1N3064.

Note C: C1 (30 pF) is used for testing Series 54L/74L devices only.

Input Waveform


3 V
0 V
90%
10%
90%
10%
tr
tf

TL/X/0003-12

54LS/74LS: $t_r \le 6$ ns, $t_f \le 6$ ns

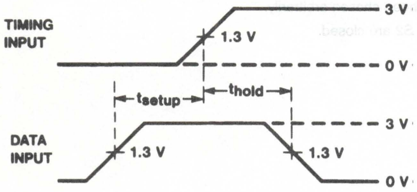
54L gates and inverters: $t_r \le 60$ ns, $t_f \le 60$ ns

54L flip-flops and MSI: $t_r \le 25$ ns, $t_f \le 25$ ns

Generator: $Z_{OUT} \approx 50\Omega$

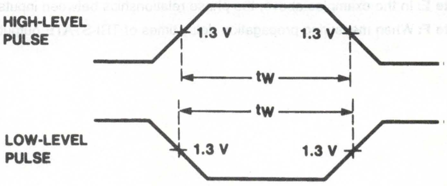
PRR $\le$ 1 MHz

Voltage Waveforms Setup and Hold Times

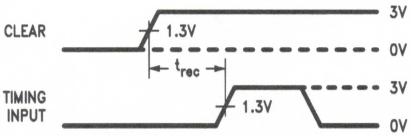

TIMING INPUT
3 V
1.3 V
0 V
tsetup
thold
DATA INPUT
3 V
1.3 V
1.3 V
0 V

TL/X/0003-13

Voltage Waveforms Pulse Widths


HIGH-LEVEL PULSE
1.3 V
1.3 V
tw
tw
LOW-LEVEL PULSE
1.3 V
1.3 V

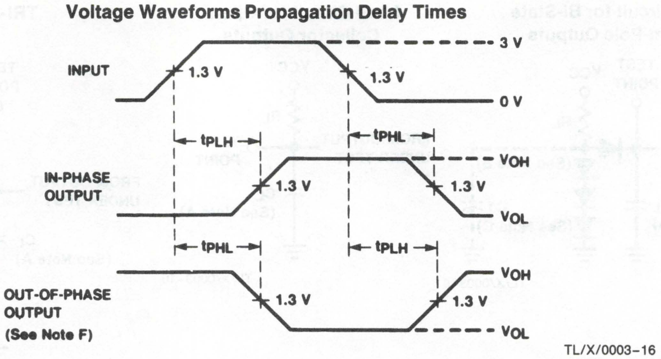
TL/X/0003-14


CLEAR
1.3V
3V
0V
trec
TIMING INPUT
1.3V
3V
0V

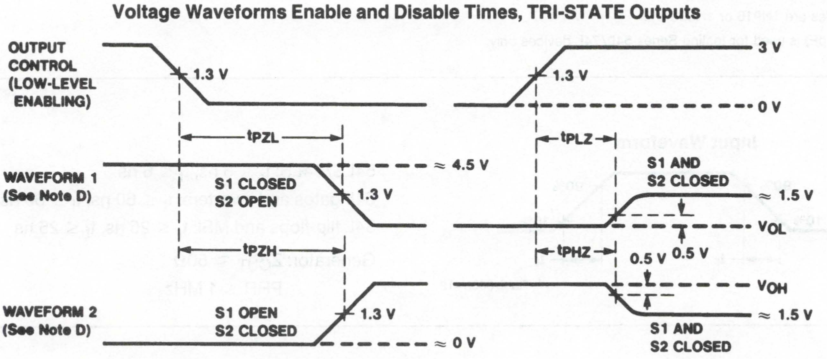
TL/X/0003-15

DM54L/DM54LS/74LS Test Waveforms (Continued)

Parameter Measurement Information (Continued)


Voltage Waveforms Propagation Delay Times
INPUT
1.3 V
1.3 V
3 V
0 V
tPLH
tPHL
IN-PHASE OUTPUT
1.3 V
1.3 V
VOH
VOL
tPHL
tPLH
OUT-OF-PHASE OUTPUT (See Note F)
1.3 V
1.3 V
VOH
VOL

TL/X/0003-16


Voltage Waveforms Enable and Disable Times, TRI-STATE Outputs
OUTPUT CONTROL (LOW-LEVEL ENABLING)
1.3 V
1.3 V
3 V
0 V
tPZL
tPLZ
WAVEFORM 1 (See Note D)
≈ 4.5 V
S1 CLOSED S2 OPEN
1.3 V
S1 AND S2 CLOSED
≈ 1.5 V
VOL
tPZH
tPHZ
0.5 V
0.5 V
VOH
WAVEFORM 2 (See Note D)
S1 OPEN S2 CLOSED
1.3 V
≈ 0 V
≈ 1.5 V
S1 AND S2 CLOSED

TL/X/0003-17

Note D: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Note E: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Note F: When measuring propagation delay times of TRI-STATE outputs, switches S1 and S2 are closed.

Section 2
Low Power Schottky

Section 2—Low Power Schottky

Low Power Schottky—Commercial Products

DM74LS00 Quad 2-Input NAND Gate ... 2-3
DM74LS02 Quad 2-Input NOR Gate ... 2-5
DM74LS03 Quad 2-Input NAND Gate with Open-Collector Outputs ... 2-7
DM74LS04 Hex Inverter ... 2-9
DM74LS05 Hex Inverter with Open-Collector Outputs ... 2-11
DM74LS08 Quad 2-Input AND Gate ... 2-13
DM74LS09 Quad 2-Input AND Gate with Open-Collector Outputs ... 2-15
DM74LS10 Triple 3-Input NAND Gate ... 2-17
DM74LS11 Triple 3-Input AND Gate ... 2-19
DM74LS12 Triple 3-Input NAND Gate with Open-Collector Outputs ... 2-21
DM74LS13 Dual 4-Input Schmitt Trigger ... 2-23
DM74LS14 Hex Inverter with Schmitt Trigger Inputs ... 2-26
DM74LS15 Triple 3-Input AND Gate with Open-Collector Outputs ... 2-29
DM74LS20 Dual 4-Input NAND Gate ... 2-32
DM74LS21 Dual 4-Input AND Gate ... 2-34
DM74LS22 Dual 4-Input NAND Gate with Open-Collector Outputs ... 2-36
DM74LS26 Quad 2-Input NAND Buffers with High-Voltage Open-Collector Outputs ... 2-39
DM74LS27 Triple 3-Input NOR Gate ... 2-41
DM74LS28 Quad 2-Input NOR Buffer ... 2-43
DM74LS30 8-Input NAND Gate ... 2-46
DM74LS32 Quad 2-Input OR Gate ... 2-48
DM74LS33 Quad 2-Input NOR Buffer with Open-Collector Outputs ... 2-50
DM74LS37 Quad 2-Input NAND Buffer ... 2-52
DM74LS38 Quad 2-Input NAND Buffer with Open-Collector Outputs ... 2-54
DM74LS40 Dual 4-Input NAND Buffer ... 2-56
DM74LS42 BCD to Decimal Decoder ... 2-59
DM74LS47 BCD to 7-Segment Decoder/Driver ... 2-62
DM74LS48 BCD to 7-Segment Decoder ... 2-67
DM74LS51 Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-INVERT Gate ... 2-74
DM74LS54 4-Wide 2-Input AND-OR-INVERT Gate ... 2-77
DM74LS55 2-Wide 4-Input AND-OR-INVERT Gate ... 2-79
DM74LS73A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs ... 2-81
DM74LS74A Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear, and Complementary Outputs ... 2-84
DM74LS75 Quad Latch ... 2-87
DM74LS83A 4-Bit Binary Adder with Fast Carry ... 2-90
DM74LS85 4-Bit Magnitude Comparator ... 2-94
DM74LS86 Quad 2-Input EXCLUSIVE-OR Gate ... 2-98
DM74LS90 Decade Counter ... 2-101
DM74LS93 4-Bit Binary Counter ... 2-101
DM74LS95B 4-Bit Right/Left Shift Register ... 2-108
DM74LS107A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flop with Clear and Complementary Outputs ... 2-113
DM74LS109A Dual Positive-Edge-Triggered J-$\overline{K}$ Flip-Flop with Preset, Clear, and Complementary Outputs ... 2-116

Section 2—Low Power Schottky (Continued)

Low Power Schottky—Commercial Products (Continued)

DM74LS112A Dual Negative-Edge-Triggered J-K Flip-Flop with Preset, Clear, and Complementary Outputs 2-119
DM74LS122 Retriggerable Monostable Multivibrator (One-Shot) with Clear and Complementary Outputs 2-129
DM74LS123 Dual Retriggerable Monostable Multivibrator (One-Shot) with Clear and Complementary Outputs 2-133
DM74LS125A Quad TRI-STATE Buffer 2-137
DM74LS126A Quad TRI-STATE Buffer 2-140
DM74LS132 Quad 2-Input Schmitt Trigger NAND Gate 2-143
DM74LS133 13-Input NAND Gate 2-146
DM74LS136 Quad 2-Input EXCLUSIVE-OR Gate with Open-Collector Outputs 2-148
DM74LS138 3-to-8 Line Decoder/Demultiplexer 2-150
DM74LS139 Dual 2-to-4 Line Decoder/Demultiplexer 2-150
DM74LS151 1-of-8 Line Data Selector/Multiplexer with Complementary Outputs 2-155
DM74LS153 Dual 1-of-4 Line Data Selectors/Multiplexers 2-161
DM74LS154 4-to-16 Line Decoder/Demultiplexer 2-164
DM74LS155 Dual 2-to-4 Line Decoder/1-to-4 Line Demultiplexer 2-167
DM74LS156 Dual 2-to-4 Line Decoder/1-to-4 Line Demultiplexer with Open-Collector Outputs 2-167
DM74LS157 Quad 2-to-1 Line Data Selector/Multiplexer 2-171
DM74LS158 Quad 2-to-1 Line Inverting Data Selector/Multiplexer 2-171
DM74LS160A Synchronous Presettable BCD Decade Counter 2-175
DM74LS161A Synchronous 4-Bit Binary Counter with Asynchronous Clear 2-180
DM74LS162A Synchronous Presettable BCD Decade Counter 2-175
DM74LS163A Synchronous 4-Bit Binary Counter with Synchronous Clear 2-180
DM74LS164 8-Bit Serial In/Parallel Out Shift Register with Asynchronous Clear 2-188
DM74LS165 8-Bit Parallel In/Serial Out Shift Register with Complementary Outputs 2-191
DM74LS166 8-Bit Parallel or Serial In/Serial Out Shift Register 2-195
DM74LS169A Synchronous 4-Bit Up/Down Binary Counter 2-203
DM74LS170 4-by-4 Register File with Open-Collector Outputs 2-208
DM74LS173A 4-Bit TRI-STATE D Register 2-212
DM74LS174 Hex D Flip-Flop with Clear 2-216
DM74LS175 Quad D Flip-Flop with Clear and Complementary Outputs 2-216
DM74LS181 4-Bit Arithmetic Logic Unit 2-221
DM74LS190 Synchronous BCD Up/Down Decade Counter with Mode Control 2-228
DM74LS191 Synchronous 4-Bit Up/Down Binary Counter with Mode Control 2-228
DM74LS192 Up/Down Decade Counter with Separate Up/Down Clocks 2-234
DM74LS193 Synchronous 4-Bit Up/Down Binary Counter with Dual Clock 2-238
DM74LS194A 4-Bit Bidirectional Universal Shift Register 2-243
DM74LS195A 4-Bit Parallel Access Shift Register 2-247
DM74LS196 Presettable Decade Counter 2-251
DM74LS197 Presettable Binary Counter 2-255
DM74LS221 Dual Monostable Multivibrator (One-Shot) with Schmitt Trigger Input 2-259
DM74LS240 Octal TRI-STATE Inverting Buffer/Line Driver/Line Receiver 2-264
DM74LS241 Octal TRI-STATE Buffer/Line Driver/Line Receiver 2-264
DM74LS243 Quadruple Bus Transceiver 2-267
DM74LS244 Octal TRI-STATE Buffer/Line Driver/Line Receiver 2-270
DM74LS245 Octal TRI-STATE Bus Transceiver 2-273
DM74LS247 BCD to 7-Segment Decoder/Driver with Open-Collector Outputs 2-276
DM74LS248 BCD to 7-Segment Decoder with 2 kΩ Pull-Up Resistors 2-279
DM74LS249 BCD to 7-Segment Decoder with Open-Collector Outputs 2-282
DM74LS251 TRI-STATE 1-of-8 Line Data Selector/Multiplexer with Complementary Outputs 2-286

Section 2—Low Power Schottky (Continued)

Low Power Schottky—Commercial Products (Continued)

DM74LS253 Dual TRI-STATE 1-of-4 Line Data Selector/Multiplexer ... 2-289
DM74LS256 Dual 4-Bit Addressable Latch ... 2-292
DM74LS257B Quad TRI-STATE 2-to-1 Line Data Selector/Multiplexer ... 2-296
DM74LS258B Quad TRI-STATE 2-to-1 Line Inverting Data Selector/Multiplexer ... 2-296
DM74LS259 8-Bit Serial In to Parallel Out Addressable Latch ... 2-301
DM74LS260 Dual 5-Input NOR Gate ... 2-304
DM74LS266 Quad 2-Input EXCLUSIVE-NOR Gate with Open-Collector Outputs ... 2-306
DM74LS273 8-Bit Register with Clear ... 2-308
DM74LS279 Quad $\overline{S}$-$\overline{R}$ Latch ... 2-311
DM74LS283 4-Bit Binary Adder with Fast Carry ... 2-314
DM74LS290 Decade Counter ... 2-318
DM74LS293 4-Bit Binary Counter ... 2-322
DM74LS295A 4-Bit Shift Register with TRI-STATE Outputs ... 2-326
DM74LS298 Quad 2-Port Register (Multiplexer with Storage) ... 2-330
DM74LS299 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins ... 2-333
DM74LS322 8-Bit Serial/Parallel Register with Sign Extend ... 2-338
DM74LS323 8-Bit Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins ... 2-343
DM74LS347 BCD to 7-Segment Decoder/Driver ... 2-348
DM74LS352 Dual 1-of-4 Line Inverting Data Selector/Multiplexer ... 2-350
DM74LS353 Dual 4-Input Multiplexer with TRI-STATE Outputs ... 2-353
DM74LS365A Hex TRI-STATE Buffer/Bus Driver ... 2-357
DM74LS366A Hex TRI-STATE Inverting Buffer/Bus Driver ... 2-360
DM74LS367A Hex TRI-STATE Buffer/Bus Driver ... 2-363
DM74LS368A Hex TRI-STATE Inverting Buffer/Bus Driver ... 2-366
DM74LS373 Octal TRI-STATE Transparent D Latch ... 2-369
DM74LS374 Octal TRI-STATE Positive Edge-Triggered D Flip-Flop ... 2-369
DM74LS375 4-Bit Latch ... 2-374
DM74LS377 Octal D Flip-Flop with Common Enable and Clock ... 2-377
DM74LS378 Parallel D Register with Enable ... 2-380
DM74LS379 Quad Parallel Register with Enable ... 2-384
DM74LS380 Multifunction Octal Register ... 2-387
DM74LS380A Multifunction Octal Register ... 2-390
DM74LS390 Dual Decade (Bi-Quinary) Counter ... 2-394
DM74LS393 Dual 4-Bit Binary Counter ... 2-398
DM74LS395 4-Bit Shift Register with TRI-STATE Outputs ... 2-401
DM74LS447 BCD to 7-Segment Decoder/Driver ... 2-404
DM74LS450 16:1 Multiplexer ... 2-407
DM74LS450A 16:1 Multiplexer ... 2-410
DM74LS451 Dual 8:1 Multiplexer ... 2-414
DM74LS451A Dual 8:1 Multiplexer ... 2-417
DM74LS453 Quad 4:1 Multiplexer ... 2-421
DM74LS453A Quad 4:1 Multiplexer ... 2-424
DM74LS460 10-Bit Comparator ... 2-428
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DM74LS461 Octal Counter ... 2-435
DM74LS461A Octal Counter ... 2-438
DM74LS465 (DM71/81LS95A) Octal TRI-STATE Buffer/Bus Driver ... 2-442
DM74LS466 (DM71/81LS96A) Octal TRI-STATE Inverting Buffer/Bus Driver ... 2-442
DM74LS467 (DM71/81LS97A) Octal TRI-STATE Buffer/Bus Driver ... 2-442
DM74LS468 (DM71/81LS98A) Octal TRI-STATE Inverting Buffer/Bus Driver ... 2-442
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Section 2—Low Power Schottky (Continued)

Low Power Schottky—Commercial Products (Continued)

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DM74LS490 Dual Decade Counter 2-453
DM74LS491 10-Bit Counter 2-456
DM74LS491A 10-Bit Counter 2-459
DM74LS498 Octal Shift Register 2-463
DM74LS498A Octal Shift Register 2-466
DM74LS502 8-Bit Successive Approximation Register 2-470
DM74LS503 8-Bit Successive Approximation Register with Expansion Control 2-474
DM74LS533 Octal Transparent Latch with TRI-STATE Outputs 2-477
DM74LS534 Octal D Flip-Flop with TRI-STATE Outputs 2-480
DM74LS540 Octal Buffer/Line Driver with TRI-STATE Outputs 2-483
DM74LS563 Octal D Latch with TRI-STATE Outputs 2-486
DM74LS564 Octal D Flip-Flop with TRI-STATE Outputs 2-489
DM74LS573 Octal D Latch with TRI-STATE Outputs 2-492
DM74LS574 Octal D Flip-Flop with TRI-STATE Outputs 2-495
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DM74LS670 TRI-STATE 4-by-4 Register File 2-501
DM74LS952 Dual TRI-STATE 8-Bit Positive Edge-Triggered Rank Shift Register 2-505
DM74LS962 Dual TRI-STATE 8-Bit Positive Edge-Triggered Rank Shift Register 2-511
DM96LS02 Dual Retriggerable Resettable Monostable Multivibrator (One-Shot) 2-517

Low Power Schottky—MIL/Aero Products

54LS00/DM54LS00 Quad 2-Input NAND Gate 2-3
54LS02/DM54LS02 Quad 2-Input NOR Gate 2-5
54LS03/DM54LS03 Quad 2-Input NAND Gate with Open-Collector Outputs 2-7
54LS04/DM54LS04 Hex Inverter 2-9
54LS05/DM54LS05 Hex Inverter with Open-Collector Outputs 2-11
54LS08/DM54LS08 Quad 2-Input AND Gate 2-13
54LS09/DM54LS09 Quad 2-Input AND Gate with Open-Collector Outputs 2-15
54LS10/DM54LS10 Triple 3-Input NAND Gate 2-17
54LS11/DM54LS11 Triple 3-Input AND Gate 2-19
DM54LS12 Triple 3-Input NAND Gate with Open-Collector Outputs 2-21
54LS13 Dual 4-Input Schmitt Trigger 2-23
54LS14 Hex Inverter with Schmitt Trigger Inputs 2-26
54LS15 Triple 3-Input AND Gate with Open-Collector Outputs 2-29
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54LS21/DM54LS21 Dual 4-Input AND Gate 2-34
54LS22 Dual 4-Input NAND Gate with Open-Collector Outputs 2-36
54LS26 Quad 2-Input NAND Buffers with High-Voltage Open-Collector Outputs 2-39
54LS27/DM54LS27 Triple 3-Input NOR Gate 2-41
54LS28 Quad 2-Input NOR Buffer 2-43
54LS30/DM54LS30 8-Input NAND Gate 2-46
54LS32/DM54LS32 Quad 2-Input OR Gate 2-48
54LS33 Quad 2-Input NOR Buffer with Open-Collector Outputs 2-50
54LS37 Quad 2-Input NAND Buffer 2-52
54LS38/DM54LS38 Quad 2-Input NAND Buffer with Open-Collector Outputs 2-54
54LS40 Dual 4-Input NAND Buffer 2-56
54LS42/DM54LS42 BCD to Decimal Decoder 2-59
54LS47 BCD to 7-Segment Decoder/Driver 2-62
54LS48 BCD to 7-Segment Decoder 2-67
54LS49 BCD to 7-Segment Decoder with Open-Collector Outputs 2-71
54LS51 Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-INVERT Gate 2-74
54LS54 4-Wide 2-Input AND-OR-INVERT Gate 2-77

Section 2—Low Power Schottky (Continued)

Low Power Schottky—MIL/Aero Products (Continued)

54LS55 2-Wide 4-Input AND-OR-INVERT Gate 2-79
DM54LS73A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs 2-81
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DM54LS75 Quad Latch 2-87
54LS83A/DM54LS83A 4-Bit Binary Adder with Fast Carry 2-90
54LS85/DM54LS85 4-Bit Magnitude Comparator 2-94
DM54LS86 Quad 2-Input EXCLUSIVE-OR Gate 2-98
54LS95B 4-Bit Right/Left Shift Register 2-108
DM54LS107A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flop with Clear and Complementary Outputs 2-113
54LS109/DM54LS109A Dual Positive-Edge-Triggered J-$\overline{K}$ Flip-Flop with Preset, Clear, and Complementary Outputs 2-116
54LS112/DM54LS112A Dual Negative-Edge-Triggered J-K Flip-Flop with Preset, Clear, and Complementary Outputs 2-119
54LS113 Dual Positive-Edge-Triggered J-K Flip-Flop with Preset and Complementary Outputs 2-122
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DM54LS132 Quad 2-Input Schmitt Trigger NAND Gate 2-143
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54LS139/DM54LS139 Dual 2-to-4 Line Decoder/Demultiplexer 2-150
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54LS161A/DM54LS161A Synchronous 4-Bit Binary Counter with Asynchronous Clear 2-180
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54LS163A/DM54LS163A Synchronous 4-Bit Binary Counter with Synchronous Clear 2-180
54LS164/DM54LS164 8-Bit Serial In/Parallel Out Shift Register with Asynchronous Clear 2-188
54LS165 8-Bit Parallel In/Serial Out Shift Register with Complementary Outputs 2-191
54LS168 Synchronous Bi-Directional BCD Decade Counter 2-199
54LS169/DM54LS169A Synchronous 4-Bit Up/Down Binary Counter 2-203
54LS170 4-by-4 Register File with Open-Collector Outputs 2-208
54LS173 4-Bit TRI-STATE D Register 2-212
54LS174/DM54LS174 Hex D Flip-Flop with Clear 2-216
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Low Power Schottky—MIL/Aero Products (Continued)

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National Semiconductor

54LS00/DM54LS00/DM74LS00 Quad 2-Input NAND Gates

General Description

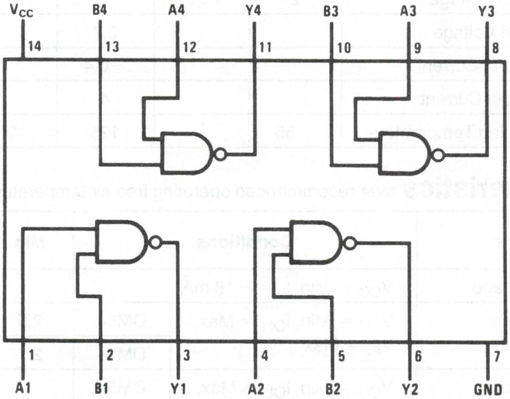
This device contains four independent gates each of which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (54LS00) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6439–1

Order Number 54LS00DMQB, 54LS00FMQB, 54LS00LMQB, DM54LS00J, DM54LS00W, DM74LS00M or DM74LS00N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS00			DM74LS00			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.4	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

54LS02/DM54LS02/DM74LS02
Quad 2-Input NOR Gates

General Description

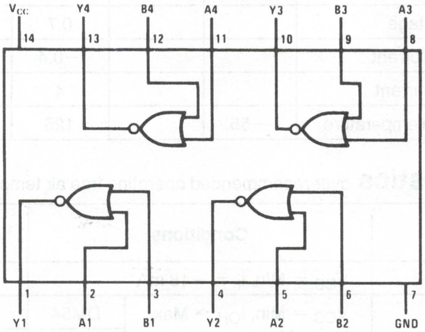
This device contains four independent gates each of which performs the logic NOR function.

Features

- Alternate Military/Aerospace device (54LS02) is available. Contact a National Semiconductor Sales Office/Distributor for specifications

Connection Diagram

Dual-In-Line Package



TL/F/6441–1

Order Number 54LS02DMQB, 54LS02FMQB, 54LS02LMQB, DM54LS02J, DM54LS02W, DM74LS02M or DM74LS02N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS02			DM74LS02			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.40	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.6	3.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.8	5.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		13		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		10		15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

54LS03/DM54LS03/DM74LS03 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Features

- Alternate Military/Aerospace device (54LS03) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

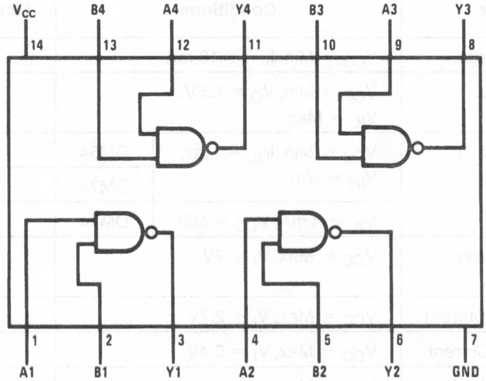
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6344–1

Order Number 54LS03DMQB, 54LS03FMQB, 54LS03LMQB, DM54LS03J, DM54LS03W, DM74LS03M or DM74LS03N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS03			DM74LS03			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.4	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	6	20	20	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	15	4	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

54LS04/DM54LS04/DM74LS04 Hex Inverting Gates

General Description

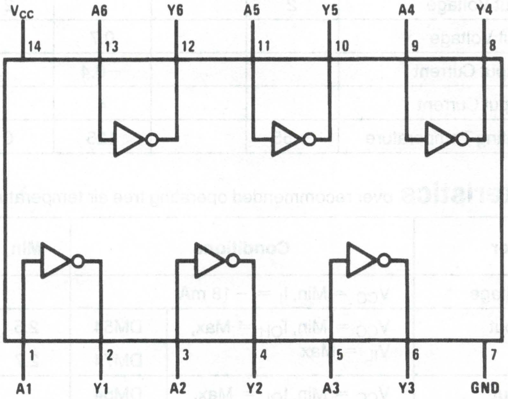
This device contains six independent gates each of which performs the logic INVERT function.

Features

- Alternate Military/Aerospace device (54LS04) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6345–1

Order Number 54LS04DMQB, 54LS04FMQB, 54LS04LMQB, DM54LS04J, DM54LS04W, DM74LS04M or DM74LS04N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS04			DM74LS04			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.2	2.4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3.6	6.6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 2\ k\Omega$				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

54LS05/DM54LS05/DM74LS05 Hex Inverters with Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Features

- Alternate Military/Aerospace device (54LS05) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

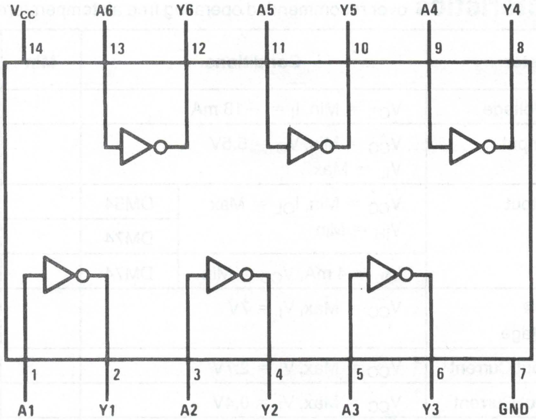
Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6346-1

Order Number 54LS05DMQB, 54LS05FMQB, DM54LS05J, DM54LS05W, DM74LS05M or DM74LS05N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS05			DM74LS05			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.2	2.4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3.6	6.6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	6	20	20	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	15	4	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

54LS08/DM54LS08/DM74LS08 Quad 2-Input AND Gates

General Description

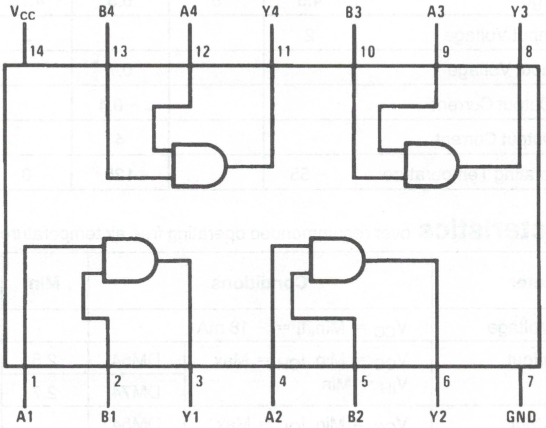
This device contains four independent gates each of which performs the logic AND function.

Features

- Alternate Military/Aerospace device (54LS08) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6347–1

Order Number 54LS08DMQB, 54LS08FMQB, 54LS08LMQB, DM54LS08J, DM54LS08W, DM74LS08M or DM74LS08N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = AB$

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS08			DM74LS08			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			2.4	4.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			4.4	8.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 2\ k\Omega$				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	5	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

54LS09/DM54LS09/DM74LS09
Quad 2-Input AND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Features

- Alternate Military/Aerospace device (54LS09) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

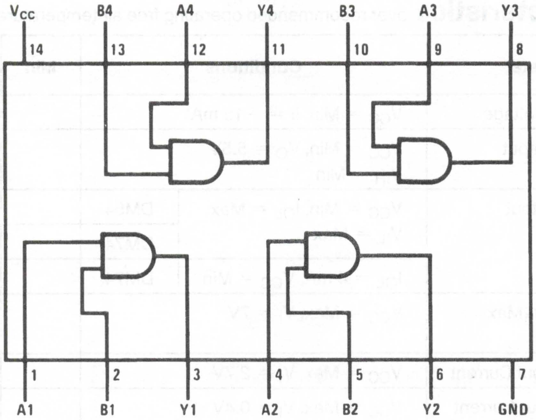
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6348-1

Order Number 54LS09DMQB, 54LS09FMQB, DM54LS09J, DM54LS09W, DM74LS09M or DM74LS09N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Y = AB

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS09			DM74LS09			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IH} = Min				100	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			2.4	4.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			4.4	8.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	5	20	8	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	4	15	6	27	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

54LS10/DM54LS10/DM74LS10
Triple 3-Input NAND Gates

General Description

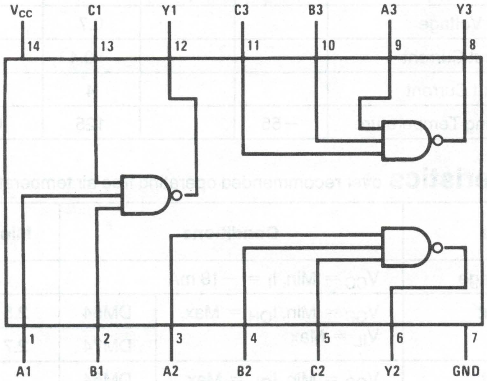
This device contains three independent gates each of which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (54LS10) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6349–1

Order Number 54LS10DMQB, 54LS10FMQB, 54LS10LMQB, DM54LS10J, DM54LS10W, DM74LS10M or DM74LS10N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{ABC}$

Inputs			Output
A	**B**	**C**	**Y**
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS10			DM74LS10			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.6	1.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.8	3.3	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

54LS11/DM54LS11/DM74LS11 Triple 3-Input AND Gates

General Description

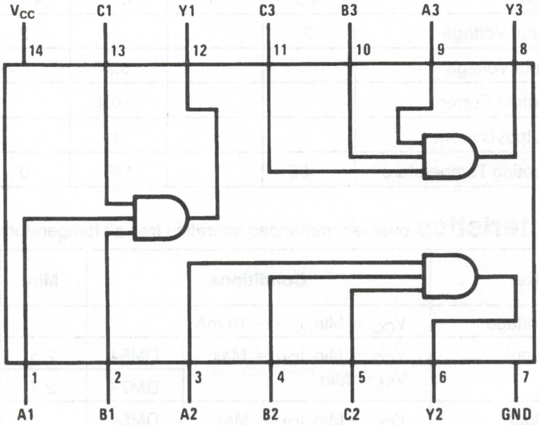
This device contains three independent gates each of which performs the logic AND function.

Features

- Alternate military/aerospace device (54LS11) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6350–1

Order Number 54LS11DMQB, 54LS11FMQB, 54LS11LMQB, DM54LS11J, DM54LS11W, DM74LS11M or DM74LS11N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Y = ABC

Inputs			Output
A	**B**	**C**	**Y**
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS11			DM74LS11			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.8	3.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3.3	6.6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	5	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54LS12/DM74LS12 Triple 3-Input NAND Gates with Open-Collector Outputs

General Description

This device contains three independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

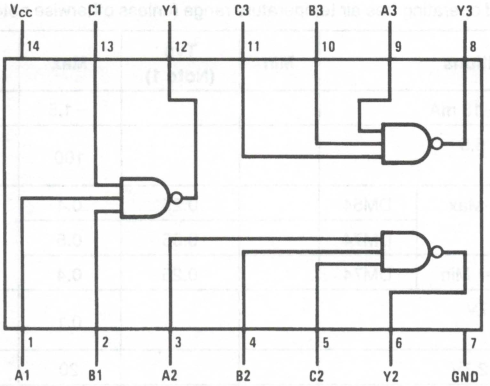
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6351–1

Order Number DM54LS12J, DM54LS12W, DM74LS12M or DM74LS12N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS12			DM74LS12			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5 V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.7	1.4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.8	3.3	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	6	20	20	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	15	4	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

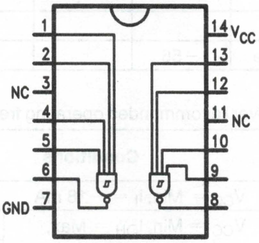
54LS13/DM74LS13
Dual 4-Input Schmitt Trigger

General Description

This device contains two independent gates each of which perform the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing jitter free output.

Connection Diagram

Dual-In-Line Package



TL/F/10166–1

Order Number 54LS13DMQB, 54LS13FMQB, 54LS13LMQB, DM74LS13M or DM74LS13N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 7V

Input Voltage 7V

Operating Free Air Temperature Range
54LS −55°C to +125°C
DM74LS 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS13			DM74LS13			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max V_{IN} = GND				6.0	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max V_{IN} = OPEN				7.0	mA
V_{T+}	Positive-Going Threshold Voltage	V_{CC} = +5.0V		1.5		2.0	V
V_{T-}	Negative-Going Threshold Voltage	V_{CC} = +5.0V		0.6		1.1	V
$V_{T+} - V_{T-}$	Hysteresis Voltage	V_{CC} = +5.0V		0.4			V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = +5.0V, V_{IN} = V_{T+}		−0.14*			mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = +5.0V, V_{IN} = V_{T-}		−0.18*			mA

*Typical Value

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 15\ pF$				Units
		54LS		DM74		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		22		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		27		30	ns

National Semiconductor

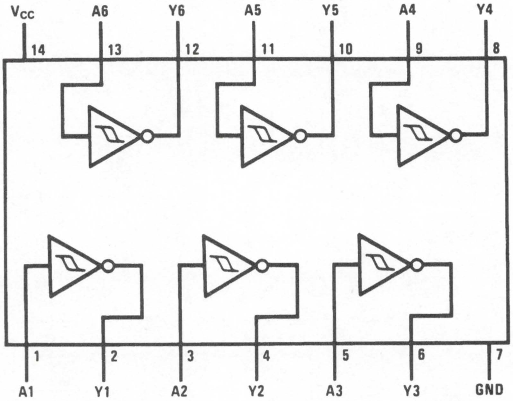
54LS14/DM74LS14 Hex Inverters with Schmitt Trigger Inputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Connection Diagram

Dual-In-Line Package



TL/F/6353-1

Order Number 54LS14DMQB, 54LS14FMQB, 54LS14LMQB, DM74LS14M or DM74LS14N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	**Y**
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS14			DM74LS14			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.5	1.6	2.0	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.6	0.8	1.1	0.5	0.8	1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	54LS	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS		0.25	0.4	V
			DM74		0.35	0.5	
		V_{CC} = Min, I_{OL} = 4 mA	DM74		0.25	0.4	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, $V_I = V_{T+}$	DM74		−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, $V_I = V_{T-}$	DM74		−0.18		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_{CC} = Max, V_I = 10.0V	54LS				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			8.6	16	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			12	21	mA

Note 1: V_{CC} = 5V.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 2\ k\Omega$				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	5	22	8	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	5	22	10	33	ns

National Semiconductor

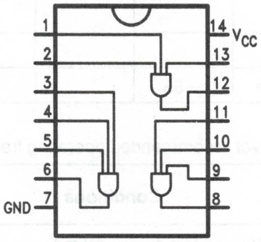
54LS15/DM74LS15 Triple 3-Input AND Gate with Open-Collector Outputs

General Description

This device contains three independent gates, each of which perform the logic AND function. The outputs are open-collector.

Connection Diagram

Dual-In-Line Package



TL/F/10167–1

Order Number 54LS15DMQB, 54LS15FMQB,
DM74LS15M or DM74LS15N
See NS Package Number J14A, M14A, N14A or W14B

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions at V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	54LS15			DM74LS15			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OH}	High Level Output Current	V_{CC} = Max, V_O = 5.5V				100	μA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max, V_{IN} = OPEN				3.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{IN} = GND				6.6	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	$R_L = 2\ k\Omega$ $C_L = 15\ pF$		Units
		Max		
		54LS	DM74	
t_{PLH}	Propagation Delay Time Low to High Level Output	24	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	18	14	ns

National Semiconductor

54LS20/DM54LS20/DM74LS20 Dual 4-Input NAND Gates

General Description

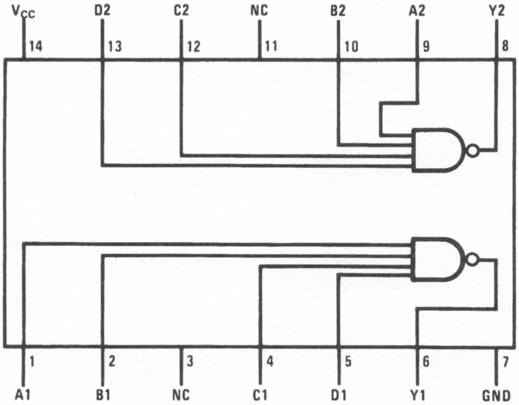
This device contains two independent gates each of which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (54LS20) is available. Contact a National Semiconductor Sales Office/Distributor for specifications

Connection Diagram

Dual-In-Line Package



TL/F/6355-1

Order Number 54LS20DMQB, 54LS20FMQB, 54LS20LMQB, DM54LS20J, DM54LS20W, DM74LS20M or DM74LS20N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 7V

Input Voltage 7V

Operating Free Air Temperature Range

DM54LS and 54LS −55°C to +125°C

DM74LS 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS20			DM74LS20			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.4	0.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.2	2.2	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

54LS21/DM54LS21/DM74LS21 Dual 4-Input AND Gates

General Description

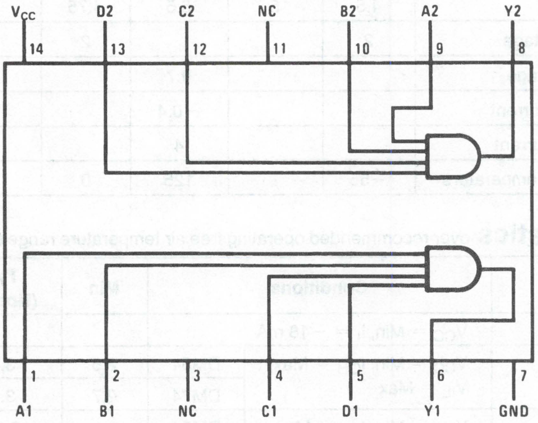
This device contains two independent gates each of which performs the logic AND function.

Features

- Alternate Military/Aerospace device (54LS21) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6356-1

Order Number 54LS21DMQB, 54LS21FMQB, 54LS21LMQB, DM54LS21J, DM54LS21W, DM74LS21M or DM74LS21N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = ABCD$

Inputs				Output
A	**B**	**C**	**D**	**Y**
X	X	X	L	L
X	X	L	X	L
X	L	X	X	L
L	X	X	X	L
H	H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS21			DM74LS21			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.2	2.4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.2	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 2\ k\Omega$				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	5	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

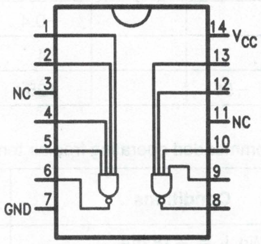
54LS22/DM74LS22 Dual 4-Input NAND Gate (with Open-Collector Output)

General Description

The 'LS22 contains two independent NAND gates, each with four data inputs.

Connection Diagram

Dual-In-Line Package



TL/F/10168-1

Order Number 54LS22DMQB, 54LS22FMQB, DM74LS22M or DM74LS22N
See NS Package Number J14A, M14A, N14A or W14B

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS22			DM74LS22			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{CCH}	Supply Current Outputs High	V_{CC} = Max, V_{IN} = GND				0.8	mA
I_{CCL}	Supply Current Outputs Low	V_{CC} = Max, V_{IN} = Open				2.2	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics

at $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 15\ pF$		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		24	ns

National Semiconductor

54LS26/DM74LS26 Quad 2-Input NAND Gates with High Voltage Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

These gates feature high-voltage output ratings (up to 15V) for interfacing with 12V systems. Although the outputs are rated for 15V, the device supply is still rated for 5V.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

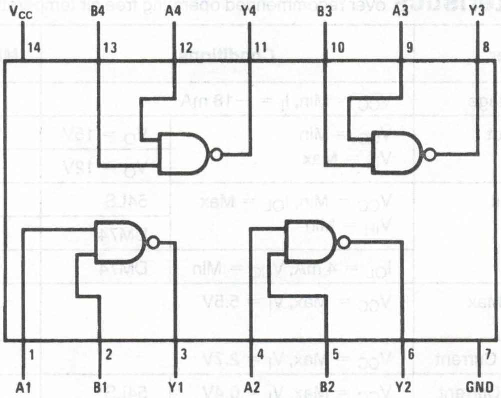
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6358-1

Order Number 54LS26DMQB, 54LS26FMQB, DM74LS26M or DM74LS26N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	15V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS26			DM74LS26			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min V_{IL} = Max	V_O = 15V			1000	μA
			V_O = 12V			50	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	54LS			−0.40	mA
			DM74			−0.36	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.4	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Max		
		54LS	DM74	
t_{PLH}	Propagation Delay Time Low to High Level Output	27	32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	18	28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

54LS27/DM54LS27/DM74LS27 Triple 3-Input NOR Gates

General Description

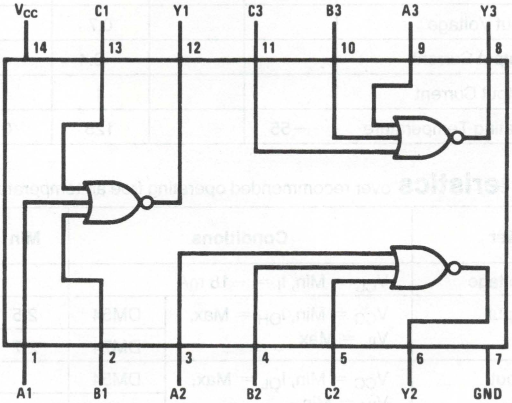
This device contains three independent gates each of which performs the logic NOR function.

Features

- ■ Alternate Military/Aerospace device (54LS27) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6359-1

Order Number 54LS27DMQB, 54LS27FMQB, 54LS27LMQB, DM54LS27J, DM54LS27W, DM74LS27M or DM74LS27N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS27			DM74LS27			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			2	4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3.4	6.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	13	5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

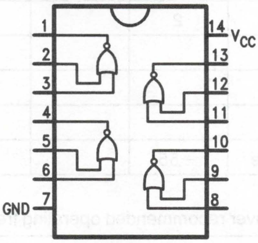
54LS28/DM74LS28 Quad 2-Input NOR Buffer

General Description

The 'LS28 contains four independent gates each of which perform the logic NOR function.

Connection Diagram

Dual-In-Line Package



TL/F/10169–1

Order Number 54LS28DMQB, 54LS28FMQB, 54LS28LMQB, DM74LS28M or DM74LS28N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS28			DM74LS28			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1.2			−1.2	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−30		−130	mA
			DM74	−30		−130	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max				3.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max				13.8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = +5.0V, T_A = +25°C (See Section 1 for test waveforms and output load)

Symbol	Parameter	$R_L = 2\ k\Omega$ $C_L = 15\ pF$		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		20	ns

National Semiconductor

54LS30/DM54LS30/DM74LS30
8-Input NAND Gate

General Description

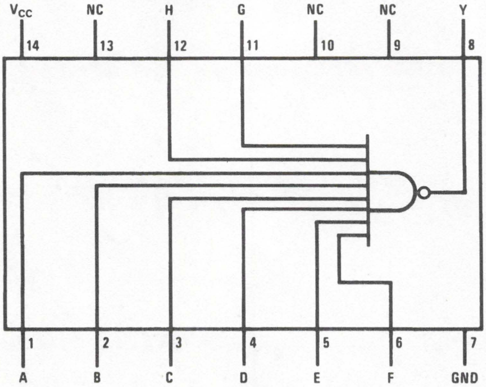
This device contains a single gate which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (54LS30) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6360–1

Order Number 54LS30DMQB, 54LS30FMQB, 54LS30LMQB, DM54LS530W, DM74LS30M or DM74LS30N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{ABCDEFGH}$

Inputs	Output
A thru H	**Y**
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS30			DM74LS30			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.35	0.5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			0.6	1.1	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	12	5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	4	15	5	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

54LS32/DM54LS32/DM74LS32 Quad 2-Input OR Gates

General Description

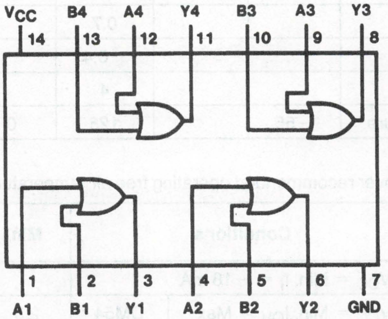
This device contains four independent gates each of which performs the logic OR function.

Features

- Alternate Military/Aerospace device (54LS32) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6361–1

Order Number 54LS32DMQB, 54LS32FMQB, 54LS32LMQB, DM54LS32J, DM54LS32W, DM74LS32M or DM74LS32N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Y = A + B

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS32			DM74LS32			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			3.1	6.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			4.9	9.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

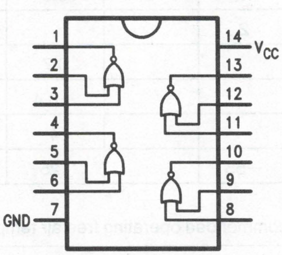
54LS33/DM74LS33
Quad 2-Input NOR Buffer with Open-Collector Outputs

General Description

This device contains four independent gates each of which perform the logic NOR function. Outputs are open-collector.

Connection Diagram

Dual-In-Line Package



TL/F/10170–1

Order Number 54LS33DMQB, 54LS33FMQB, DM74LS33M or DM74LS33N
See NS Package Number J14A, M14A, N14A or W14B

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS33			DM74LS33			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max				100	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max V_{IN} = GND				3.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max V_{IN} = Open				13.8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 2\ k\Omega$ $C_L = 15\ pF$		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		22	ns

National Semiconductor

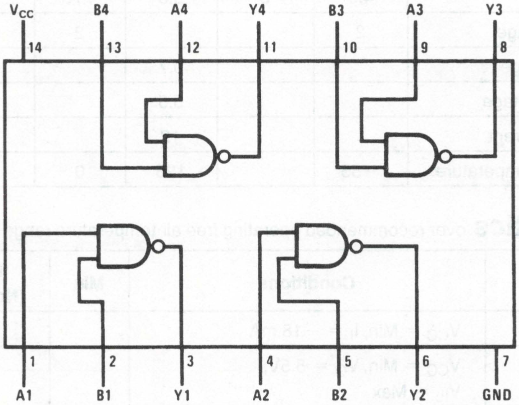
54LS37/DM74LS37
Quad 2-Input NAND Buffers

General Description

This device contains four independent buffer gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package


V_CC
B4
A4
Y4
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
Y1
A2
B2
Y2
GND

TL/F/6362-1

Order Number 54LS37DMQB, 54LS37FMQB, 54LS37LMQB, DM74LS37M or DM74LS37N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS37			DM74LS37			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1.2			−1.2	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	54LS	2.5			V
			DM74LS	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS			0.4	V
			DM74LS		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V (54LS) V_I = 7V (DM74LS)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	54LS			−0.40	mA
			DM74LS			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−30		−130	mA
			DM74LS	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.9	2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			6	12	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	54LS		DM74LS		Units
		C_L = 50 pF		C_L = 150 pF, R_L = 667Ω		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		20	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		20	4	21	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

54LS38/DM54LS38/DM74LS38 Quad 2-Input NAND Buffers with Open-Collector Outputs

General Description

This device contains four independent gates, each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Features

- Alternate Military/Aerospace device (54LS38) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

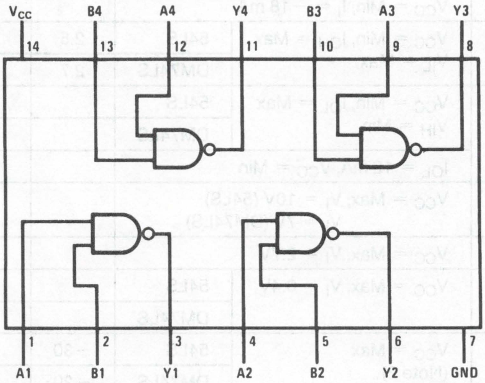
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6363-1

Order Number 54LS38DMQB, 54LS38FMQB, 54LS38LMQB, DM54LS38J, DM74LS38M or DM74LS38N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS38			DM74LS38			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.9	2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			6	12	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 667\Omega$				Units
		C_L = 45 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		22		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		22		29	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

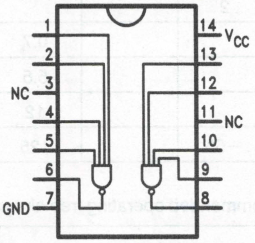
54LS40/DM74LS40
Dual 4-Input NAND Buffer

General Description

This device contains two independent gates each of which perform the logic NAND function.

Connection Diagrams

Dual-In-Line Package



TL/F/10171–1

Order Number 54LS40DMQB, 54LS40FMQB, 54LS40LMQB, DM74LS40M or DM74LS40N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS40			DM74LS40			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1.2			−1.2	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−30		−130	mA
			DM74	−30		−130	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max, V_{IN} = GND				1.0	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max, V_{IN} = OPEN				6.0	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Note more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	$R_L = 2\ k\Omega$ $C_L = 15\ pF$		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		24	ns

National Semiconductor

54LS42/DM54LS42/DM74LS42 BCD/Decimal Decoders

General Description

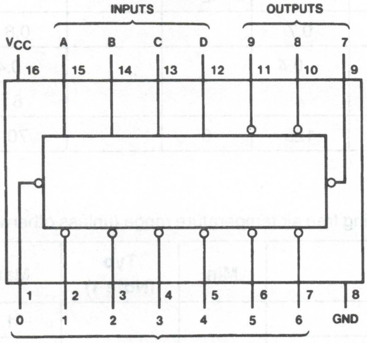
These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10–15) input conditions.

Features

- Diode clamped inputs
- Also for applications as 4-line-to-16-line decoders; 3-line-to-8-line decoders
- All outputs are high for invalid input conditions
- Alternate Military/Aerospace device (54LS42) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package


INPUTS
OUTPUTS
V_{CC}
A
B
C
D
9
8
7
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
0
1
2
3
4
5
6
GND
OUTPUTS

TL/F/6365–1

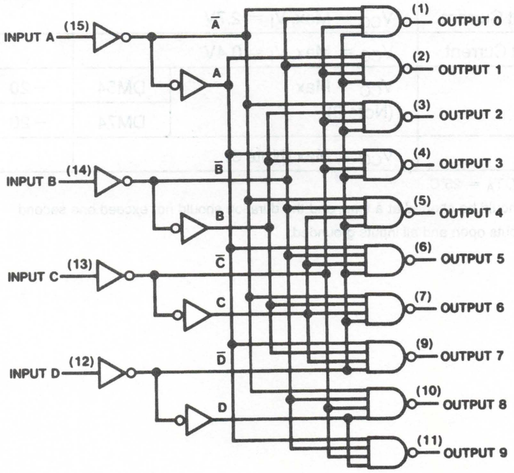
Order Number 54LS42DMQB, 54LS42FMQB, DM54LS42J, DM54LS42W, DM74LS42M or DM74LS42N
See NS Package Number J16A, M16A, N16E or W16A

Function Table

No.	BCD Inputs				Decimal Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level
L = Low Level

Logic Diagram


INPUT A
(15)
$\overline{A}$
A
INPUT B
(14)
$\overline{B}$
B
INPUT C
(13)
$\overline{C}$
C
INPUT D
(12)
$\overline{D}$
D
(1) OUTPUT 0
(2) OUTPUT 1
(3) OUTPUT 2
(4) OUTPUT 3
(5) OUTPUT 4
(6) OUTPUT 5
(7) OUTPUT 6
(9) OUTPUT 7
(10) OUTPUT 8
(11) OUTPUT 9

TL/F/6365–2

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 7V
Input Voltage 7V
Operating Free Air Temperature Range
DM54LS and 54LS −55°C to +125°C
DM74LS 0°C to +70°C
Storage Temperature Range −65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS42			DM74LS42			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			7	13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$				Units
			$C_L = 15\ pF$		$C_L = 50\ pF$		
			Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C, or D (2 Levels of Logic) to Output		25		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C, or D (3 Levels of Logic) to Output		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C, or D (2 Levels of Logic) to Output		25		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C, or D (3 Levels of Logic) to Output		30		35	ns

National Semiconductor

54LS47/DM74LS47
BCD to 7-Segment Decoder/Driver

General Description

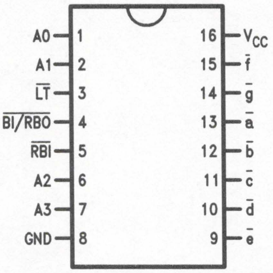
The 'LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 24 mA in the ON (LOW) state and withstand 15V in the OFF (HIGH) state with a maximum leakage current of 250 μA. Auxiliary inputs provided blanking, lamp test and cascadable zero-suppression functions. Also see the 'LS47 data sheet.

Features

- Open-collector outputs
- Drive indicator segments directly
- Cascadable zero-suppression capability
- Lamp test input

Connection Diagram

Dual-In-Line Package


A0 1
A1 2
$\overline{LT}$ 3
$\overline{BI}/\overline{RBO}$ 4
$\overline{RBI}$ 5
A2 6
A3 7
GND 8
16 V_{CC}
15 $\bar{f}$
14 $\bar{g}$
13 $\bar{a}$
12 $\bar{b}$
11 $\bar{c}$
10 $\bar{d}$
9 $\bar{e}$

TL/F/9817-1

Order Number 54LS47DMQB, 54LS47FMQB, DM74LS47M or DM74LS47N
See NS Package Number J16A, M16A, N16E or W16A

Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI}/\overline{RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
$\bar{a}$–$\bar{g}$	*Segment Outputs (Active LOW)

*OC—Open Collector

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS47			DM74SL47			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current @ 15V = V_{OH}*			−50			−250	µA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

*OFF state at $\overline{a}$–$\overline{g}$.

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.4			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				100	µA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2), I_{OS} at $\overline{BI}/\overline{RBO}$	54LS	−0.3		−2.0	mA
			DM74	−0.3		−2.0	
I_{CC}	Supply Current	V_{CC} = Max				13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = +5.0V, T_A = +25°C

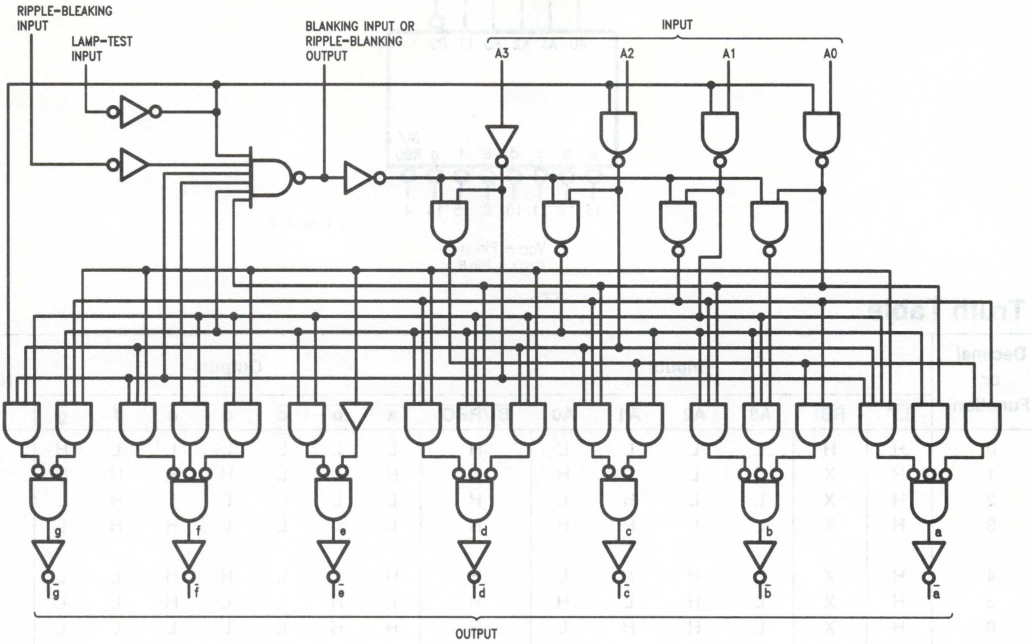
Symbol	Parameter	Conditions	R_L = 665Ω C_L = 15 pF		Units
			Min	Max	
t_{PLH} t_{PHL}	Propagation Delay An to $\overline{a}-\overline{g}$			100 100	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{RBI}}$ to $\overline{a}-\overline{g}$*			100 100	ns

*$\overline{\text{LT}}$ = HIGH, A0–A3 = LOW

Functional Description

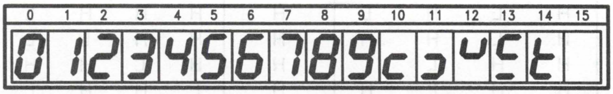
The 'LS47 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the $\overline{\text{RBI}}$ blanks the display and causes a multidigit display. For example, by grounding the $\overline{\text{RBI}}$ of the highest order decoder and connecting its $\overline{\text{BI/RBO}}$ to $\overline{\text{RBI}}$ of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding $\overline{\text{RBI}}$ of the lowest order decoder and connecting its $\overline{\text{BI/RBO}}$ to $\overline{\text{RBI}}$ of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, i.e.: by driving $\overline{\text{RBI}}$ of a intermediate decoder from an OR gate whose inputs are $\overline{\text{BI/RBO}}$ of the next highest and lowest order decoders. $\overline{\text{BI/RBO}}$ also serves as an unconditional blanking input. The internal NAND gate that generates the $\overline{\text{RBO}}$ signal has a resistive pull-up, as opposed to a totem pole, and thus $\overline{\text{BI/RBO}}$ can be forced LOW by external means, using wired-collector logic. A LOW signal thus applied to $\overline{\text{BI/RBO}}$ turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to $\overline{\text{LT}}$ turns on all segment outputs, provided that $\overline{\text{BI/RBO}}$ is not forced LOW.

Logic Diagram


RIPPLE-BLEAKING INPUT
LAMP-TEST INPUT
BLANKING INPUT OR RIPPLE-BLANKING OUTPUT
INPUT
A3
A2
A1
A0
g
f
e
d
c
b
a
$\bar{g}$
$\bar{f}$
$\bar{e}$
$\bar{d}$
$\bar{c}$
$\bar{b}$
$\bar{a}$
OUTPUT

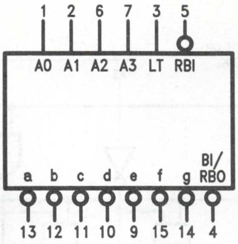
TL/F/9817-3

Numerical Designations—Resultant Displays


0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

TL/F/9817-4

Logic Symbol



TL/F/9817-2

V_{CC} = Pin 16
GND = Pin 8

Truth Table

Decimal or Function	Inputs							Outputs							Note
	$\overline{\text{LT}}$	$\overline{\text{RBI}}$	A3	A2	A1	A0	$\overline{\text{BI}}/\overline{\text{RBO}}$	$\overline{\text{a}}$	$\overline{\text{b}}$	$\overline{\text{c}}$	$\overline{\text{d}}$	$\overline{\text{e}}$	$\overline{\text{f}}$	$\overline{\text{g}}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	1
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	1
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{\text{BI}}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	2
$\overline{\text{RBI}}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	3
$\overline{\text{LT}}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	4

Note 1: $\overline{\text{BI}}/\overline{\text{RBO}}$ is wire-AND logic serving as blanking input ($\overline{\text{BI}}$) and/or ripple-blanking output ($\overline{\text{RBO}}$). The blanking out ($\overline{\text{BI}}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{\text{RBI}}$) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.

Note 2: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

Note 3: When ripple-blanking input ($\overline{\text{RBI}}$) and inputs A0, A1, A2 and A3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{\text{RBO}}$) goes to a LOW level (response condition).

Note 4: When the blanking input/ripple-blanking output ($\overline{\text{BI}}/\overline{\text{RBO}}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

National Semiconductor

54LS48/DM74LS48
BCD to 7-Segment Decoder

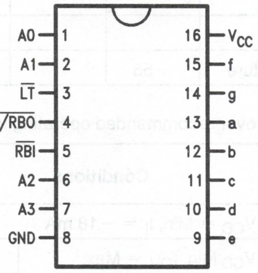
General Description

The 'LS48 translates four lines of BCD (8421) input data into the 7-segment numeral code and provides seven corresponding outputs having pull-up resistors, as opposed to totem pole pull-ups. These outputs can serve as logic signals, with a HIGH output corresponding to a lighted lamp segment, or can provide a 1.3 mA base current to npn lamp driver transistors. Auxiliary inputs provide lamp test, blanking and cascadable zero-suppression functions.

The 'LS48 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration.

Connection Diagram

Dual-In-Line Package


A0 1
A1 2
$\overline{LT}$ 3
$\overline{BI}/\overline{RBO}$ 4
$\overline{RBI}$ 5
A2 6
A3 7
GND 8
16 V_{CC}
15 f
14 g
13 a
12 b
11 c
10 d
9 e

TL/F/10172-1

Order Number 54LS48DMQB, 54LS48FMQB, DM74LS48M, or DM74LS48N
See NS Package Number J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS48			DM74LS48			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−50			−50	μA
I_{OL}	Low Level Output Current			2.0			6.0	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} Min, I_{OH} = Max, V_{IL} = Max	54LS	2.4			V
			DM74	2.4			
I_{OFF}	Output High Current Segment Outputs	V_{CC} = Min, V_O = 0.85V		−1.3			mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 2.0 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, V_O = 0V at $\overline{BI}/\overline{RBO}$ (Note 2)	54LS	−0.3		−2	mA
			DM74	−0.3		−2	
I_{CCH}	Supply Current	V_{CC} = Max, V_{IN} = 4.5V				38	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

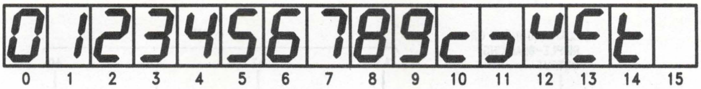
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Time A_n to a–g		100 100	ns
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{RBI}$ to a–f		100 100	ns

Note: $\overline{LT}$ = HIGH, A_0–A_3 = HIGH.

Numerical Designations—Resultant Displays



TL/F/10172-4

Truth Table

Decimal Or Function	Inputs							Outputs						
	$\overline{LT}$	$\overline{RBI}$	A_3	A_2	A_1	A_0	$\overline{BI}/\overline{RBO}$	a	b	c	d	e	f	g
0 (Note 1)	H	H	L	L	L	L	H	H	H	H	H	H	H	L
1 (Note 1)	H	X	L	L	L	H	H	L	H	H	L	L	L	L
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L
$\overline{BI}$ (Note 2)	X	X	X	X	X	X	L	L	L	L	L	L	L	L
$\overline{RBI}$ (Note 3)	H	L	L	L	L	L	L	L	L	L	L	L	L	L
$\overline{LT}$ (Note 4)	L	X	X	X	X	X	H	H	H	H	H	H	H	H

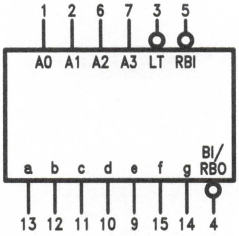
Note 1: $\overline{BI}/\overline{RBO}$ is wired-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

Note 2: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.

Note 3: When ripple-blanking input ($\overline{RBI}$) and inputs A_0, A_1, A_2, and A_3 are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a LOW level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

Note 4: When the blanking input/ripple-blanking output ($\overline{BI}/\overline{RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a HIGH level.

Logic Symbol

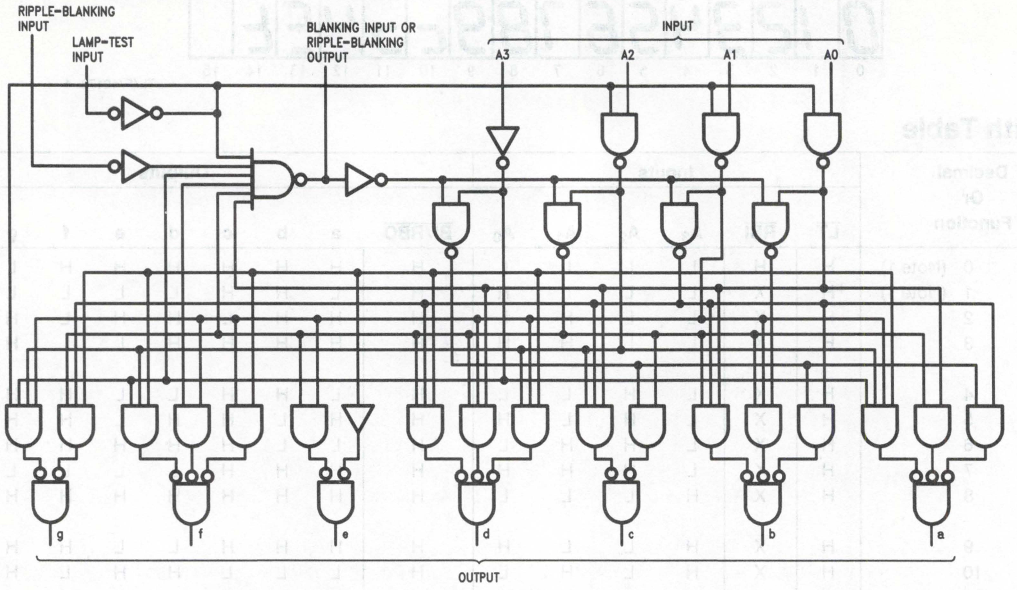


TL/F/10172-2

V_{CC} = Pin 16

GND = Pin 8

Logic Diagram


RIPPLE-BLANKING INPUT
LAMP-TEST INPUT
BLANKING INPUT OR RIPPLE-BLANKING OUTPUT
INPUT
A3
A2
A1
A0
g
f
e
d
c
b
a
OUTPUT

TL/F/10172-3

National Semiconductor

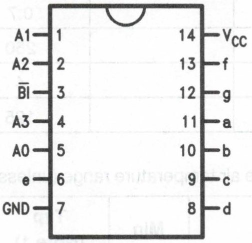
54LS49 BCD to 7-Segment Decoder

General Description

The 54LS49 translates four lines of BCD (8421) input data into the 7-segment numeral code as shown in the Function Table. It has open-collector outputs and is logically the 14-pin verson of the '48, without the lamp test and ripple blanking features. Also see the 'LS249 data sheet.

Connection Diagram

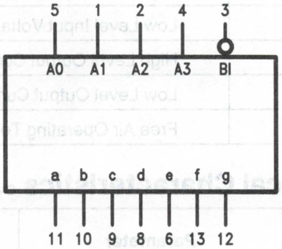
Dual-In-Line Package


A1
A2
BI
A3
A0
e
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8
V_{CC}
f
g
a
b
c
d

TL/F/10204-1

Order Number 54LS49DMQB or 54LS49FMQB
See NS Package Number J14A or W14B

Logic Symbol

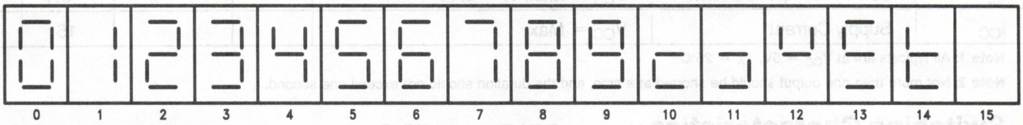

5
1
2
4
3
A0
A1
A2
A3
BI
a
b
c
d
e
f
g
11
10
9
8
6
13
12

TL/F/10204-2

V_{CC} = Pin 14
GND = Pin 7

Pin Names	Description
A0–A3	BCD Inputs
$\overline{BI}$	Blanking Input (Active LOW)
a–g	Segment Outputs (Active HIGH)

Numerical Designations—Resultant Displays


0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

TL/F/10204-3

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS49			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			250	μA
I_{OL}	Low Level Output Current			4	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10.0V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{CC}	Supply Current	V_{CC} = Max			15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and output load)

Symbol	Parameter	54LS		Units
		C_L = 15 pF		
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay; R_L = 2 kΩ A_n to a–g		100 100	ns
t_{PLH} t_{PHL}	Propagation Delay; R_L = 6 kΩ $\overline{BI}$ to a–g		100 100	ns

Function Table

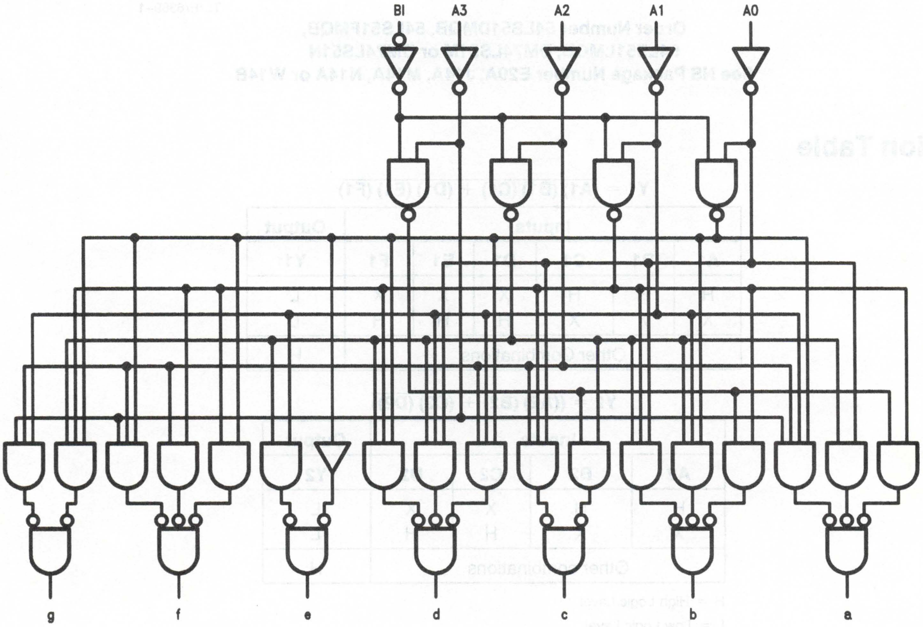
Decimal or Function	Inputs					Outputs							Note
	A3	A2	A1	A0	$\overline{BI}$	a	b	c	d	e	f	g	
0	L	L	L	L	H	H	H	H	H	H	H	L	1
1	L	L	L	H	H	L	H	H	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	
3	L	L	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	L	L	L	L	L	L	L	L	2

Note 1: The blanking input must be open or held at a HIGH level when output functions 0 through 15 are desired.

Note 2: When a LOW level is applied to the blanking input all segment outputs go to a LOW level regardless of the state of any other input condition. X = Input may be HIGH or LOW.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/10204-4

National Semiconductor

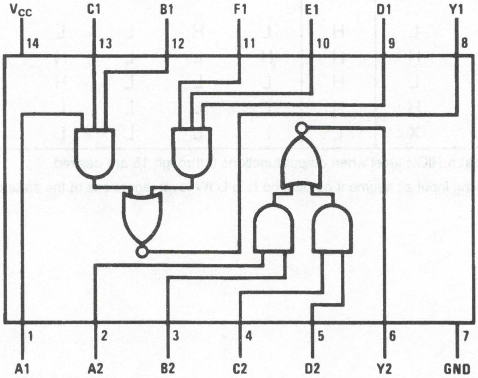
54LS51/DM74LS51 Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-INVERT Gates

General Description

This device contains two independent combinations of gates each of which performs the logic AND-OR-INVERT function. Each package contains one 2-wide 2-input and one 2-wide 3-input AND-OR-INVERT gates.

Connection Diagram

Dual-In-Line Package



TL/F/6369-1

Order Number 54LS51DMQB, 54LS51FMQB, 54LS51LMQB, DM74LS51M or DM74LS51N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$$Y1 = \overline{(A1)\,(B1)\,(C1) + (D1)\,(E1)\,(F1)}$$

Inputs						Output
A1	**B1**	**C1**	**D1**	**E1**	**F1**	**Y1**
H	H	H	X	X	X	L
X	X	X	H	H	H	L
Other Combinations						H

$$Y2 = \overline{((A2)\,(B2) + (C2)\,(D2))}$$

Inputs				Output
A2	**B2**	**C2**	**D2**	**Y2**
H	H	X	X	L
X	X	H	H	L
Other combinations				H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS51			DM74LS51			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V (54LS)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	54LS			−0.40	mA
			DM74			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.4	2.8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	54LS51		DM74LS51		Units
		$C_L = 15$ pF, $R_L = 2$ kΩ		$C_L = 50$ pF, $R_L = 2$ kΩ		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		20	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		20	3	15	ns

National Semiconductor

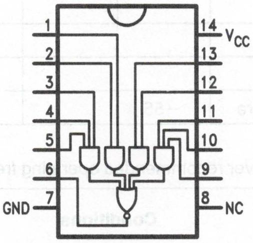
54LS54/DM74LS54
4-WIDE, 2-Input AND-OR-INVERT Gate

General Description

This device contains a combination of four, two input AND gates whose outputs are connected to a four input NOR Gate.

Connection Diagram

Dual-In-Line Package



TL/F/10173-1

Order Number 54LS54DMQB, 54LS54FMQB, DM74LS54M or DM74LS54N
See NS Package Number J14A, M14A, N14A or W14B

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS54			DM74LS54			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Voltage			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74LS	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74LS			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74LS			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74LS	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max V_{IN} = GND				1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max V_{IN} = Open				2.0	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	C_L = 15 pF, R_L = 2 kΩ		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

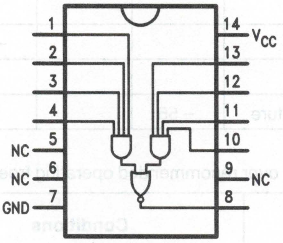
54LS55/DM74LS55
2-Wide, 4-Input AOI Gate

General Description

This device contains a combination of AND-OR-INVERT functions. The internal gates are configured as two, four-input AND gates with their outputs connected to a two-input NOR gate.

Connection Diagram

Dual-In-Line Package



TL/F/10174-1

Order Number 54LS55DMQB, 54LS55FMQB, DM74LS55M or DM74LS55N
See NS Package Number J14A, M14A, N14A or W14B

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS55			DM74LS55			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max, V_{IN} = GND				0.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max, V_{IN} = Open				1.3	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	C_L = 15 pF, R_L = 2 kΩ		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Time		15 15	ns

National Semiconductor

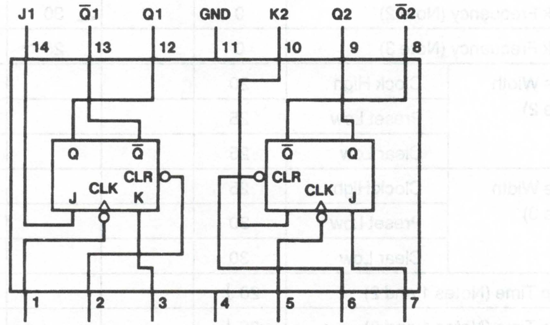
DM54LS73A/DM74LS73A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J and K inputs is allowed to change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6372–1

Order Number DM54LS73AJ, DM54LS73AW, DM74LS73AM or DM74LS73AN
See NS Package Number J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
CLR	**CLK**	**J**	**K**	**Q**	**$\overline{Q}$**
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
↓ = Negative going edge of pulse.
Q_0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS73A			DM74LS73A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 and 2)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 1 and 3)		25↓			25↓			ns
t_H	Hold Time (Notes 1 and 2)		0↓			0↓			ns
t_H	Hold Time (Notes 1 and 3)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	J, K			0.1	mA
			Clear			0.3	
			Clock			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	J, K			20	µA
			Clear			60	
			Clock			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	J, K			−0.4	mA
			Clear			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		20		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		20		28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state, an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock is grounded.

National Semiconductor

54LS74/DM54LS74A/DM74LS74A Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

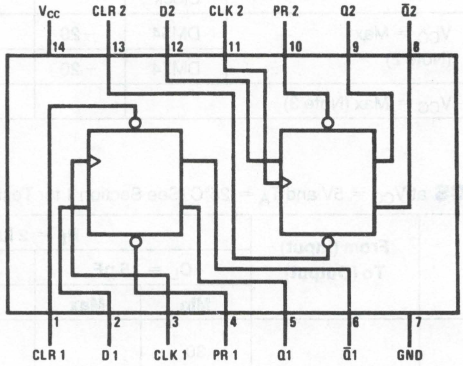
This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate military/aerospace device (54LS74) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6373–1

Order Number 54LS74DMQB, 54LS74FMQB, 54LS74LMQB, DM54LS74AJ, DM54LS74AW, DM74LS74AM or DM74LS74AN
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↑ = Positive-going Transition

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.

Q_0 = The output logic level of Q before the indicated input conditions were established.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS74A			DM74LS74A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
f_{CLK}	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width (Note 2)	Clock High	18			18			ns
		Preset Low	15			15			
		Clear Low	15			15			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	20			20			
		Clear Low	20			20			
t_{SU}	Setup Time (Notes 1 and 2)		20↑			20↑			ns
t_{SU}	Setup Time (Notes 1 and 3)		25↑			25↑			ns
t_H	Hold Time (Note 1 and 4)		0↑			0↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF, $R_L = 2$ kΩ, $T_A = 25°C$, and $V_{CC} = 5V$.

Note 3: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25°C$, and $V_{CC} = 5V$.

Note 4: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max V_I = 7V	Data			0.1	mA
			Clock			0.1	
			Preset			0.2	
			Clear			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Data			20	µA
			Clock			20	
			Clear			40	
			Preset			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Data			−0.4	mA
			Clock			−0.4	
			Preset			−0.8	
			Clear			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with CLOCK grounded after setting the Q and $\overline{Q}$ outputs high in turn.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		30		35	ns

National Semiconductor

DM54LS75/DM74LS75 Quad Latches

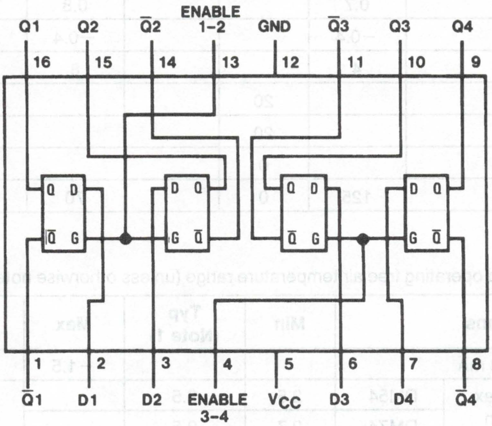
General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occured) is retained at the Q output until the enable is permitted to go high.

These latches feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and are available in 16-pin packages.

Connection Diagram

Dual-In-Line Package


ENABLE 1–2
Q1
Q2
$\overline{Q}$2
GND
$\overline{Q}$3
Q3
Q4
16
15
14
13
12
11
10
9
Q D
$\overline{Q}$ G
D Q
G $\overline{Q}$
Q D
$\overline{Q}$ G
D Q
G $\overline{Q}$
1
2
3
4
5
6
7
8
$\overline{Q}$1
D1
D2
ENABLE 3–4
V_{CC}
D3
D4
$\overline{Q}$4

TL/F/6374–1

Order Number DM54LS75J, DM54LS75W, DM74LS75M or DM74LS75N
See NS Package Number J16A, M16A, N16A or W16A

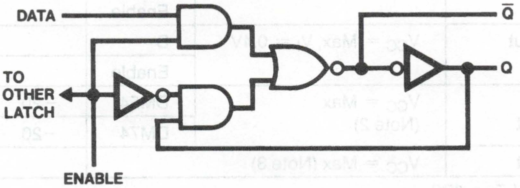
Function Table (Each Latch)

Inputs		Outputs	
D	**Enable**	**Q**	**$\overline{Q}$**
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level, L = Low Level, X = Don't Care

Q_0 = The Level of Q Before the High-to-Low Transition of ENABLE

Logic Diagram (Each Latch)


DATA
$\overline{Q}$
Q
TO OTHER LATCH
ENABLE

TL/F/6374–2

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS75			DM74LS75			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
t_W	Enable Pulse Width (Note 4)	20			20			ns
t_{SU}	Setup Time (Note 4)	20			20			ns
t_H	Hold Time (Note 4)	0			0			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.5		V
			DM74	2.7	3.5		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	D			0.1	mA
			Enable			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	D			20	μA
			Enable			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	D			−0.4	mA
			Enable			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.3	12	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$				Units
			$C_L = 15\ pF$		$C_L = 50\ pF$		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	D to Q		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to Q		17		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to $\overline{Q}$		20		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to $\overline{Q}$		15		20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Q		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Q		25		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to $\overline{Q}$		30		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to $\overline{Q}$		15		20	ns

National Semiconductor

54LS83A/DM54LS83A/DM74LS83A
4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

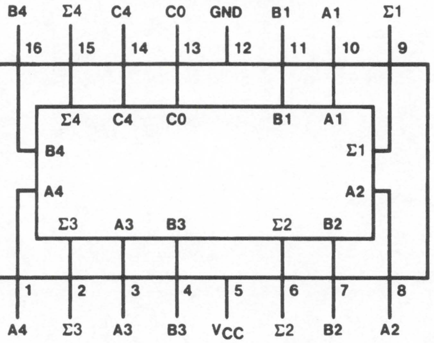
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  - Two 8-bit words 25 ns
  - Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW
- Alternate Military/Aerospace device (54LS83A) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6378-1

Order Number 54LS83ADMQB, 54LS83AFMQB, DM54LS83AJ, DM54LS83AW, DM74LS83AWM or DM74LS83AN
See NS Package Number J16A, M16B, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS83A			DM74LS83A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	A or B			0.2	mA
			C0			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	A or B			40	μA
			C0			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	A or B			−0.8	mA
			C0			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			19	34	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			22	39	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, all B inputs low and all other inputs at 4.5V, or all inputs at 4.5V.

Note 4: I_{CC2} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$				Units
			$C_L = 15\ pF$		$C_L = 50\ pF$		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ1 or Σ2		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ1 or Σ2		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ3		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ3		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ4		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ4		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i, B_i to Σ_i		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i, B_i to Σ_i		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to C4		17		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i, B_i to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i, B_i to C4		17		26	ns

Truth Table

Inputs				Outputs					
				When C0 = L When C2 = L			When C0 = H When C2 = H		
A1 A3	B1 B3	A2 A4	B2 B4	Σ1 Σ3	Σ2 Σ4	C2 C4	Σ1 Σ3	Σ2 Σ4	C2 C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = High Level, L = Low Level

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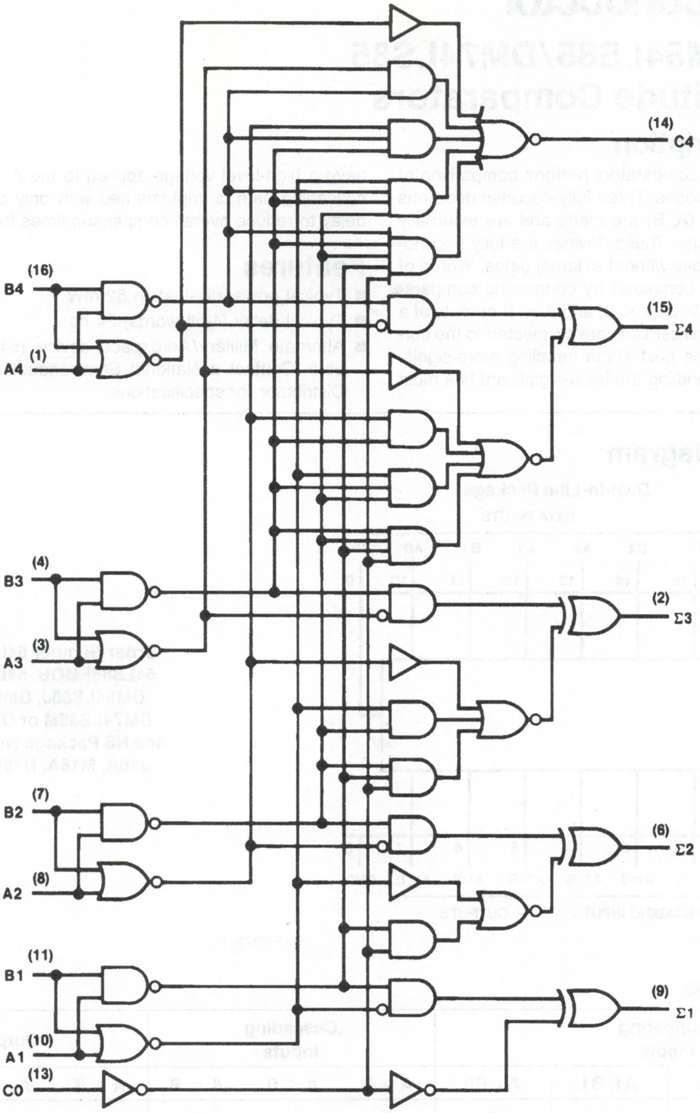
Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Logic Diagram


(16)
B4
(1)
A4
(4)
B3
(3)
A3
(7)
B2
(8)
A2
(11)
B1
(10)
A1
(13)
C0
(14)
C4
(15)
Σ4
(2)
Σ3
(6)
Σ2
(9)
Σ1

TL/F/6378-2

National Semiconductor

54LS85/DM54LS85/DM74LS85 4-Bit Magnitude Comparators

General Description

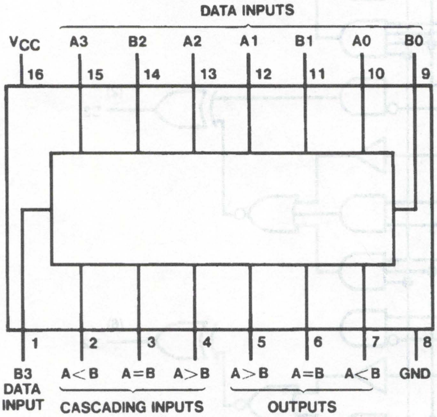
These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two, 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

Features

- Typical power dissipation 52 mW
- Typical delay (4-bit words) 24 ns
- Alternate Military/Aerospace device (54LS85) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6379-1

Order Number 54LS85DMQB, 54LS85FMQB, 54LS85LMQB, DM54LS85J, DM54LS85W, DM74LS85M or DM74LS85N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS85			DM74LS85			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	A < B			0.1	mA
			A > B			0.1	
			Others			0.3	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	A < B			20	μA
			A > B			20	
			Others			60	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	A < B			−0.4	mA
			A > B			−0.4	
			Others			−1.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			10	20	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

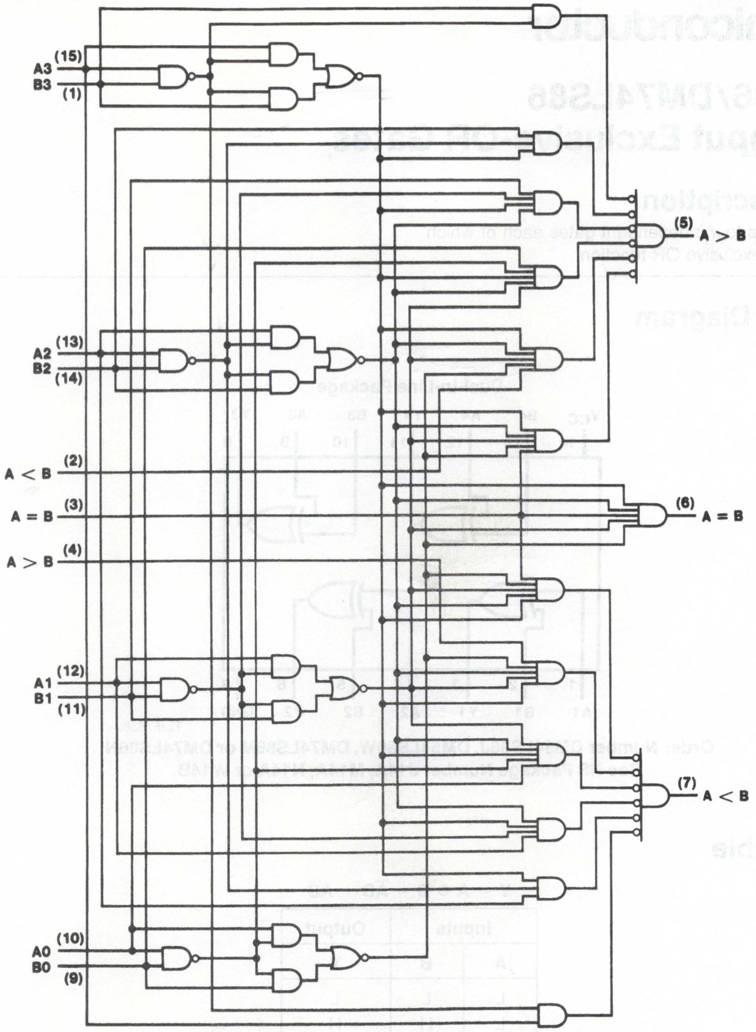
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, A = B grounded and all other inputs at 4.5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From Input	To Output	Number of Gate Levels	$R_L = 2\ k\Omega$				Units
					C_L = 15 pF		C_L = 50 pF		
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	Any A or B Data Input	A < B, A > B	3		36		42	ns
			A = B	4		40		40	
t_{PHL}	Propagation Delay Time High-to-Low Level Output	Any A or B Data Input	A < B, A > B	3		30		40	ns
			A = B	4		30		40	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A < B or A = B	A > B	1		22		26	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A < B or A = B	A > B	1		17		26	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A = B	A = B	2		20		25	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A = B	A = B	2		17		26	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A > B or A = B	A < B	1		22		26	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A > B or A = B	A < B	1		17		26	ns

Logic Diagram


A3
(15)
B3
(1)
A2
(13)
B2
(14)
A < B
(2)
A = B
(3)
A > B
(4)
A1
(12)
B1
(11)
A0
(10)
B0
(9)
(5)
A > B
(6)
A = B
(7)
A < B

TL/F/6379-2

National Semiconductor

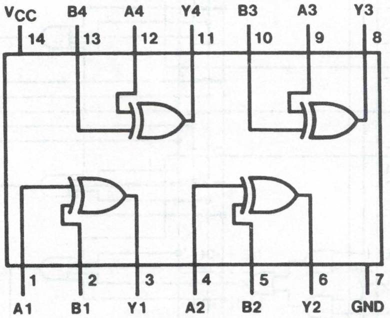
DM54LS86/DM74LS86
Quad 2-Input Exclusive-OR Gates

General Description

This device contains four independent gates each of which performs the logic exclusive-OR function.

Connection Diagram

Dual-In-Line Package



V_{CC}
14
B4
13
A4
12
Y4
11
B3
10
A3
9
Y3
8
1
A1
2
B1
3
Y1
4
A2
5
B2
6
Y2
7
GND

TL/F/6380–1

Order Number DM54LS86J, DM54LS86W, DM74LS86M or DM74LS86N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS86			DM74LS86			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			6.1	10	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)			9	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with all outputs open, one input at each gate at 4.5V, and the other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input Low		18		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			17		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input High		10		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			12		15	ns

National Semiconductor

DM74LS90/DM74LS93 Decade and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 'LS90 and divide-by-eight for the 'LS93.

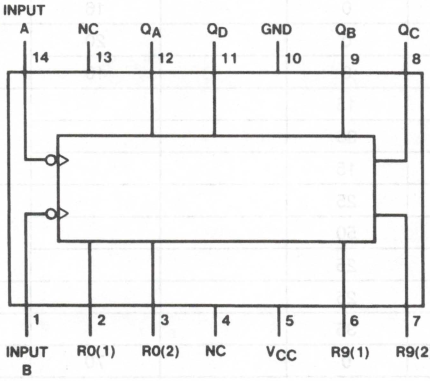
All of these counters have a gated zero reset and the LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade or four bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

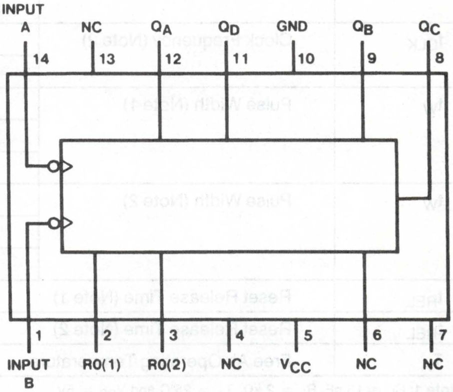
- Typical power dissipation 45 mW
- Count frequency 42 MHz

Connection Diagrams (Dual-In-Line Packages)


INPUT A
NC
Q_A
Q_D
GND
Q_B
Q_C
14
13
12
11
10
9
8
1
2
3
4
5
6
7
INPUT B
R0(1)
R0(2)
NC
V_{CC}
R9(1)
R9(2)

TL/F/6381-1

Order Number DM74LS90M or DM74LS90N
See NS Package Number M14A or N14A


INPUT A
NC
Q_A
Q_D
GND
Q_B
Q_C
14
13
12
11
10
9
8
1
2
3
4
5
6
7
INPUT B
R0(1)
R0(2)
NC
V_{CC}
NC
NC

TL/F/6381-2

Order Number DM74LS93M or DM74LS93N
See NS Package Number M14A or N14A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage (Reset)	7V
Input Voltage (A or B)	5.5V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74LS90			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 1)	A to Q_A	0		32	MHz
		B to Q_B	0		16	
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		20	MHz
		B to Q_B	0		10	
t_W	Pulse Width (Note 1)	A	15			ns
		B	30			
		Reset	15			
t_W	Pulse Width (Note 2)	A	25			ns
		B	50			
		Reset	25			
t_{REL}	Reset Release Time (Note 1)		25			ns
t_{REL}	Reset Release Time (Note 2)		35			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

'LS90 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min (Note 4)			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
		V_{CC} = Max V_I = 5.5V	A			0.2	
			B			0.4	

'LS90 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	μA
			A			40	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

'LS90 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		48		52	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		50		60	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		32		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		30		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		40		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		52	ns

Recommended Operating Conditions

Symbol	Parameter		DM74LS93 Min	DM74LS93 Nom	DM74LS93 Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 1)	A to Q_A	0		32	MHz
		B to Q_B	0		16	
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		20	
		B to Q_B	0		10	
t_W	Pulse Width (Note 1)	A	15			ns
		B	30			
		Reset	15			
t_W	Pulse Width (Note 2)	A	25			ns
		B	50			
		Reset	25			
t_{REL}	Reset Release Time (Note 1)		25			ns
t_{REL}	Reset Release Time (Note 2)		35			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 1: $C_L = 15$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 2: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

’LS93 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min (Note 4)			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
		V_{CC} = Max V_I = 5.5V	A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Reset			20	µA
			A			40	
			B			80	

’LS93 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

’LS93 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		70		85	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		70		90	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		51		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		51		70	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		52	ns

Function Tables

LS90
BCD Count Sequence
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

LS90
Bi-Quinary (5-2)
(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

LS93
Count Sequence
(See Note C)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

LS90
Reset/Count Truth Table

Reset Inputs				Output			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

LS93
Reset/Count Truth Table

Reset Inputs		Output			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

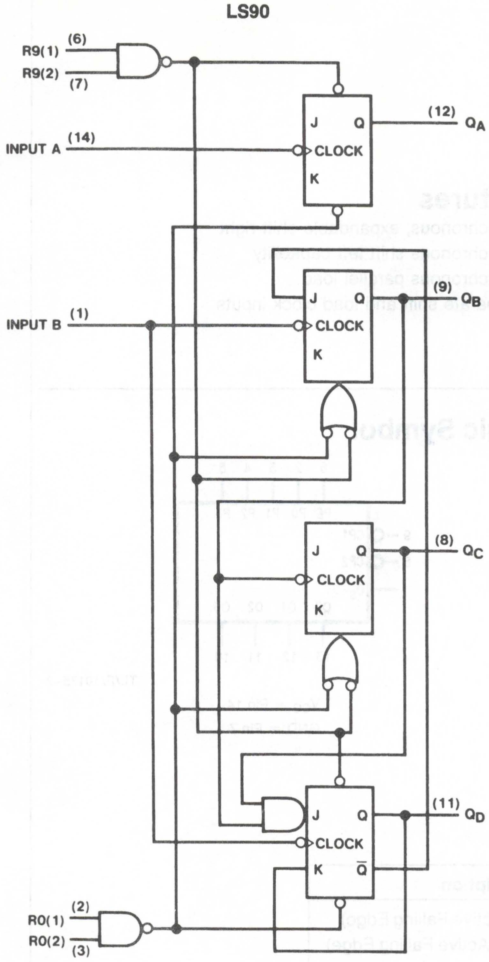
Note A: Output Q_A is connected to input B for BCD count.

Note B: Output Q_D is connected to input A for bi-quinary count.

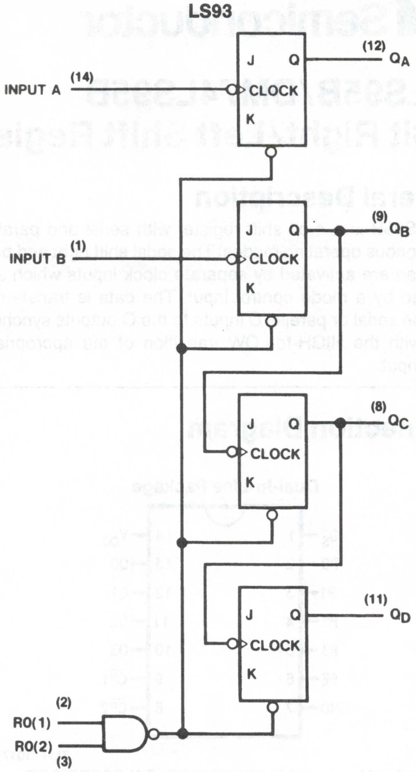
Note C: Output Q_A is connected to input B.

Note D: H = High Level, L = Low Level, X = Don't Care.

Logic Diagrams


LS90
R9(1)
(6)
R9(2)
(7)
INPUT A
(14)
INPUT B
(1)
R0(1)
(2)
R0(2)
(3)
J
Q
CLOCK
K
Q̄
(12)
QA
(9)
QB
(8)
QC
(11)
QD

TL/F/6381-3


LS93
INPUT A
(14)
INPUT B
(1)
R0(1)
(2)
R0(2)
(3)
J
Q
CLOCK
K
(12)
QA
(9)
QB
(8)
QC
(11)
QD

TL/F/6381-4

The J and K inputs shown without connection are for reference only and are functionally at a high level.

National Semiconductor

54LS95B/DM74LS95B
4-Bit Right/Left Shift Register

General Description

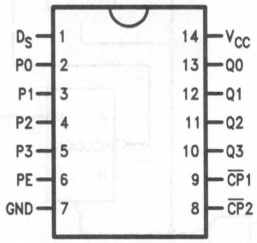
The 'LS95B is a 4-bit shift register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH-to-LOW transition of the appropriate clock input.

Features

- Synchronous, expandable shift right
- Synchronous shift left capability
- Synchronous parallel load
- Separate shift and load clock inputs

Connection Diagram

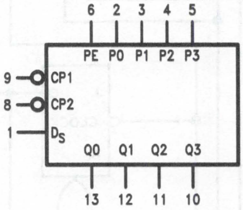
Dual-In-Line Package



TL/F/10175-1

Order Number 54LS95BDMQB, 54LS95BFMQB, DM74LS95BM or DM74LS95BN
See NS Package Number J14A, M14A, N14A or W14B

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

TL/F/10175-2

Pin Names	Description
$\overline{CP}1$	Serial Clock Input (Active Falling Edge)
$\overline{CP}2$	Parallel Clock Input (Active Falling Edge)
D_S	Serial Data Input
P0–P3	Parallel Data Inputs
PE	Parallel Enable Input (Active HIGH)
Q0–Q3	Parallel Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions $V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	54LS95			DM74LS95			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_S or Pn to $\overline{CP}$n	20 20			20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_S or Pn to $\overline{CP}$n	10 10			10 10			ns
t_w (H)	$\overline{CP}$n Pulse Width HIGH	20			20			ns
t_{en} (L)	Enable Time LOW, PE to $\overline{CP}$1	25			25			ns
t_{inh} (H)	Inhibit Time HIGH, PE to $\overline{CP}$1	20			20			ns
t_{en} (H)	Enable Time HIGH, PE to $\overline{CP}$2	25			25			ns
t_{inh} (L)	Inhibit Time LOW, PE to $\overline{CP}$2	20			20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
	PE Input	V_{CC} = Max, V_I = 10V				200	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
	PE Input	V_{CC} = Max, V_I = 2.7V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
	PE Input	V_{CC} = Max, V_I = 0.4V				−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		27	ns
f_{max}	Maximum Shift Frequency	30		MHz

Functional Description

The '95 is a 4-bit shift register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel (P0–P3) Data inputs and four Parallel Data outputs (Q0–Q3). The serial or parallel mode of operation is controlled by a Parallel Enable input (PE) and two Clock inputs, $\overline{CP}1$ and $\overline{CP}2$. The serial (right-shift) or parallel data transfers occur synchronous with the HIGH-to-LOW transition of the selected clock input.

When PE is HIGH, $\overline{CP}2$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}2$ transfers parallel data from the P0–P3 inputs to the Q0–Q3 outputs. When PE is LOW, $\overline{CP}1$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}1$ transfers the data from Serial input (D_S) to Q0 and shifts the data in Q0 to Q1, Q1 to Q2, and Q2 to Q3 respectively (right-shift). A left-shift is accomplished by externally connecting Q3 to P2, Q2 to P1, and Q1 to P0, and operating the '95 in the parallel mode (PE = HIGH). For normal operation, PE should only change states when both Clock inputs are LOW. However, changing PE from LOW to HIGH while $\overline{CP}2$ is HIGH, or changing PE from HIGH to LOW while $\overline{CP}1$ is HIGH and $\overline{CP}2$ is LOW will not cause any changes on the register outputs.

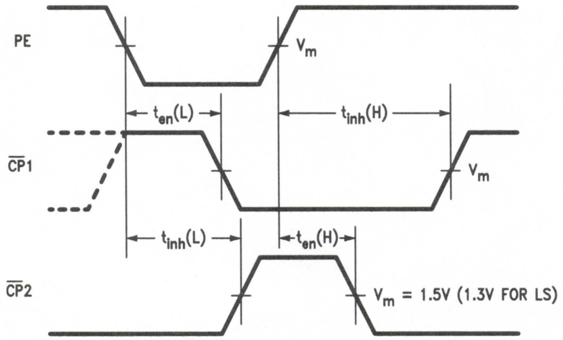
Mode Select Table

Operating Mode	Inputs					Outputs			
	PE	$\overline{CP}1$	$\overline{CP}2$	D_S	Pn	Q0	Q1	Q2	Q3
Shift	L	↓	X	I	X	L	q0	q1	q2
	L	↓	X	h	X	H	q0	q1	q2
Parallel Load	H	X	↓	X	pn	p0	p1	p2	p3
Mode Change	↓	L	L	X	X	No Change			
	↑	L	L	X	X	No Change			
	↓	H	L	X	X	No Change			
	↑	H		X	X	Undetermined			
	↓	L	H	X	X	Undetermined			
	↑	L	H	X	X	No Change			
	↓	H	H	X	X	Undetermined			
	↑	H	H	X	X	No Change			

I = LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.

pn = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

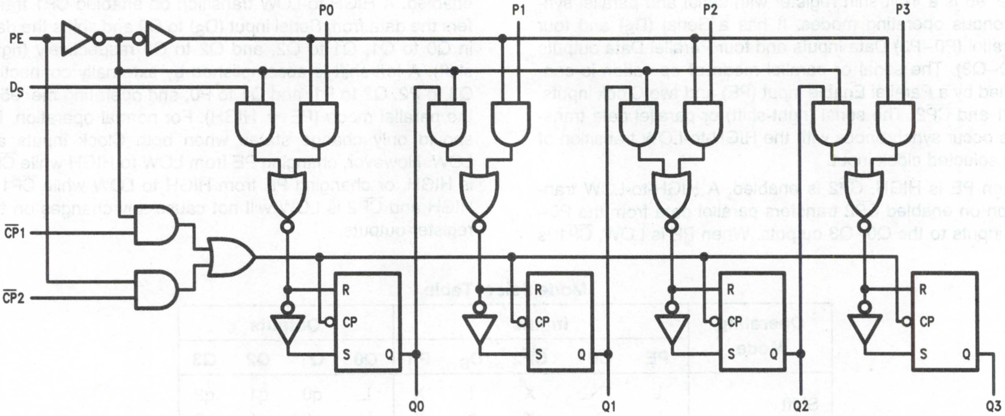
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial



TL/F/10175–3

FIGURE A

Logic Diagram


PE
D_S
$\overline{CP}1$
$\overline{CP}2$
P0
P1
P2
P3
R
CP
S
Q
Q0
Q1
Q2
Q3

TL/F/10175-4

National Semiconductor

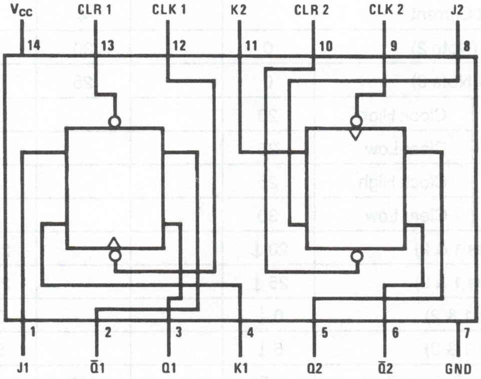
DM54LS107A/DM74LS107A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J and K inputs may change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6367–1

Order Number DM54LS107AJ, DM54LS107AW, DM74LS107AM or DM74LS107AN
See NS Package Number J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
CLR	**CLK**	**J**	**K**	**Q**	**$\overline{Q}$**
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level
X = Either Low or High Logic Level
L = Low Logic Level
↓ = Negative going edge of pulse.
Q_0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS107A Min	DM54LS107A Nom	DM54LS107A Max	DM74LS107A Min	DM74LS107A Nom	DM74LS107A Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 & 2)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 1 & 3)		25↓			25↓			ns
t_H	Hold Time (Notes 1 & 2)		0↓			0↓			ns
t_H	Hold Time (Notes 1 & 3)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF, $R_L = 2$ kΩ, $T_A = 25$°C and $V_{CC} = 5$V.

Note 3: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25$°C and $V_{CC} = 5$V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Clear			0.3	
			Clock			0.4	

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	J, K			20	μA
			Clear			60	
			Clock			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	J, K			−0.4	mA
			Clear			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	6	mA

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		20		28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all inputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

National Semiconductor

54LS109/DM54LS109A/DM74LS109A Dual Positive-Edge-Triggered J-$\overline{K}$ Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

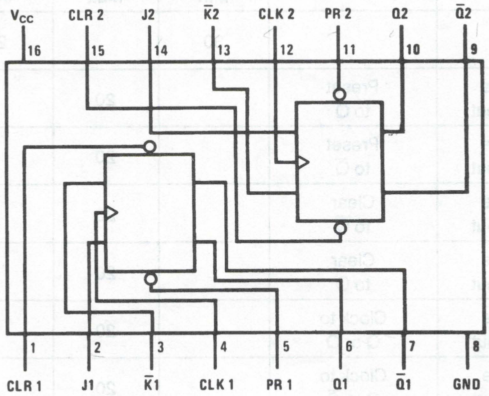
This device contains two independent positive-edge-triggered J-$\overline{K}$ flip-flops with complementary outputs. The J and $\overline{K}$ data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the J and $\overline{K}$ inputs may be changed while the clock is high or low as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate Military/Aerospace device (54LS109) is available. Contact a National Semiconductor Sales Office/Distributor for specifications

Connection Diagram

Dual-In-Line Package



TL/F/6368–1

Order Number 54LS109DMQB, 54LS109FMQB, DM54LS109AJ, DM54LS109AW, DM74LS109AM or DM74LS109AN
See NS Package Number J16A, M16A, N16E or W16A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
↑ = Rising Edge of Pulse

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) state.

Q_0 = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each active transition of the clock pulse.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS109A			DM74LS109A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
f_{CLK}	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width (Note 2)	Clock High	18			18			ns
		Preset Low	15			15			
		Clear Low	15			15			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	20			20			
		Clear Low	20			20			
t_{SU}	Setup Time (Notes 1 & 2)	Data High	30 ↑			30 ↑			ns
		Data Low	20 ↑			20 ↑			
t_{SU}	Setup Time (Notes 1 & 3)	Data High	35 ↑			35 ↑			ns
		Data Low	25 ↑			25 ↑			
t_H	Hold Time (Note 4)		0 ↑			0 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 4: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18\text{ mA}$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		$I_{OL} = 4\text{ mA}, V_{CC} = \text{Min}$	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ $V_I = 7V$	J, $\overline{K}$			0.1	mA
			Clock			0.1	
			Preset			0.2	
			Clear			0.2	
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7V$	J,$\overline{K}$			20	μA
			Clock			20	
			Preset			40	
			Clear			40	
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.4V$	J, $\overline{K}$			−0.4	mA
			Clock			−0.4	
			Preset			−0.8	
			Clear			−0.8	
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 3)			4	8	mA

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\text{ k}\Omega$				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		30		35	ns

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where $V_O = 2.25V$ and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: I_{CC} is measured with all outputs open, with CLOCK grounded after setting the Q and $\overline{Q}$ outputs high in turn.

National Semiconductor

54LS112/DM54LS112A/DM74LS112A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

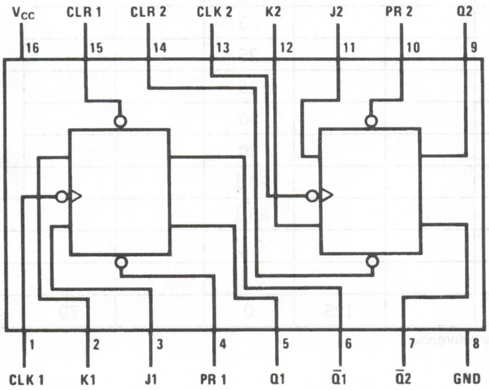
This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the falling edge of the clock pulse. Data on the J and K inputs may be changed while the clock is high or low without affecting the outputs as long as the setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate Military/Aerospace device (54LS112) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6382–1

Order Number 54LS112DMQB, 54LS112FMQB, 54LS112LMQB, DM54LS112AJ, DM54LS112AW, DM74LS112AM or DM74LS112AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Inputs					Outputs	
PR	**CLR**	**CLK**	**J**	**K**	**Q**	**$\overline{Q}$**
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↓ = Negative Going Edge of Pulse

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) level.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS112A			DM74LS112A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 and 2)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 1 and 3)		25↓			25↓			ns
t_H	Hold Time (Notes 1 and 2)		0↓			0↓			ns
t_H	Hold Time (Notes 1 and 3)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		$I_{OL} = 4$ mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, $V_I = 7V$	J, K			0.1	mA
			Clear			0.3	
			Preset			0.3	
			Clock			0.4	

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	μA
			Clear			60	
			Preset			60	
			Clock			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−0.4	mA
			Clear			−0.8	
			Preset			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		20		28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

National Semiconductor

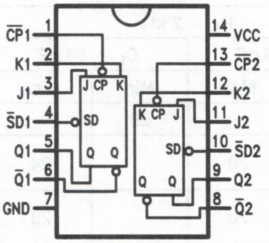
54LS113
Dual JK Edge-Triggered Flip-Flop

General Description

The 54LS113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

Connection Diagram

Dual-In-Line Package

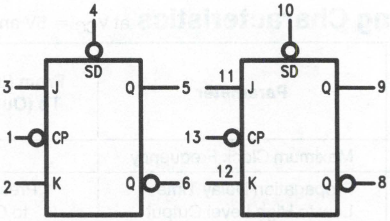


$\overline{CP}$1
K1
J1
$\overline{SD}$1
Q1
$\overline{Q}$1
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8
VCC
$\overline{CP}$2
K2
J2
$\overline{SD}$2
Q2
$\overline{Q}$2
J CP K
SD
Q Q
K CP J
SD
Q Q

TL/F/10205-1

Order Number 54LS113DMQB, 54LS113FMQB or 54LS113LMQB
See NS Package Number E20A, J14A or W14B

Logic Symbol



4
10
SD
SD
3
J
Q
5
11
J
Q
9
1
CP
13
CP
2
K
Q
6
12
K
Q
8

TL/F/10205-2

V_{CC} = Pin 14
GND = Pin 7

Pin Names	Description
J1, J2, K1, K2	Data Inputs
$\overline{CP}$1, $\overline{CP}$2	Clock Pulse Inputs (Active Falling Edge)
$\overline{SD}$1, $\overline{SD}$2	Direct Set Inputs (Active LOW)
Q1, Q2, $\overline{Q}$1, $\overline{Q}$2	Outputs

Truth Table

Inputs		Output
@ t_n		@ $t_n + 1$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

t_n = Bit Time before Clock Pulse
$t_n + 1$ = Bit Time after Clock Pulse
H = HIGH Voltage Level
L = LOW Voltage Level

Asynchronous Input:
Low input to $\overline{S}_D$ sets Q to HIGH level
Set is independent of clock

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS113			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			4	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}_n$	20 20			ns
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}_n$	0 0			ns
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width	20 15			ns
t_w (L)	$\overline{S}_{Dn}$ Pulse Width LOW	15			ns

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V	J, K			0.1	mA
			SD			0.3	
			CP			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	µA
			SD			60	
			CP			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	J, K	−30		−400	µA
			CP, SD	−60		−800	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

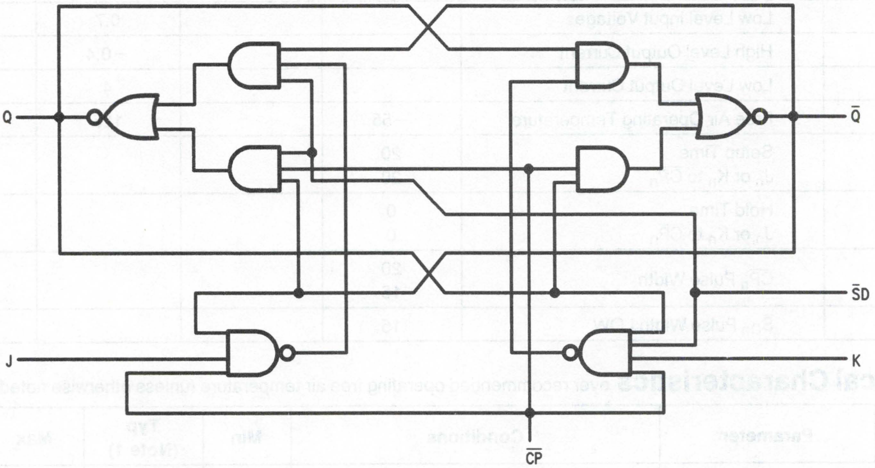
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	54LS113 $C_L = 15$ pF		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$		16 24	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		16 24	ns

Logic Diagram (one half shown)



TL/F/10205-3

National Semiconductor

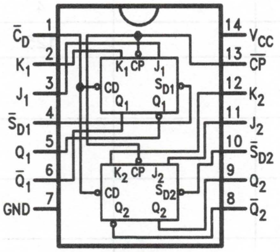
54LS114
Dual JK Negative Edge-Triggered Flip-Flop with Common Clocks and Clears

General Description

The 'LS114 features individual J, K and set inputs and common clock and common clear inputs. When the clock goes HIGH the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the Clock Pulse is HIGH and the bistable will perform according to the truth table as long as the minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

Connection Diagram

Dual-In-Line Package

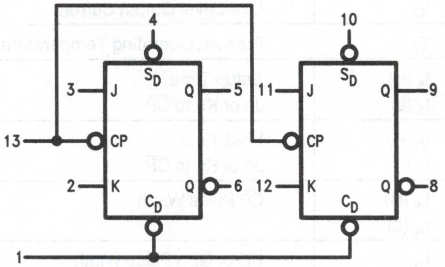


$\overline{C}_D$ 1
K_1 2
J_1 3
$\overline{S}_{D1}$ 4
Q_1 5
$\overline{Q}_1$ 6
GND 7
14 V_{CC}
13 $\overline{CP}$
12 K_2
11 J_2
10 $\overline{S}_{D2}$
9 Q_2
8 $\overline{Q}_2$
K_1 CP J_1
CD S_{D1}
Q_1 $\overline{Q}_1$
K_2 CP J_2
CD S_{D2}
Q_2 $\overline{Q}_2$

TL/F/10176–1

Order Number 54LS114DMQB, 54LS114FMQB or 54LS114LMQB
See NS Package Number E20A, J14A or W14B

Logic Symbol



4
10
S_D
S_D
3 J
Q 5
11 J
Q 9
13
CP
CP
2 K
Q 6
12 K
Q 8
C_D
C_D
1

TL/F/10176–2

V_{CC} = Pin 14
GND = Pin 7

Pin Names	Description
J1, J2, K1, K2	Data Inputs
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)
$\overline{CD}$	Direct Clear Input (Active LOW)
$\overline{SD1}$, $\overline{SD2}$	Direct Set Inputs (Active LOW)
Q1, Q2, $\overline{Q}1$, $\overline{Q}2$	Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range 54LS	 −55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS114			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			4	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time Jn or Kn to $\overline{CP}$	20 20			ns
t_h (H) t_h (L)	Hold Time Jn or Kn to $\overline{CP}$	0 0			ns
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	20 15			ns
t_w	$\overline{CD}$ or $\overline{SD}$n Pulse Width	15			ns

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.5			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.4 0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V; Jn, Kn Inputs SD1, SD2 Inputs CD Input CP Input			0.1 0.3 0.6 0.8	mA mA mA mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V; Jn, Kn Inputs SD1, SD2 Inputs CD Input CP Input			20 60 120 160	μA μA μA μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Electrical Characteristics (Continued)

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V Jn, Kn Inputs SD1, SD2 Inputs CD Input CP Input			−0.4 −0.8 −1.6 −1.44	mA mA mA mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max, V_{CP} = 0V			8.0	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2k, C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Count Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q or $\overline{Q}$		16 24	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CD}$ or $\overline{SD}$n to Q or $\overline{Q}$		16 24	ns

Truth Table

Inputs		Output
@ t_n		@ t_{n+1}
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Q}$n

Asynchronous Inputs:

LOW input to $\overline{SD}$ sets Q to HIGH level

LOW input to $\overline{CD}$ sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on $\overline{CD}$ and $\overline{SD}$ makes both Q and $\overline{Q}$ HIGH

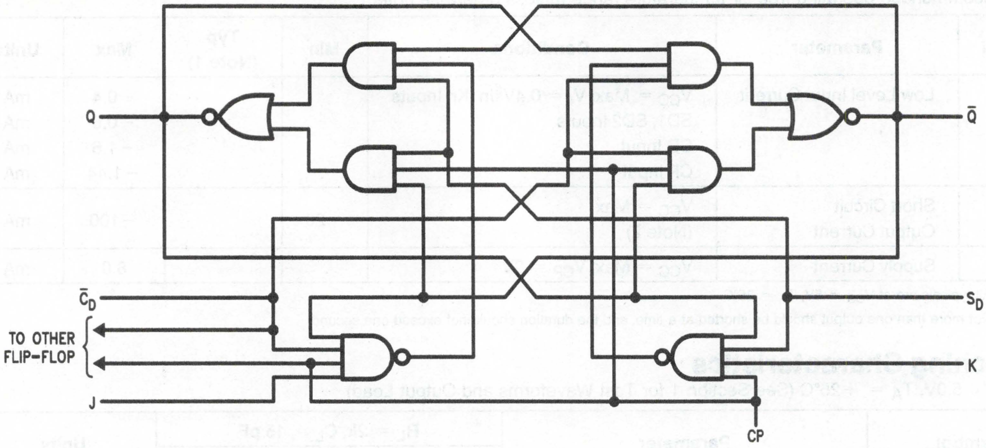
H = HIGH Voltage Level

L = LOW Voltage Level

t_n = Bit time before clock pulse.

t_{n+1} = Bit time after clock pulse.

Logic Diagram (one half shown)


Q
$\overline{Q}$
$\overline{C}_D$
$\overline{S}_D$
TO OTHER FLIP-FLOP
J
K
CP

TL/F/10176-3

National Semiconductor

DM74LS122 Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM74LS122 is a retriggerable monostable multivibrator featuring both positive and negative edge triggering with complementary outputs. An internal 10 kΩ timing resistor is provided for design convenience minimizing component count and layout problems. This device can be used with a single external capacitor. The 'LS122 has two active-low transition triggering inputs (A), two active-high transition triggering inputs (B), and a CLEAR input that terminates the output pulse width at a predetermined time independent of the timing components. The clear (CLR) input also serves as a trigger input when it is pulsed with a low level pulse transition (⊔). To obtain optimum and trouble free operation please read operating rules and NSC one-shot application notes carefully and observe recommendations.

Features

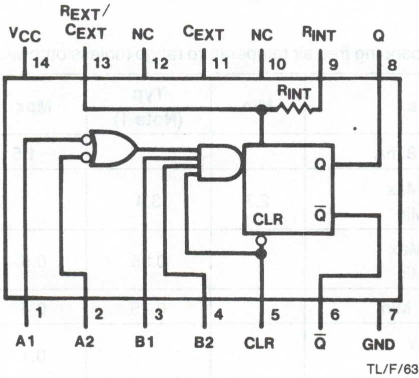
- DC triggered from active-high transition or active-low transition inputs
- Retriggerable to 100% duty cycle
- Over-riding clear terminates output pulse
- Internal 10 kΩ timing resistor
- TTL, DTL compatible
- Compensated for V_{CC} and temperature variations
- Input clamp diodes

Functional Description

The basic output pulse width is determined by selection of the internal resistor R_{INT} or an external resistor (R_X) and capacitor (C_X). Once triggered, the output pulse width may be extended by retriggering the gated active-low (A) transition inputs or the active-high transition (B) inputs or the CLEAR input. The output pulse width can be reduced or terminated by overriding it with the active-low CLEAR input.

Connection Diagram

Dual-In-Line Package



TL/F/6385-1

Order Number DM74LS122M or DM74LS122N
See NS Package Number M14A or N14A

Function Table

Inputs					Outputs	
CLEAR	**A1**	**A2**	**B1**	**B2**	**Q**	**Q̅**
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⊓	⊔
H	L	X	H	↑	⊓	⊔
H	X	L	↑	H	⊓	⊔
H	X	L	H	↑	⊓	⊔
H	H	↓	H	H	⊓	⊔
H	↓	↓	H	H	⊓	⊔
H	↓	H	H	H	⊓	⊔
↑	L	X	H	H	⊓	⊔
↑	X	L	H	H	⊓	⊔

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⊓ = A Positive Pulse
⊔ = A Negative Pulse

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameters		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
t_W	Pulse Width (Note 6)	A or B High	40			ns
		A or B Low	40			
		Clear Low	40			
R_{EXT}	External Timing Resistor		5		260	kΩ
C_{EXT}	External Timing Capacitance		No Restriction			µF
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal				50	pF
T_A	Free Air Operating Temperature		0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Notes 3, 4 and 5)		6	11	mA

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$				Units
			$C_L = 15\ pF$, $C_{EXT} = 0\ pF$, $R_{EXT} = 5\ k\Omega$		$C_L = 15\ pF$, $C_{EXT} = 1000\ pF$, $R_{EXT} = 10\ k\Omega$		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q		33			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q		44			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to $\overline{Q}$		45			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to $\overline{Q}$		56			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		45			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		27			ns
$t_{WQ(Min)}$	Minimum Width of Pulse at Output Q	A or B to Q		200			ns
$t_{W(out)}$	Output Pulse Width	A or B to Q			4	5	µs

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open, $C_{EXT} = 0.02\ \mu F$, and $R_{EXT} = 25\ k\Omega$.

Note 4: I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open, $C_{EXT} = 0.02\ \mu F$, and $R_{EXT} = 25\ k\Omega$.

Note 5: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to the clock.

Note 6: $T_A = 25°C$ and $V_{CC} = 5V$.

Operating Rules

1. To use the internal 10 kΩ timing resistor, connect the R_{INT} pin to V_{CC}.
2. An external resistor (R_X) or the internal resistor (10 kΩ) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants use high-quality mica, glass, polypropylene, polycarbonate, or polystyrene capacitors. For large time constants use solid tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
3. The pulse width is essentially determined by external timing components R_X and C_X. For $C_X < 1000$ pF see *Figure 1;* design curves on T_W as function of timing components value. For $C_X >> 1000$ pF the output is defined as:

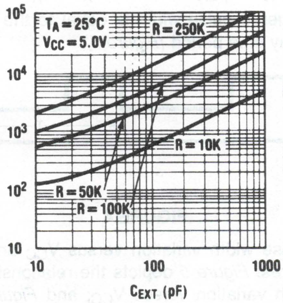
$$T_W = KR_XC_X$$

where [R_X is in kΩ]

[C_X is in pF]

[T_W is in ns]

$K \approx 0.37$

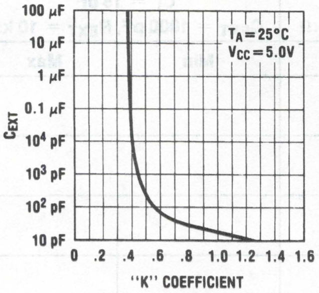


TL/F/6385–2

FIGURE 1

Operating Rules (Continued)

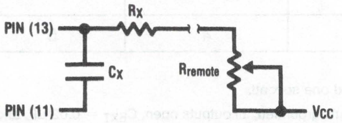
The K factor is not a constant, but, varies with C_X. See *Figure 2*.



TL/F/6385–3

FIGURE 2

4. The switching diode required for most TTL one-shots when using an electrolytic timing capacitor is not needed for the 'LS122 and should not be used.
5. To obtain variable pulse width by remote trimming, the following circuit is recommended:



TL/F/6385–4

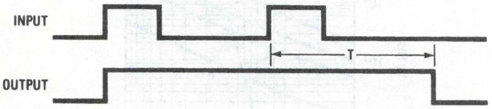
Note: "R_{remote}" should be as close to the device pins as possible.

FIGURE 3

6. The retriggerable pulse width is calculated as shown below:

$$T = T_W + t_{PLH} = 0.50 \times R_X \times C_X + T_{PLH}$$

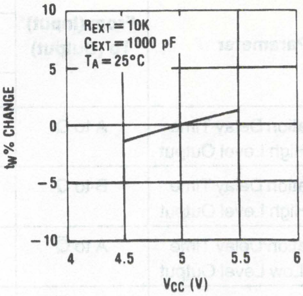
The retriggered pulse width is equal to the pulse width plus a delay time period *(Figure 4)*.



TL/F/6385–5

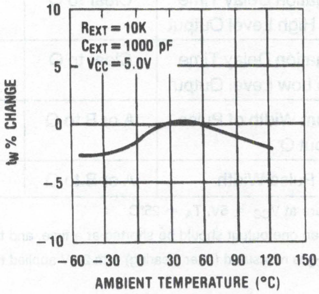
FIGURE 4

7. Output pulse width variation versus V_{CC} and operation temperatures: *Figure 5* depicts the relationship between pulse width variation versus V_{CC}; and *Figure 6* depicts pulse width variation versus temperatures.



TL/F/6385–6

FIGURE 5



TL/F/6385–7

FIGURE 6

8. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (13) and (11) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.
9. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 µF to 0.10 µF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC} pin as space permits.

***For further detailed device characteristics and output performance please refer to the NSC one-shot application note AN-366.**

National Semiconductor

DM74LS123 Dual Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM74LS123 is a dual retriggerable monostable multivibrator capable of generating output pulses from a few nanoseconds to extremely long duration up to 100% duty cycle. Each device has three inputs permitting the choice of either leading edge or trailing edge triggering. Pin (A) is an active-low transition trigger input and pin (B) is an active-high transition trigger input. The clear (CLR) input terminates the output pulse at a predetermined time independent of the timing components. The clear input also serves as a trigger input when it is pulsed with a low level pulse transition (⊔). To obtain the best trouble free operation from this device please read the operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

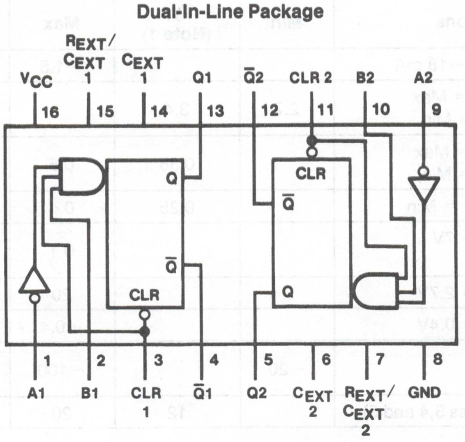
Features

- DC triggered from active-high transition or active-low transition inputs
- Retriggerable to 100% duty cycle
- Compensated for V_{CC} and temperature variations
- Triggerable from CLEAR input
- DTL, TTL compatible
- Input clamp diodes

Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width may be extended by retriggering the gated active-low transition or active-high transition inputs or be reduced by use of the active-low or CLEAR input. Retriggering to 100% duty cycle is possible by application of an input pulse train whose cycle time is shorter than the output cycle time such that a continuous "HIGH" logic state is maintained at the "Q" output.

Connection Diagram



TL/F/6386–1

Order Number DM74LS123M or DM74LS123N
See NS Package Number M16A or N16E

Function Table

Inputs			Outputs	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⊓ = A Positive Pulse
⊔ = A Negative Pulse

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
t_W	Pulse Width (Note 6)	A or B High	40			ns
		A or B Low	40			
		Clear Low	40			
R_{EXT}	External Timing Resistor		5		260	kΩ
C_{EXT}	External Timing Capacitance			No Restriction		μF
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal				50	pF
T_A	Free Air Operating Temperature		0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Notes 3,4 and 5)		12	20	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{EXT} = 0.02 μF, and R_{EXT} = 25 kΩ.

Note 4: I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{EXT} = 0.02 μF, and R_{EXT} = 25 kΩ.

Note 5: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to the clock.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C

Symbol	Parameters	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15pF C_{EXT} = 0 pF, R_{EXT} = 5 kΩ		C_L = 15pF C_{EXT} = 1000 pF, R_{EXT} = 10 KΩ		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q		33			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q		44			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to $\overline{Q}$		45			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to $\overline{Q}$		56			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		45			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		27			ns
$t_{WQ(Min)}$	Minimum Width of Pulse at Output Q	A or B to Q		200			ns
$t_{W(out)}$	Output Pulse Width	A or B to Q			4	5	µs

Operating Rules

1. An external resistor (R_X) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitors may be used. For large time constants use tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current. This switching diode is not needed for the 'LS123 one-shot and should not be used. In general the use of the switching diode is not recommended with retriggerable operation.
3. For $C_X >> 1000$ pF the output pulse width (T_W) is defined as follows:

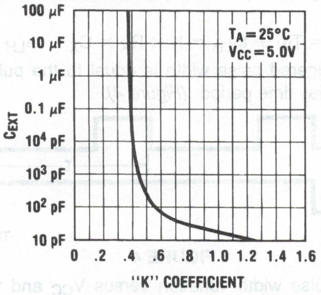
   $T_W = KR_X C_X$

   where [R_X is in kΩ]

   [C_X is in pF]

   [T_W is in ns]

   $K \approx 0.37$
4. The multiplicative factor K is plotted as a function of C_X below for design considerations:

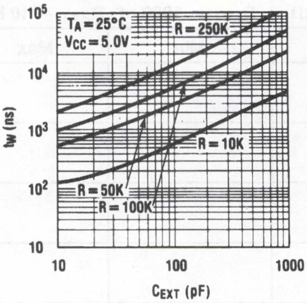


TL/F/6386–2

FIGURE 1

Operating Rules (Continued)

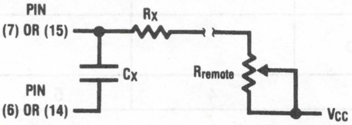
5. For $C_X < 1000$ pF see *Figure 2* for T_W vs C_X family curves with R_X as a parameter:



TL/F/6386-3

FIGURE 2

6. To obtain variable pulse widths by remote trimming, the following circuit is recommended:



TL/F/6386-4

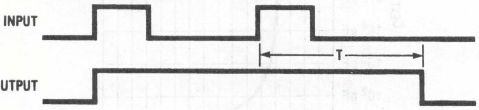
FIGURE 3

Note: "R_{remote}" should be as close to the device pin as possible.

7. The retriggerable pulse width is calculated as shown below:

$$T = T_W + t_{PLH} = K \times R_X \times C_X + t_{PLH}$$

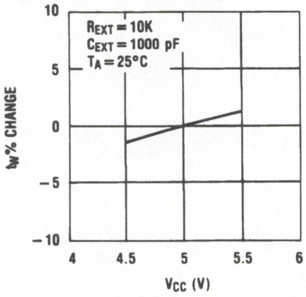
The retriggered pulse width is equal to the pulse width plus a delay time period *(Figure 4)*.



TL/F/6386-5

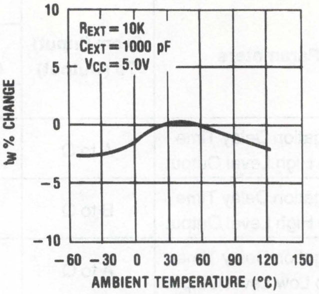
FIGURE 4

8. Output pulse width variation versus V_{CC} and temperatures: *Figure 5* depicts the relationship between pulse width variation versus V_{CC}, and *Figure 6* depicts pulse width variation versus temperatures.



TL/F/6386-6

FIGURE 5



TL/F/6386-7

FIGURE 6

9. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.

10. The C_{EXT} pins of this device are internally connected to the internal ground. For optimum system performance they should be hard wired to the system's return ground plane.

11. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 μF to 0.10 μF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC}-pin as space permits.

For further detailed device characteristics and output performance please refer to the NSC one-shot application note AN-336.

National Semiconductor

54LS125A/DM54LS125A/DM74LS125A Quad TRI-STATE® Buffers

General Description

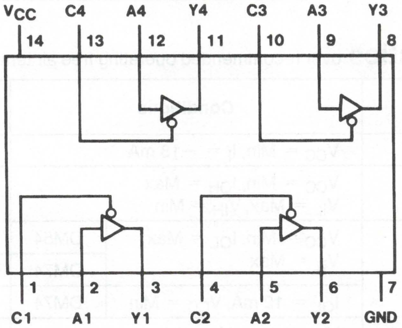
This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Features

- Alternate Military/Aerospace device (54LS125) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6387–1

Order Number 54LS125ADMQB, 54LS125AFMQB, 54LS125ALMQB, DM54LS125AJ, DM54LS125AW, DM74LS125AM or DM74LS125AN See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Y = A

Inputs		Output
A	C	Y
L	L	L
H	L	H
X	H	Hi-Z

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS125A			DM74LS125A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			11	20	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the data control (C) inputs at 4.5V and the data inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		15		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		18		22	ns
t_{PZH}	Output Enable Time to High Level Output		25		35	ns
t_{PZL}	Output Enable Time to Low Level Output		25		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)		20			ns

Note 1: C_L = 5pF.

National Semiconductor

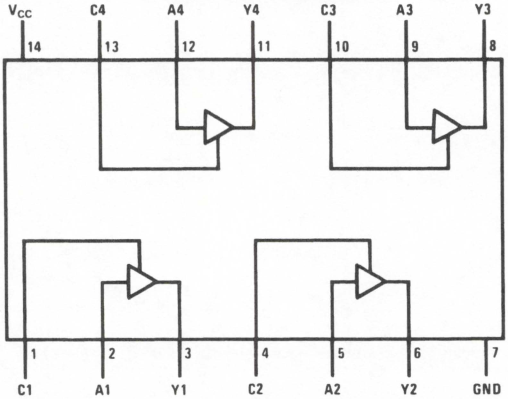
54LS126/DM74LS126A Quad TRI-STATE® Buffers

General Description

This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6388-1

Order Number 54LS126DMQB, 54LS126FMQB, DM74LS126AM or DM74LS126AN
See NS Package Number M14A, N14A or W14B

Function Table

Y = A

Inputs		Output
A	**C**	**Y**
L	H	L
H	H	H
X	L	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS126			DM74LS126A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V (54LS) V_I = 7V (DM74)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−30		−130	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM74		12	22	mA
I_{CCL}	Supply Current	V_I = 0V	54LS			24	mA
I_{CCH}	Supply Current	V_I = 4.5V	54LS			20	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with both the output control and data inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	54LS C_L = 50 pF		DM74LS C_L = 150 pF, R_L = 667Ω		Units
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		15		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		18		22	ns
t_{PZH}	Output Enable Time to High Level Output		30		36	ns
t_{PZL}	Output Enable Time to Low Level Output		20		42	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)		30			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)		30			ns

Note 1: C_L = 5pF.

National Semiconductor

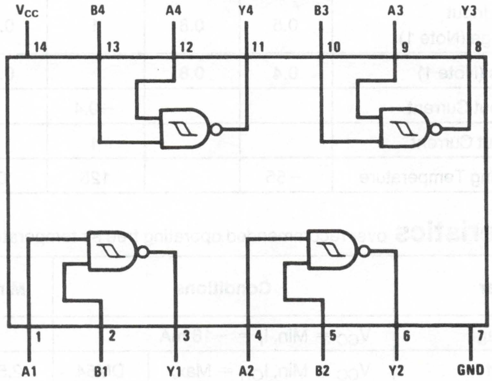
DM54LS132/DM74LS132 Quad 2-Input NAND Gates with Schmitt Trigger Inputs

General Description

This device contains four independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Connection Diagram

Dual-In-Line Package



TL/F/6389–1

Order Number DM54LS132J, DM54LS132W, DM74LS132M or DM74LS132N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS132			DM74LS132			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.5	0.8	1	0.5	0.8	1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, $V_I = V_{T-}$ Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max,	DM54		0.25	0.4	V
		$V_I = V_{T+}$ Max	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, $V_I = V_{T+}$			−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, $V_I = V_{T-}$			−0.18		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			5.9	11	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			8.2	14	mA

Note 1: V_{CC} = 5V

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 2\ k\Omega$				Units
		$C_L = 15\ pF$		$C_L = 50\ pF$		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	5	22	8	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	5	22	10	33	ns

National Semiconductor

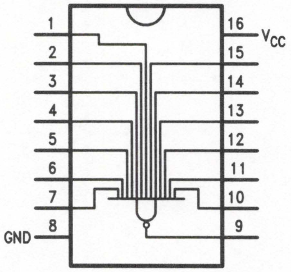
54LS133/DM74LS133
13-Input NAND Gate

General Description

This device contains one, 13-input gate that performs the logic NAND functions.

Connection Diagram

Dual-In-Line Package



TL/F/9818-1

Order Number 54LS133DMQB, 54LS133FMQB, 54LS133LMQB, DM74LS133M or DM74LS133N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for acutal device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS133			DM74LS133			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max, V_{IN} = GND				0.5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max, V_{IN} = Open				1.1	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 2\ k\Omega, C_L = 15\ pF$		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		38	ns

National Semiconductor

54LS136/DM54LS136/DM74LS136 Quad 2-Input Exclusive-OR Gate with Open-Collector Outputs

General Description

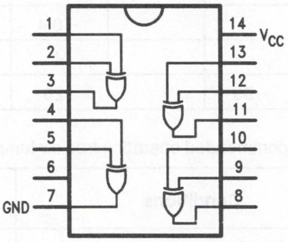
This device contains four independent gates, each of which performs the logic exclusive-OR function.

Features

- Alternate Military/Aerospace device (54LS136) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/9819-1

Order Number 54LS136DMQB, 54LS136FMQB, DM54LS136J, DM54LS136W, DM74LS136M or DM74LS136N
See NS Package Number J14A, M14A, N14A or W14B

Truth Table

Inputs		Output
A	**B**	**Z**
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS136			DM74LS136			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.6	mA
I_{CC}	Supply Current	V_{CC} = Max				10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		23	ns

National Semiconductor

54LS138/DM54LS138/DM74LS138, 54LS139/DM54LS139/DM74LS139 Decoders/Demultiplexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

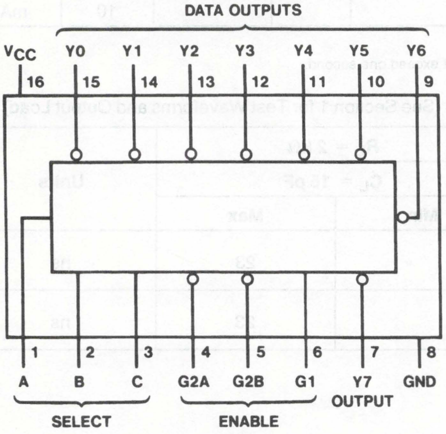
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  Memory decoders
  Data transmission systems
- LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  LS138 21 ns
  LS139 21 ns
- Typical power dissipation
  LS138 32 mW
  LS139 34 mW
- Alternate Military/Aerospace devices (54LS138, 54LS139) are available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

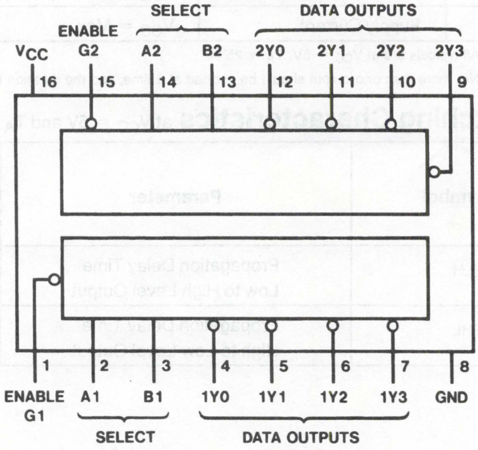
Dual-In-Line Package



TL/F/6391-1

Order Number 54LS138DMQB, 54LS138FMQB, 54LS138LMQB, DM54LS138J, DM54LS138W, DM74LS138M or DM74LS138N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Dual-In-Line Package



TL/F/6391-2

Order Number 54LS139DMQB, 54LS139FMQB, 54LS139LMQB, DM54LS139J, DM54LS139W, DM74LS139M or DM74LS139N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	$-55^{\circ}C$ to $+125^{\circ}C$
DM74LS	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS138			DM74LS138			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS138 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.3	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs enabled and open.

'LS138 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Levels of Delay	R_L = 2 kΩ C_L = 15 pF Min	 C_L = 15 pF Max	 C_L = 50 pF Min	 C_L = 50 pF Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	2		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	2		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	3		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	3		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	2		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	2		24		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	3		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	3		28		40	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS139 Min	DM54LS139 Nom	DM54LS139 Max	DM74LS139 Min	DM74LS139 Nom	DM74LS139 Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS139 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.8	11	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs enabled and open.

'LS139 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output		24		40	ns

Function Tables

LS138

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* G2 = G2A + G2B

H = High Level, L = Low Level, X = Don't Care

LS139

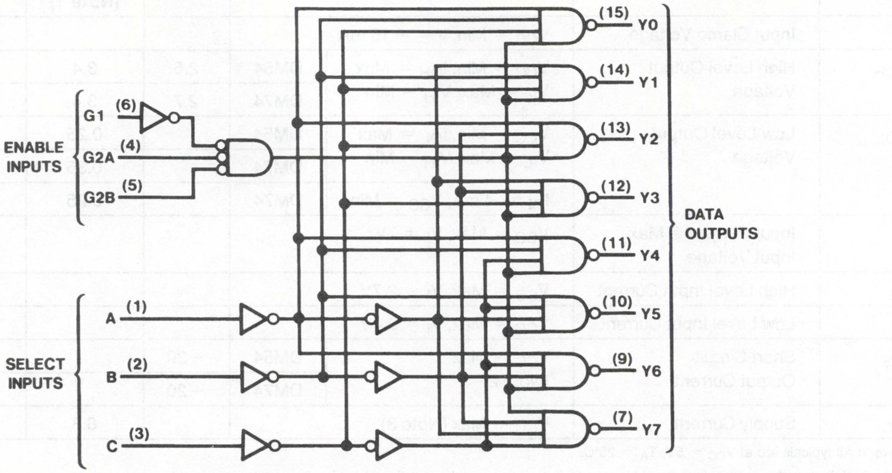
Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don't Care

2

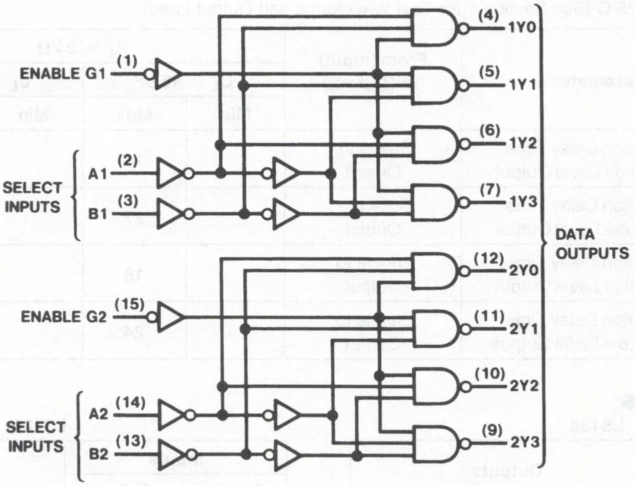
Logic Diagrams

LS138


ENABLE INPUTS
G1
(6)
G2A
(4)
G2B
(5)
SELECT INPUTS
A
(1)
B
(2)
C
(3)
(15) Y0
(14) Y1
(13) Y2
(12) Y3
(11) Y4
(10) Y5
(9) Y6
(7) Y7
DATA OUTPUTS

TL/F/6391-3

LS139


ENABLE G1
(1)
SELECT INPUTS
A1
(2)
B1
(3)
ENABLE G2
(15)
SELECT INPUTS
A2
(14)
B2
(13)
(4) 1Y0
(5) 1Y1
(6) 1Y2
(7) 1Y3
(12) 2Y0
(11) 2Y1
(10) 2Y2
(9) 2Y3
DATA OUTPUTS

TL/F/6391-4

National Semiconductor

54LS151/DM54LS151/DM74LS151
Data Selector/Multiplexer

General Description

This data selector/multiplexer contains full on-chip decoding to select the desired data source. The 'LS151 selects one-of-eight data sources. The 'LS151 has a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output low.

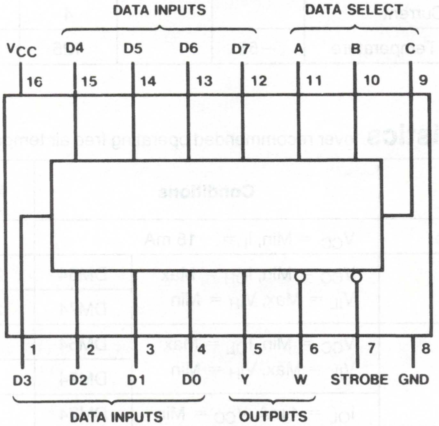
The 'LS151 features complementary W and Y outputs.

Features

- Select one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time data input to W output 12.5 ns
- Typical power dissipation 30 mW
- Alternate Military/Aerospace device (54LS151) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6392-1

Order Number 54LS151DMQB, 54LS151FMQB, 54LS151LMQB, DM54LS151J, DM54LS151W, DM74LS151M or DM74LS151N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care

D0, D1...D7 = the level of the respective D input

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS151			DM74LS151			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

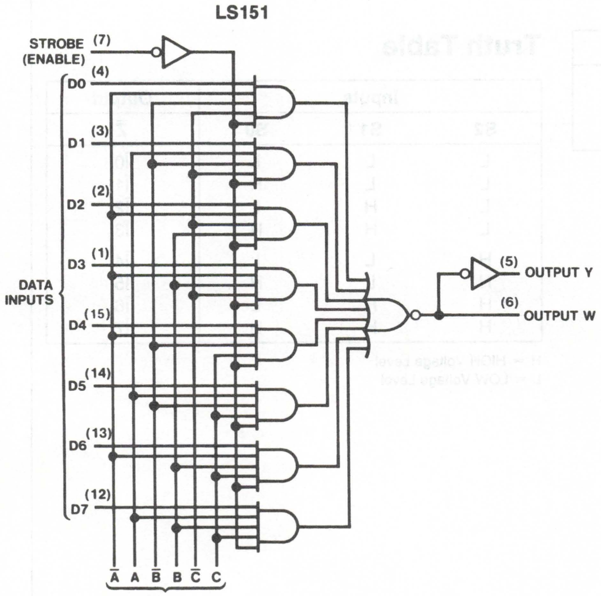
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, strobe and data select inputs at 4.5V, and all other inputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (output)	R_L = 2 kΩ C_L = 15 pF Min	 Max	 C_L = 50 pF Min	 Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Select (4 Levels) to Y		43		46	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select (4 Levels) to Y		30		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select (3 Levels) to W		23		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select (3 Levels) to W		32		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		42		44	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		32		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to W		24		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to W		30		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D0 thru D7 to Y		32		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D0 thru D7 to Y		26		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D0 thru D7 to W		21		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D0 thru D7 to W		20		27	ns

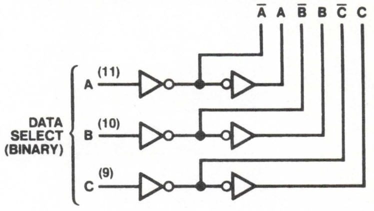
Logic Diagram



TL/F/6392–2

See Address Buffers to the Right

Address Buffers for 54LS151/74LS151



TL/F/6392–3

National Semiconductor

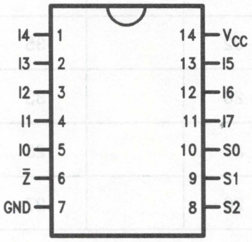
54LS152
8-Input Multiplexer

General Description

The 54LS152 is a high speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The 54LS152 can be used as a universal function generator to generate any logic function of four variables. It is supplied in Flatpak only; for Dual-In-Line Package applications use the 'LS151.

Connection Diagram

Dual-In-Line Package

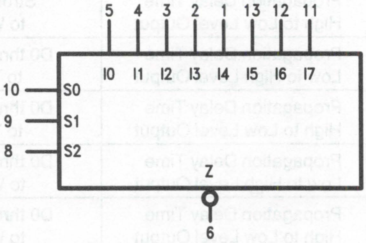


I4 1
I3 2
I2 3
I1 4
I0 5
$\overline{Z}$ 6
GND 7
14 V_{CC}
13 I5
12 I6
11 I7
10 S0
9 S1
8 S2

TL/F/10206-1

Order Number 54LS152FMQB
See NS Package Number W14B

Logic Symbol



5
4
3
2
1
13
12
11
I0
I1
I2
I3
I4
I5
I6
I7
10
S0
9
S1
8
S2
Z
6

TL/F/10206-2

V_{CC} = Pin 14
GND = Pin 7

Pin Names	Description
I0–I7	Data Inputs
S0–S2	Select Inputs
$\overline{Z}$	Inverted Data Outputs

Truth Table

Inputs			Output
S2	S1	S0	$\overline{Z}$
L	L	L	$\overline{I0}$
L	L	H	$\overline{I1}$
L	H	L	$\overline{I2}$
L	H	H	$\overline{I3}$
H	L	L	$\overline{I4}$
H	L	H	$\overline{I5}$
H	H	L	$\overline{I6}$
H	H	H	$\overline{I7}$

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54LS	−55°C to +25°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS152			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			4.0	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.5	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10.0V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	−30		−400	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics V_{CC} = +5.0V, T_A = +25°C (See Section 1 for test waveforms and output load)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay, Sn to $\overline{Z}$		23 32	ns
t_{PLH} t_{PHL}	Propagation Delay, In to $\overline{Z}$		21 20	ns

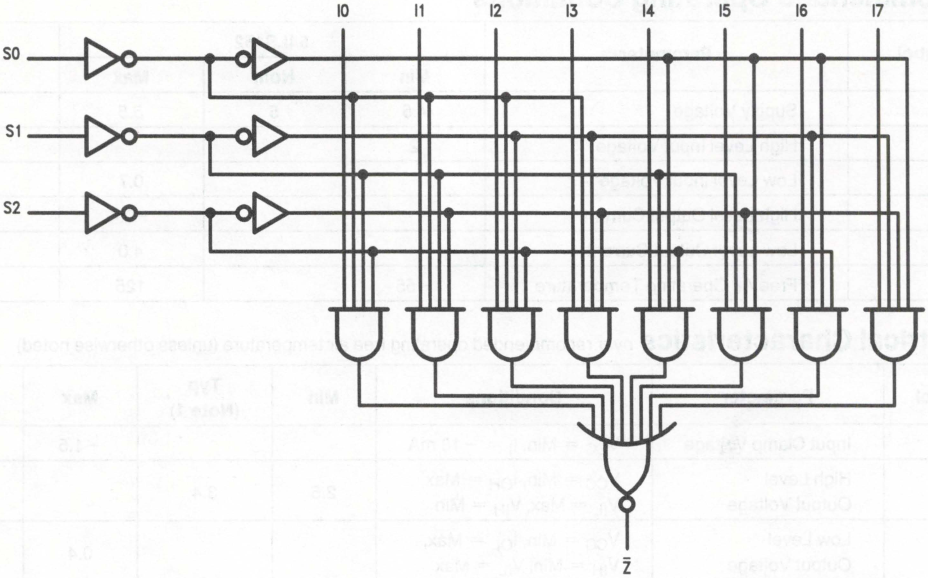
Functional Description

The 54LS152 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S0, S1, S2. The logic function provided at the output is:

$$Z = (I0 \bullet \overline{S0} \bullet \overline{S1} \bullet \overline{S2} + I1 \bullet S0 \bullet \overline{S1} \bullet \overline{S2} + I2 \bullet \overline{S0} \bullet S1 \bullet \overline{S2} + I3 \bullet S0 \bullet S1 \bullet \overline{S2}$$
$$+ I4 \bullet \overline{S0} \bullet \overline{S1} \bullet S2 + I5 \bullet S0 \bullet \overline{S1} \bullet S2 + I6 \bullet \overline{S0} \bullet S1 \bullet S2 + I7 \bullet S0 \bullet S1 \bullet S2).$$

The 54LS152 provides the ability, in one package, to select from eight sources of data or control information.

Logic Diagram



TL/F/10206–3

National Semiconductor

54LS153/DM54LS153/DM74LS153 Dual 4-Line to 1-Line Data Selectors/Multiplexers

General Description

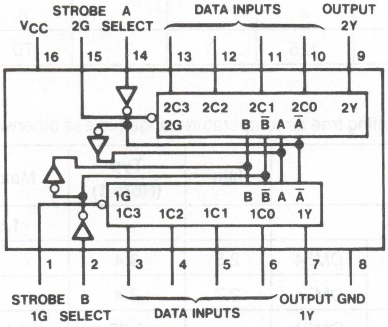
Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

- Permits multiplexing from N lines to 1 line
- Performs at parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low impedance, totem pole outputs
- Typical average propagation delay times
  - From data 14 ns
  - From strobe 19 ns
  - From select 22 ns
- Typical power dissipation 31 mW
- Alternate Military/Aerospace device (54LS153) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

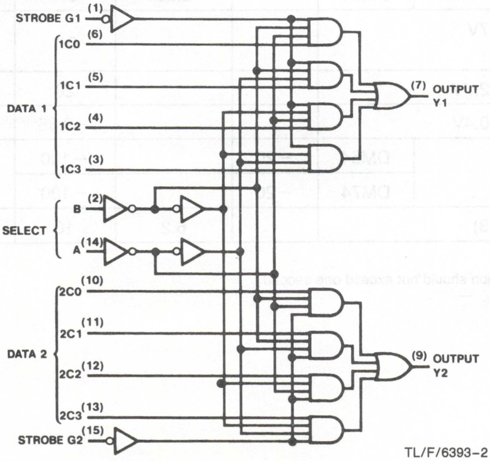
Dual-In-Line Package


STROBE 2G
A SELECT
DATA INPUTS
OUTPUT 2Y
VCC
16
15
14
13
12
11
10
9
2C3
2C2
2C1
2C0
2Y
2G
B
B̄
A
Ā
1G
B
B̄
A
Ā
1C3
1C2
1C1
1C0
1Y
1
2
3
4
5
6
7
8
STROBE 1G
B SELECT
DATA INPUTS
OUTPUT 1Y
GND

TL/F/6393–1

Order Number 54LS153DMQB, 54LS153FMQB, 54LS153LMQB, DM54LS153J, DM54LS153W, DM74LS153M or DM74LS153N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Logic Diagram


STROBE G1
(1)
(6)
1C0
(5)
1C1
DATA 1
(4)
1C2
(3)
1C3
(7) OUTPUT Y1
(2)
B
SELECT
(14)
A
(10)
2C0
(11)
2C1
DATA 2
(12)
2C2
(13)
2C3
(9) OUTPUT Y2
(15)
STROBE G2

TL/F/6393–2

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS153			DM74LS153			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.2	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25° C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all other inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) to (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		15		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		26		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		29		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		38		45	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		32		40	ns

National Semiconductor

DM54LS154/DM74LS154 4-Line to 16-Line Decoders/Demultiplexers

General Description

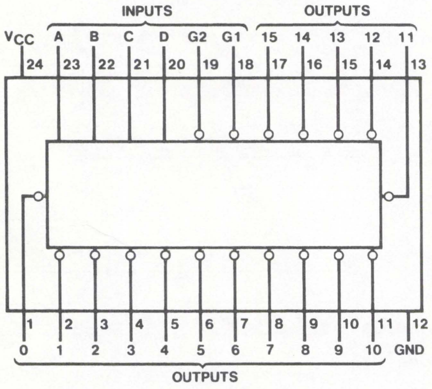
Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay
  3 levels of logic 23 ns
  Strobe 19 ns
- Typical power dissipation 45 mW

Connection and Logic Diagrams

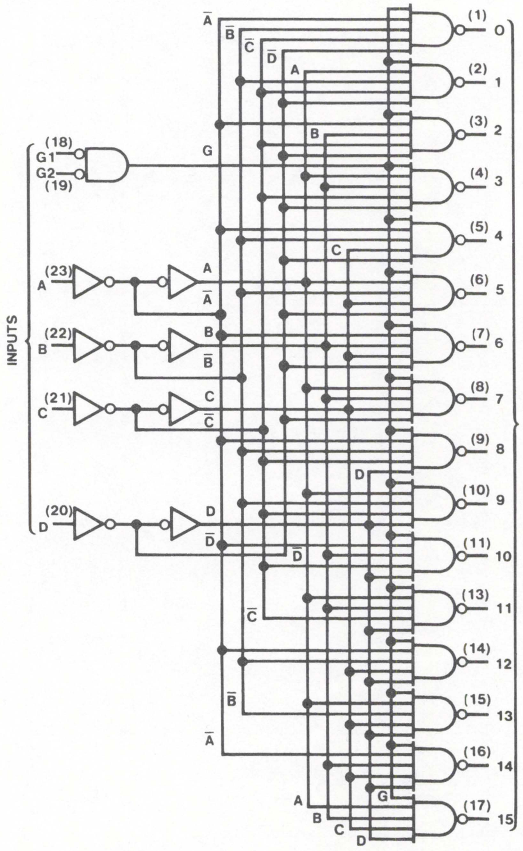
Dual-In-Line Package



INPUTS
OUTPUTS
VCC
A
B
C
D
G2
G1
15
14
13
12
11
24
23
22
21
20
19
18
17
16
15
14
13
1
2
3
4
5
6
7
8
9
10
11
12
0
1
2
3
4
5
6
7
8
9
10
GND
OUTPUTS

TL/F/6394–1

Order Number DM54LS154J, DM74LS154WM or DM74LS154N
See NS Package Number J24A, M24B or N24A



(18)
G1
G2
(19)
G
(23)
A
(22)
B
(21)
C
(20)
D
INPUTS
A
$\overline{A}$
B
$\overline{B}$
C
$\overline{C}$
D
$\overline{D}$
$\overline{A}$
$\overline{B}$
$\overline{C}$
$\overline{D}$
A
B
C
D
$\overline{D}$
$\overline{C}$
$\overline{B}$
$\overline{A}$
A
B
C
D
G
(1) 0
(2) 1
(3) 2
(4) 3
(5) 4
(6) 5
(7) 6
(8) 7
(9) 8
(10) 9
(11) 10
(13) 11
(14) 12
(15) 13
(16) 14
(17) 15
OUTPUTS

TL/F/6394–2

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS154			DM74LS154			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9	14	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		30		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		20		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		25		35	ns

Function Table

Inputs						Outputs															
G1	**G2**	**D**	**C**	**B**	**A**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

National Semiconductor

54LS155/DM54LS155/DM74LS155, 54LS156/DM54LS156/DM74LS156 Dual 2-Line to 4-Line Decoders/Demultiplexers

General Description

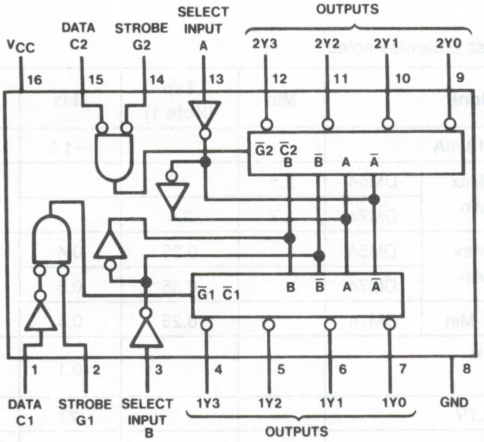
These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demultiplexer, without external gating. Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

Features

- Applications:
  Dual 2-to-4-line decoder
  Dual 1-to-4-line demultiplexer
  3-to-8-line decoder
  1-to-8-line demultiplexer
- Individual strobes simplify cascading for decoding or demultiplexing larger words
- Input clamping diodes simplify system design
- Choice of outputs:
  Totem-pole (LS155)
  Open-collector (LS156)
- Alternate Military/Aerospace device (54LS155/156) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram and Function Tables

Dual-In-Line Package



TL/F/6395–1

Order Number 54LS155DMQB, 54LS155FMQB, 54LS155LMQB, DM54LS155J, DM54LS155W, DM74LS155M, DM74LS155N, 54LS156DMQB, 54LS156FMQB, DM54LS156J, DM54LS156W, DM74LS156M or DM74LS156N
See NS Package Number E20A, J16A, M16A, N16E or W16A

3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer

Inputs				Outputs							
Select			Strobe Or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

2-Line-to-4-Line Decoder or 1-Line-to-4-Line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

†C = inputs C1 and C2 connected together
‡G = inputs G1 and G2 connected together
H = high level, L = low level, X = don't care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS155			DM74LS155			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS155 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.1	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25° C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, A,B, and C1 inputs at 4.5V, and C2, G1, and G2 inputs grounded.

’LS155 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ, C_L = 15 pF Min	R_L = 2 kΩ, C_L = 15 pF Max	R_L = 2 kΩ, C_L = 50 pF Min	R_L = 2 kΩ, C_L = 50 pF Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C2, G1 or G2 to Y		18		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C2, G1 or G2 to Y		27		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to Y		18		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to Y		27		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C1 to Y		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C1 to Y		27		35	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS156 Min	DM54LS156 Nom	DM54LS156 Max	DM74LS156 Min	DM74LS156 Nom	DM74LS156 Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

’LS156 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			6.1	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25° C.

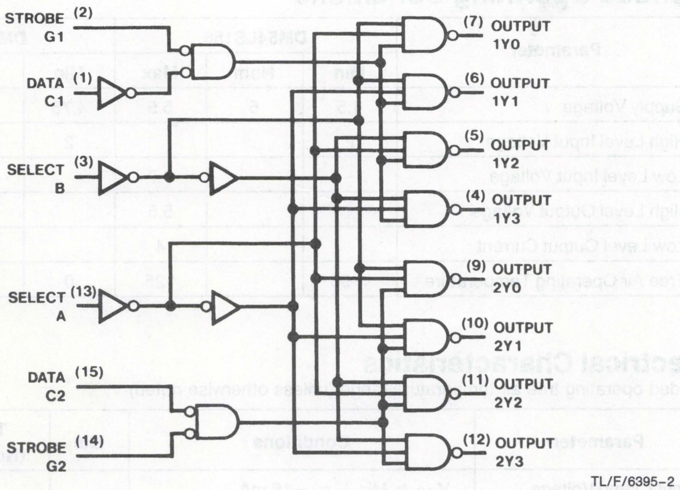
Note 2: I_{CC} is measured with all outputs open, A, B, and C1 inputs at 4.5V, and C2, G1, and G2 grounded.

'LS156 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C2, G1 or G2 to Y		28		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C2, G1 or G2 to Y		33		43	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to Y		28		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to Y		33		43	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C1 to Y		28		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C1 to Y		34		43	ns

Logic Diagram


STROBE G1 (2)
DATA C1 (1)
SELECT B (3)
SELECT A (13)
DATA C2 (15)
STROBE G2 (14)
(7) OUTPUT 1Y0
(6) OUTPUT 1Y1
(5) OUTPUT 1Y2
(4) OUTPUT 1Y3
(9) OUTPUT 2Y0
(10) OUTPUT 2Y1
(11) OUTPUT 2Y2
(12) OUTPUT 2Y3

TL/F/6395-2

National Semiconductor

54LS157/DM54LS157/DM74LS157, 54LS158/DM54LS158/DM74LS158 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The LS157 presents true data whereas the LS158 presents inverted data to minimize propagation delay time.

Applications

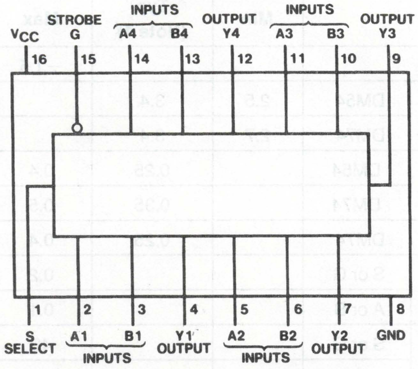
- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Features

- Buffered inputs and outputs
- Typical Propagation Time
  LS157 9 ns
  LS158 7 ns
- Typical Power Dissipation
  LS157 49 mW
  LS158 24 mW
- Alternate Military/Aerospace device (54LS157, 54LS158) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

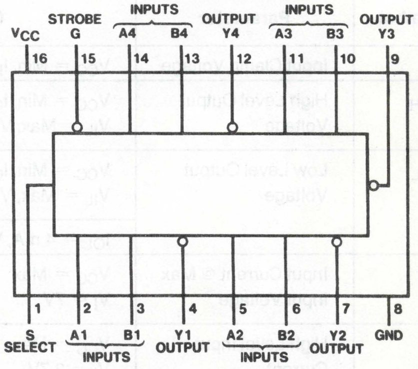
Dual-In-Line Package


VCC
STROBE G
INPUTS
A4
B4
OUTPUT Y4
INPUTS
A3
B3
OUTPUT Y3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
S SELECT
A1
B1
INPUTS
Y1 OUTPUT
A2
B2
INPUTS
Y2 OUTPUT
GND

TL/F/6396-1

Order Number 54LS157DMQB, 54LS157FMQB, 54LS157LMQB, DM54LS157J, DM54LS157W, DM74LS157M or DM74LS157N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Dual-In-Line Package


VCC
STROBE G
INPUTS
A4
B4
OUTPUT Y4
INPUTS
A3
B3
OUTPUT Y3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
S SELECT
A1
B1
INPUTS
Y1 OUTPUT
A2
B2
INPUTS
Y2 OUTPUT
GND

TL/F/6396-2

Order Number 54LS158DMQB, 54LS158FMQB, 54LS158LMQB, DM54LS158J, DM54LS158W, DM74LS158M or DM74LS158N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Inputs				Output Y	
Strobe	**Select**	**A**	**B**	**LS157**	**LS158**
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS157			DM74LS157			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS157 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	S or G			0.2	mA
			A or B			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	S or G			40	µA
			A or B			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	S or G			−0.8	mA
			A or B			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9.7	16	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

'LS157 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		14		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		14		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		21		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		23		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		27		32	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS158			DM74LS158			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS158 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	S or G			0.2	mA
			A or B			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	S or G			40	μA
			A or B			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	S or G			−0.8	mA
			A or B			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4.8	8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

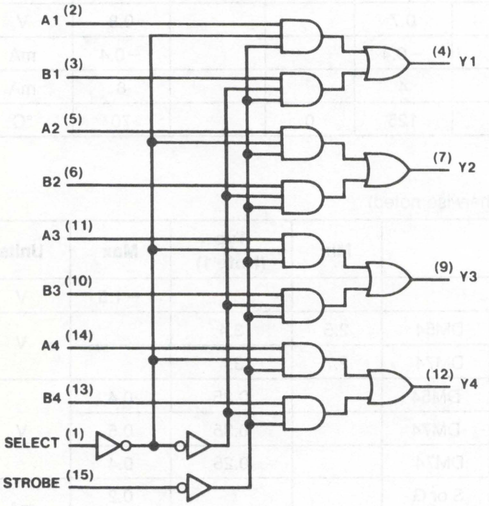
'LS158 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		12		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		12		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		17		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		18		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		24		36	ns

Logic Diagrams

LS157


A1 (2)
B1 (3)
A2 (5)
B2 (6)
A3 (11)
B3 (10)
A4 (14)
B4 (13)
SELECT (1)
STROBE (15)
(4) Y1
(7) Y2
(9) Y3
(12) Y4

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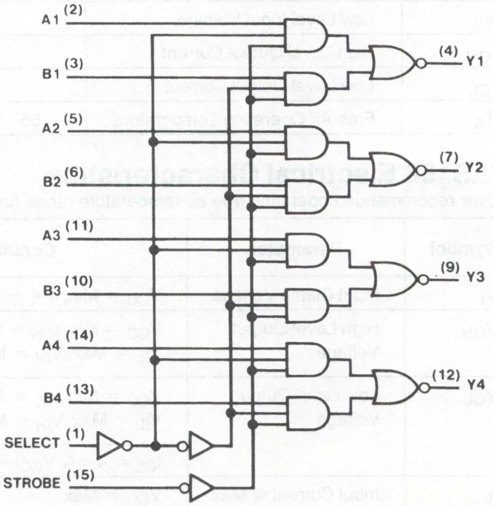
LS158


A1 (2)
B1 (3)
A2 (5)
B2 (6)
A3 (11)
B3 (10)
A4 (14)
B4 (13)
SELECT (1)
STROBE (15)
(4) Y1
(7) Y2
(9) Y3
(12) Y4

TL/F/6396-4

National Semiconductor

54LS160A/DM74LS160A, 54LS162A/DM74LS162A Synchronous Presettable BCD Decade Counters

General Description

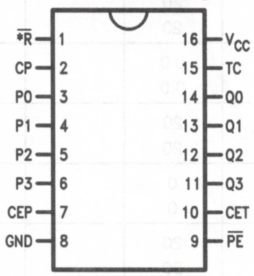
The 'LS160 and 'LS162 are high speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'LS160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'LS162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock.

Features

- Synchronous counting and loading
- High speed synchronous expansion
- Typical count rate of 35 MHz
- Fully edge triggered

Connection Diagram

Dual-In-Line Package



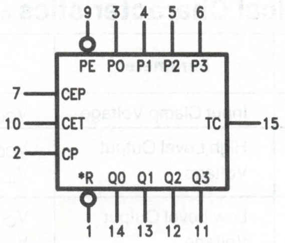
TL/F/10177-1

*$\overline{MR}$ for 'LS160
*$\overline{SR}$ for 'LS162

Order Number 54LS160ADMQB, 54LS160AFMQB, 54LS160ALMQB, 54LS162ADMQB, 54LS162AFMQB, 54LS162ALMQB, DM74LS160AM, DM74LS160AN, DM74LS162AM or DM74LS162AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('160)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('162)	Synchronous Reset Input (Active LOW)
P0–P3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q0–Q3	Flip-Flop Outputs
TC	Terminal Count Output

Logic Symbol



TL/F/10177-2

V_{CC} = Pin 16
GND = Pin 8
*$\overline{MR}$ for 'LS160
*$\overline{SR}$ for 'LS162

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS160A/162A			DM74LS160A/162A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP	20 20			20 20			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	0.0 0.0			0.0 0.0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ to CP	20 20			20 20			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0			0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW CEP, CET or $\overline{SR}$ to CP	20 20			20 20			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW CEP, CET or $\overline{SR}$ to CP	0 0			0 0			ns
$t_w(H)$ $t_w(L)$	CP Pulse Width, HIGH or LOW	15 25			15 25			ns
$t_w(L)$	$\overline{MR}$ Pulse Width LOW ('160)	15			15			ns
t_{rec}	Recovery Time $\overline{MR}$ to CP ('160)	20			20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V Inputs $\overline{PE}$, CET Inputs				0.1 0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V Inputs $\overline{PE}$, CET Inputs				20 40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V Inputs	54LS DM74			−0.4 −1.6	mA
		$\overline{PE}$, CET Inputs				−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max, $\overline{PE}$ = GND CP = ⌐, Other Inputs = 4.5V				31	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max, V_{IN} = GND CP = ⌐				31	mA

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	$R_L = 2\ k\Omega$ $C_L = 15\ pF$		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	25		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to TC		25 21	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		20 27	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		24 27	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC		14 14	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('160)		28	ns

Functional Description

The 'LS160 and 'LS162 count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The '161 and '163 count modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 'LS160) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('LS160), synchronous reset ('LS162), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, 'LS160), Synchronous Reset ($\overline{SR}$, 'LS162), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('LS160) or $\overline{SR}$ ('LS162) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'LS160A and 'LS162A use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Functional Description (Continued)

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state (9 for the decade counters, 15 for the binary counters). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. These two schemes are shown in the 9310 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the decade counters of the 'LS160, 'LS162, the TC output is fully decoded and can only be HIGH in state 9.

LOGIC EQUATIONS:

Count Enable = $CEP \bullet CET \bullet PE$

TC = $Q0 \bullet \overline{Q}1 \bullet \overline{Q}2 \bullet Q3 \bullet CET$

Mode Select Table

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (_/‾)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the 'LS162

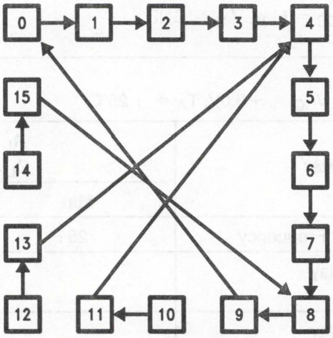
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

State Diagrams

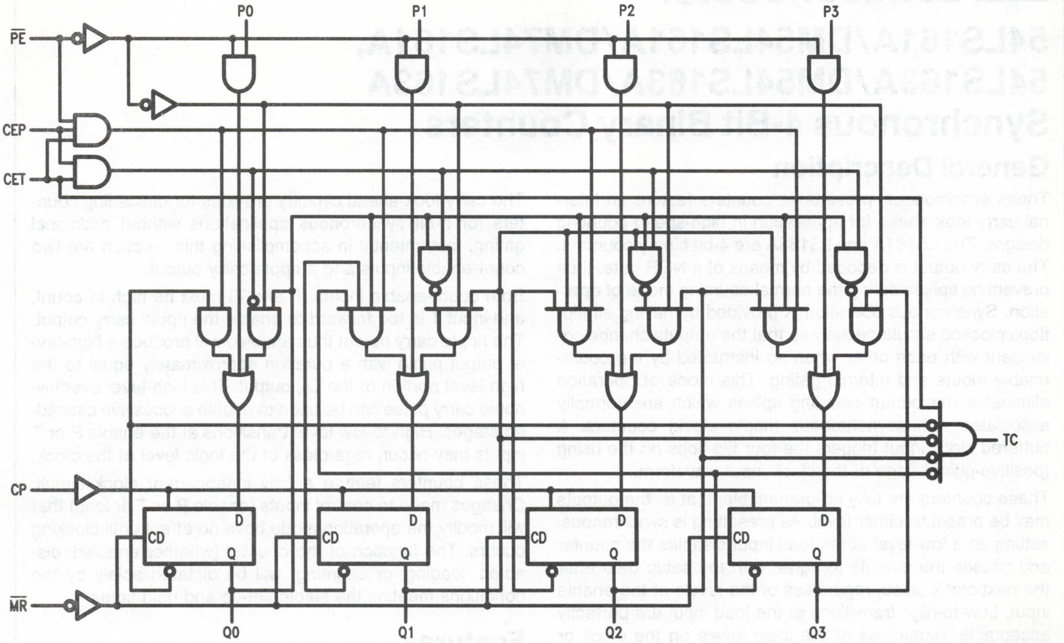
'LS160, 'LS162



TL/F/10177-5

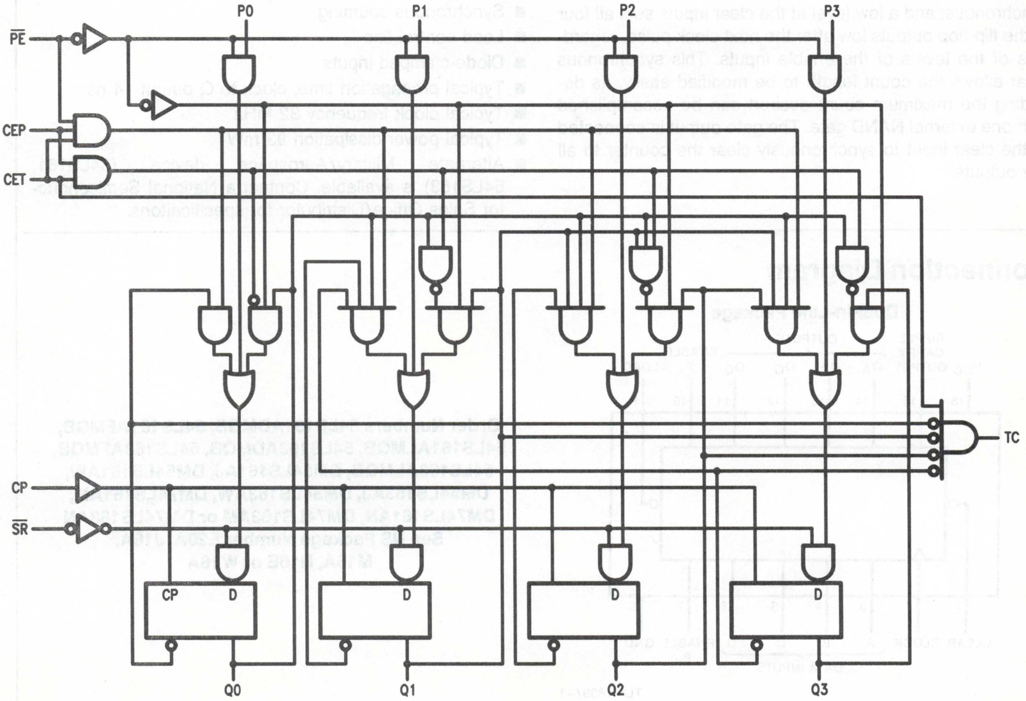
Logic Diagrams

'LS160


P0
P1
P2
P3
PE
CEP
CET
TC
CP
CD
D
Q
CD
D
Q
CD
D
Q
CD
D
Q
MR
Q0
Q1
Q2
Q3

TL/F/10177-3

'LS162


P0
P1
P2
P3
PE
CEP
CET
TC
CP
SR
CP
D
D
D
D
Q0
Q1
Q2
Q3

TL/F/10177-4

National Semiconductor

54LS161A/DM54LS161A/DM74LS161A, 54LS163A/DM54LS163A/DM74LS163A Synchronous 4-Bit Binary Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The LS161A and LS163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable, regardless of the logic levels on the clock or enable inputs. The clear function for the LS161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low, regardless of the levels of clock, load, or enable inputs. The clear function for the LS163A is synchronous; and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output.

Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur, regardless of the logic level of the clock.

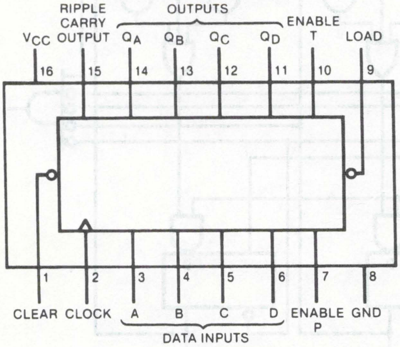
These counters feature a fully independent clock circuit. Changes made to control inputs (enable P or T or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical propagation time, clock to Q output 14 ns
- Typical clock frequency 32 MHz
- Typical power dissipation 93 mW
- Alternate Military/Aerospace device (54LS161, 54LS163) is available. Contact a National Semiconductor Sales Office/Distributor for specificaitons.

Connection Diagram

Dual-In-Line Package



TL/F/6397-1

Order Numbers 54LS161ADMQB, 54LS161AFMQB, 54LS161ALMQB, 54LS163ADMQB, 54LS163AFMQB, 54LS163ALMQB, DM54LS161AJ, DM54LS161AW, DM54LS163AJ, DM54LS163AW, DM74LS161AM, DM74LS161AN, DM74LS163AM or DM74LS163AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS161A			DM74LS161A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Pulse Width (Note 1)	Clock	20	6		20	6		ns
		Clear	20	9		20	9		
	Pulse Width (Note 2)	Clock	25			25			ns
		Clear	25			25			
t_{SU}	Setup Time (Note 1)	Data	20	8		20	8		ns
		Enable P	25	17		25	17		
		Load	25	15		25	15		
	Setup Time (Note 2)	Data	20			20			ns
		Enable P	30			30			
		Load	30			30			
t_H	Hold Time (Note 1)	Data	0	−3		0	−3		ns
		Others	0	−3		0	−3		
	Hold Time (Note 2)	Data	5			5			ns
		Others	5			5			
t_{REL}	Clear Release Time (Note 1)		20			20			ns
	Clear Release Time (Note 2)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15\ pF$, $R_L = 2\ k\Omega$, $T_A = 25°C$ and $V_{CC} = 5.5V$.

Note 2: $C_L = 50\ pF$, $R_L = 2\ k\Omega$, $T_A = 25°C$ and $V_{CC} = 5.5V$.

'LS161 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	Enable T			0.2	mA
			Clock			0.2	
			Load			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Enable T			40	μA
			Clock			40	
			Load			40	
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Enable T			−0.8	mA
			Clock			−0.8	
			Load			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			18	31	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)			19	32	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.

Note 4: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

'LS161 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		30		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load High)		22		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load High)		27		38	ns

'LS161 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load) (Continued)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load Low)		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load Low)		29		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		15		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		35		45	ns

Recommended Operating Conditions

Symbol	Parameter		DM54LS163A			DM74LS163A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Pulse Width (Note 1)	Clock	20	6		20	6		ns
		Clear	20	9		20	9		
	Pulse Width (Note 2)	Clock	25			25			ns
		Clear	25			25			
t_{SU}	Setup Time (Note 1)	Data	20	8		20	8		ns
		Enable P	25	17		25	17		
		Load	25	15		25	15		
	Setup Time (Note 2)	Data	20			20			ns
		Enable P	30			30			
		Load	30			30			
t_H	Hold Time (Note 1)	Data	0	−3		0	−3		ns
		Others	0	−3		0	−3		
	Hold Time (Note 2)	Data	5			5			ns
		Others	5			5			
t_{REL}	Clear Release Time (Note 1)		20			20			ns
	Clear Release Time (Note 2)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

'LS163 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	Enable T			0.2	mA
			Clock, Clear			0.2	
			Load			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Enable T			40	µA
			Load			40	
			Clock, Clear			40	
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Enable T			−0.8	mA
			Clock, Clear			−0.8	
			Load			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			18	31	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)			18	32	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.

Note 4: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

'LS163 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		30		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load High)		22		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load High)		27		38	ns

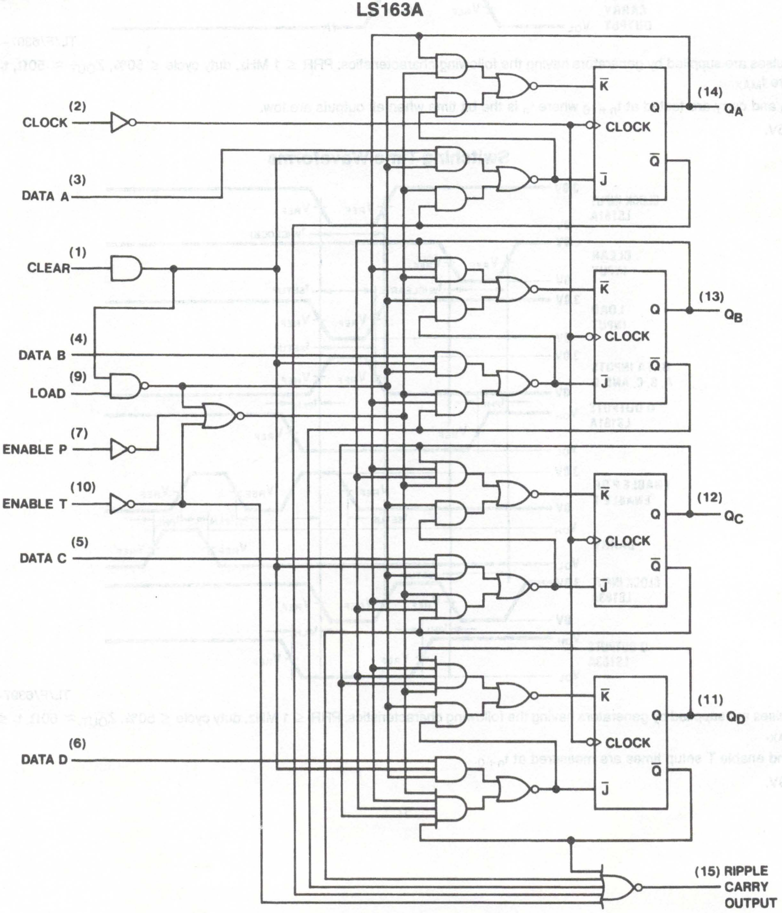
'LS163 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load) (Continued)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load Low)		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load Low)		29		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		15		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q (Note 1)		35		45	ns

Note 1: The propagation delay clear to output is measured from the clock input transition.

Logic Diagram

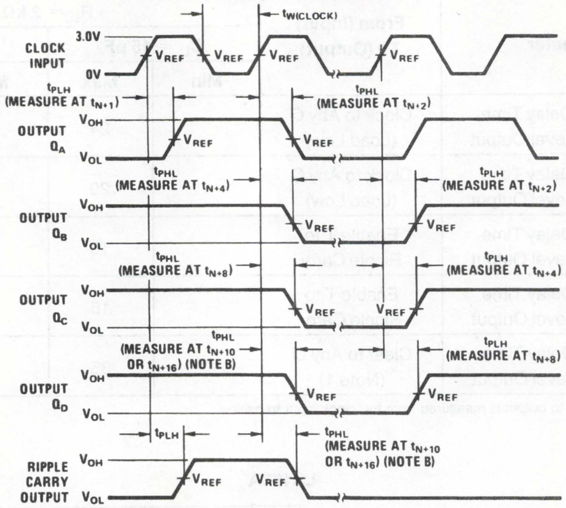

LS163A
(2) CLOCK
(3) DATA A
(1) CLEAR
(4) DATA B
(9) LOAD
(7) ENABLE P
(10) ENABLE T
(5) DATA C
(6) DATA D
$\overline{K}$
Q
CLOCK
$\overline{Q}$
J
(14) Q_A
(13) Q_B
(12) Q_C
(11) Q_D
(15) RIPPLE CARRY OUTPUT

TL/F/6397-2

The LS161A is similar, however, the clear buffer is connected directly to the flip flops.

Parameter Measurement Information

Switching Time Waveforms


t_W(CLOCK)
CLOCK INPUT
3.0V
0V
V_REF
t_PLH (MEASURE AT t_N+1)
t_PHL (MEASURE AT t_N+2)
OUTPUT Q_A
V_OH
V_OL
t_PHL (MEASURE AT t_N+4)
t_PLH (MEASURE AT t_N+2)
OUTPUT Q_B
t_PHL (MEASURE AT t_N+8)
t_PLH (MEASURE AT t_N+4)
OUTPUT Q_C
t_PHL (MEASURE AT t_N+10 OR t_N+16) (NOTE B)
t_PLH (MEASURE AT t_N+8)
OUTPUT Q_D
t_PLH
t_PHL (MEASURE AT t_N+10 OR t_N+16) (NOTE B)
RIPPLE CARRY OUTPUT

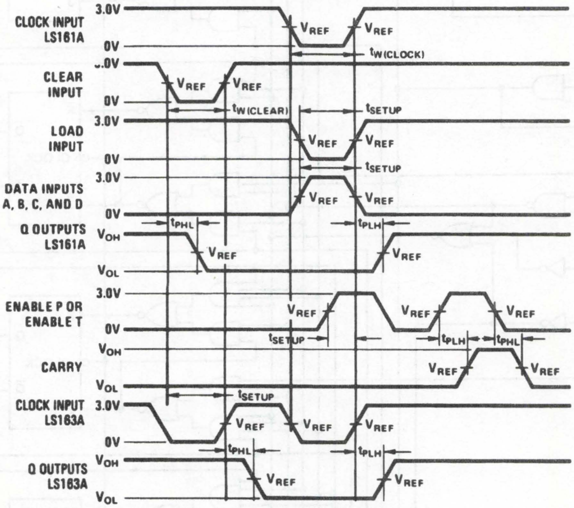
TL/F/6397-3

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \le 10$ ns, $t_f \le 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+16} where t_n is the bit time when all outputs are low.

Note C: $V_{REF} = 1.5V$.

Switching Time Waveforms


CLOCK INPUT LS161A
3.0V
0V
V_REF
t_W(CLOCK)
CLEAR INPUT
t_W(CLEAR)
t_SETUP
LOAD INPUT
DATA INPUTS A, B, C, AND D
Q OUTPUTS LS161A
V_OH
V_OL
t_PHL
t_PLH
ENABLE P OR ENABLE T
t_SETUP
CARRY
CLOCK INPUT LS163A
Q OUTPUTS LS163A

TL/F/6397-4

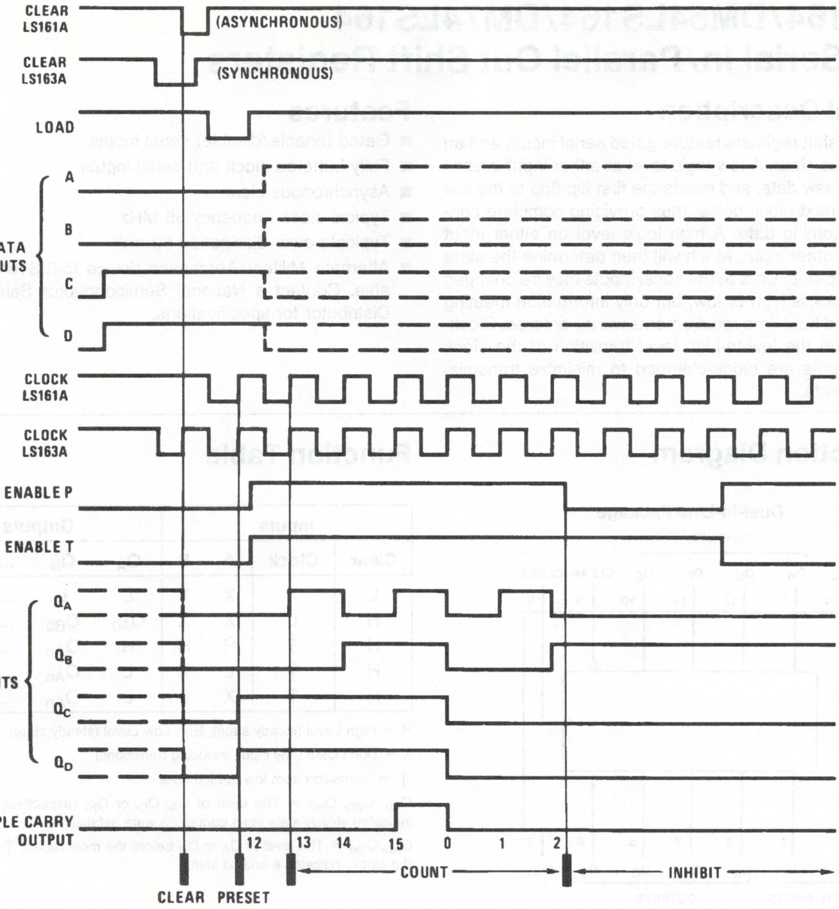
Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \le 6$ ns, $t_f \le 6$ ns. Vary PRR to measure f_{MAX}.

Note B: Enable P and enable T setup times are measured at t_{n+0}.

Note C: $V_{REF} = 1.3V$.

Timing Diagram

LS161A, LS163A Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences


CLEAR LS161A
(ASYNCHRONOUS)
CLEAR LS163A
(SYNCHRONOUS)
LOAD
DATA INPUTS
A
B
C
D
CLOCK LS161A
CLOCK LS163A
ENABLE P
ENABLE T
OUTPUTS
Q_A
Q_B
Q_C
Q_D
RIPPLE CARRY OUTPUT
12
13
14
15
0
1
2
COUNT
INHIBIT
CLEAR
PRESET

TL/F/6397–5

Sequence:

(1) Clear outputs to zero

(2) Preset to binary twelve

(3) Count to thirteen, fourteen, fifteen, zero, one, and two

(4) Inhibit

National Semiconductor

54LS164/DM54LS164/DM74LS164
8-Bit Serial In/Parallel Out Shift Registers

General Description

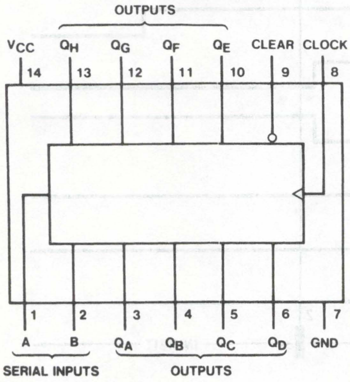
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 80 mW
- Alternate Military/Aerospace device (54LS164) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package


OUTPUTS
V_{CC}
Q_H
Q_G
Q_F
Q_E
CLEAR
CLOCK
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A
B
Q_A
Q_B
Q_C
Q_D
GND
SERIAL INPUTS
OUTPUTS

TL/F/6398-1

Order Number 54LS164DMQB, 54LS164FMQB, 54LS164LMQB, DM54LS164J, DM54LS164W, DM74LS164M or DM74LS164N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs			
Clear	**Clock**	**A**	**B**	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

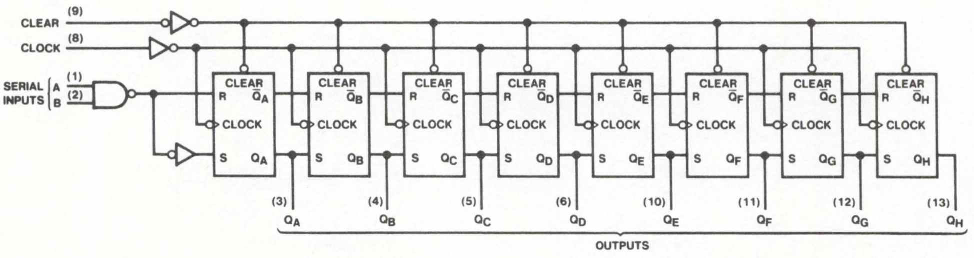
X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Logic Diagram


CLEAR
(9)
CLOCK
(8)
SERIAL INPUTS
A
B
(1)
(2)
CLEAR
R
S
CLOCK
$\overline{Q}_A$
Q_A
$\overline{Q}_B$
Q_B
$\overline{Q}_C$
Q_C
$\overline{Q}_D$
Q_D
$\overline{Q}_E$
Q_E
$\overline{Q}_F$
Q_F
$\overline{Q}_G$
Q_G
$\overline{Q}_H$
Q_H
(3)
(4)
(5)
(6)
(10)
(11)
(12)
(13)
OUTPUTS

TL/F/6398-2

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" tables will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS164			DM74LS164			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 4)		0		25	0		25	MHz
t_W	Pulse Width (Note 4)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time (Note 4)		17			17			ns
t_H	Data Hold Time (Note 4)		5			5			ns
t_{REL}	Clear Release Time (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			16	27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

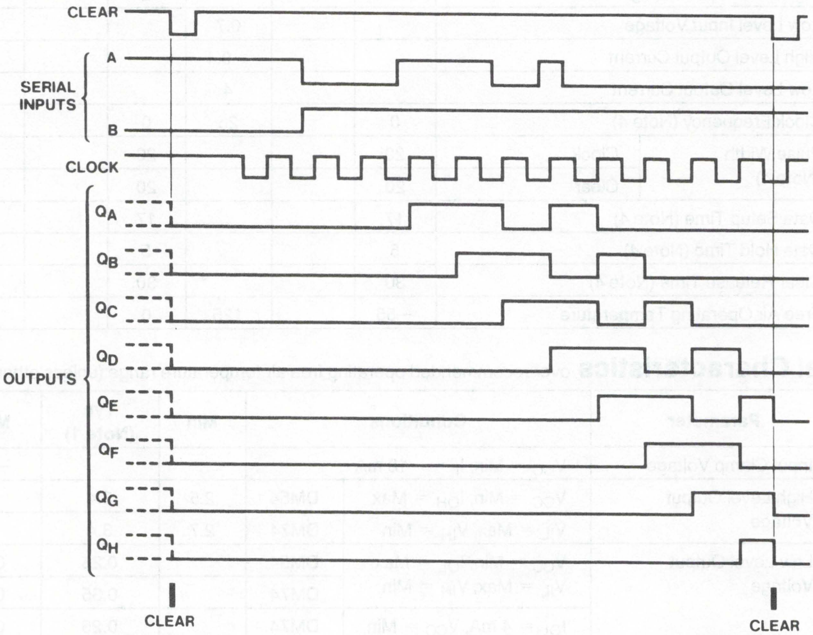
Note 3: I_{CC} is measured with all outputs open, the SERIAL input grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ C_L = 15 pF Min	C_L = 15 pF Max	C_L = 50 pF Min	C_L = 50 pF Max	Units
f_{MAX}	Maximum Clock Frequency		25				MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		32		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		36		45	ns

Timing Diagram


CLEAR
SERIAL INPUTS
A
B
CLOCK
OUTPUTS
Q_A
Q_B
Q_C
Q_D
Q_E
Q_F
Q_G
Q_H
CLEAR
CLEAR

TL/F/6398–3

National Semiconductor

54LS165/DM74LS165 8-Bit Parallel In/Serial Output Shift Registers

General Description

This device is an 8-bit serial shift register which shifts data in the direction of Q_A toward Q_H when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high.

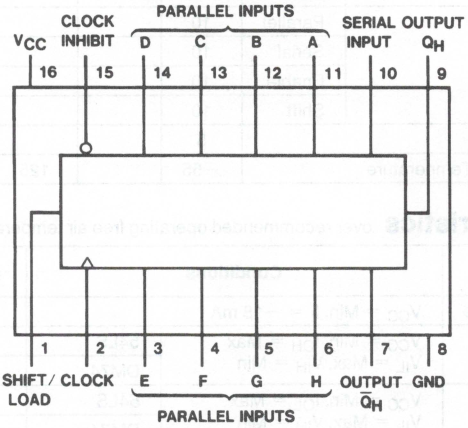
Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

Features

- Complementary outputs
- Direct overriding (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion
- Typical frequency 35 MHz
- Typical power dissipation 105 mW

Connection Diagram

Dual-In-Line Package



TL/F/6399–1

Order Number 54LS165DMQB, 54LS165FMQB, DM74LS165WM or DM74LS165N
See NS Package Number J16A, M16B, N16E or W16A

Function Table

Inputs					Internal Outputs		Output Q_H
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low-to-high level

a...h = The level of steady-state input at inputs A through H, respectively.

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		54LS165			DM74LS165			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)				30	0		25	MHz
f_{CLK}	Clock Frequency (Note 2)					0		20	MHz
t_W	Pulse Width (Note 2)	Clock	18			25			ns
		Load	15			15			
t_{SU}	Setup Time (Note 6)	Parallel	10			10			ns
		Serial	10			20			
		Enable	10			30			
		Shift	10			45			
t_H	Hold Time (Note 6)		5			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V (DM74) V_I = 10V (54LS)	Shift/Load			0.3	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Shift/Load			60	µA
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Shift/Load			−1.2	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			21	36	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V

Note 3: All typicals are at V_{CC} = 5V, T_A = 25° C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: With all outputs open, clock inhibit and shift/load at 4.5V, and a clock pulse applied to the CLOCK input, I_{CC} is measured first with the parallel inputs at 4.5V, then again grounded.

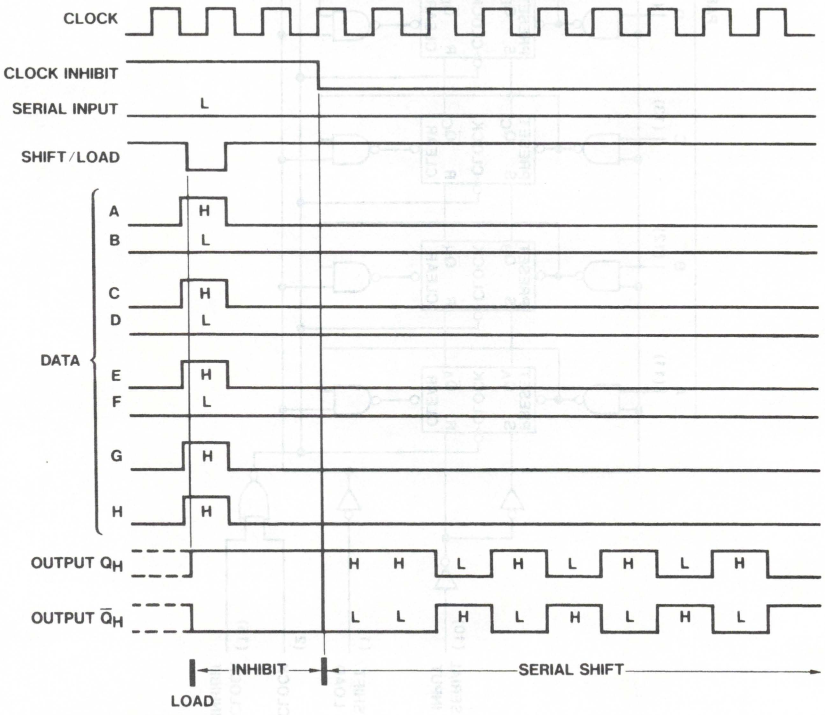
Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	54LS		DM74LS		Units
			C_L = 15 pF		R_L = 2 kΩ C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		30		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		30		42	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		30		42	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		30		47	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	H to Q_H		20		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	H to Q_H		30		37	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	H to $\overline{Q}_H$		30		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	H to $\overline{Q}_H$		25		32	ns

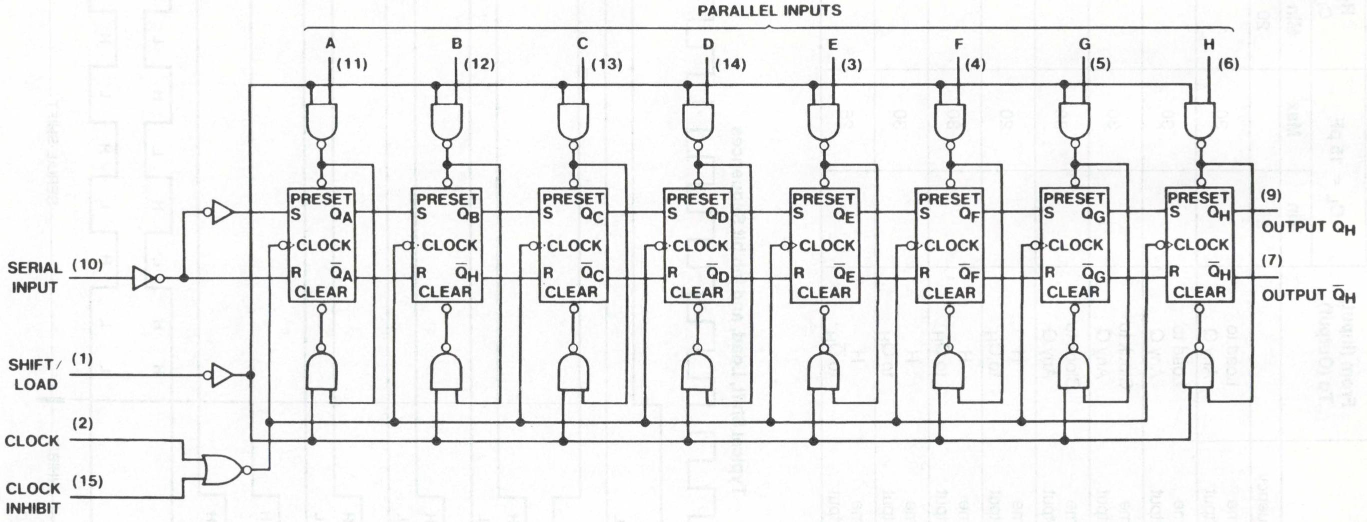
Timing Diagram

Typical Shift, Load, and Inhibit Sequences


CLOCK
CLOCK INHIBIT
SERIAL INPUT
L
SHIFT/LOAD
DATA
A
H
B
L
C
H
D
L
E
H
F
L
G
H
H
H
OUTPUT Q_H
H H L H L H L H
OUTPUT $\overline{Q}_H$
L L H L H L H L
INHIBIT
SERIAL SHIFT
LOAD

TL/F/6399-3

Logic Diagram


PARALLEL INPUTS
A (11)
B (12)
C (13)
D (14)
E (3)
F (4)
G (5)
H (6)
PRESET
S
CLOCK
R
CLEAR
Q_A
$\overline{Q}_A$
Q_B
$\overline{Q}_H$
Q_C
$\overline{Q}_C$
Q_D
$\overline{Q}_D$
Q_E
$\overline{Q}_E$
Q_F
$\overline{Q}_F$
Q_G
$\overline{Q}_G$
Q_H
$\overline{Q}_H$
(9) OUTPUT Q_H
(7) OUTPUT $\overline{Q}_H$
SERIAL INPUT (10)
SHIFT/LOAD (1)
CLOCK (2)
CLOCK INHIBIT (15)

TL/F/6399-2

National Semiconductor

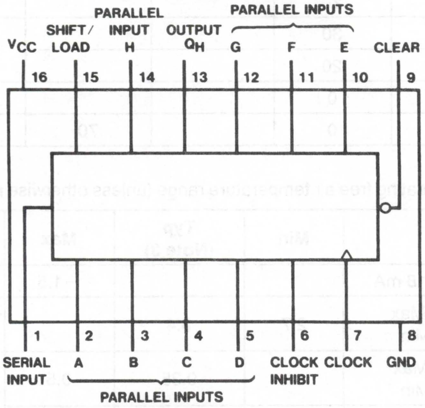
DM74LS166
8-Bit Parallel-In/Serial-Out Shift Registers

General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

Connection Diagram

Dual-In-Line Package



TL/F/6400–1

Order Number DM74LS166WM or DM74LS166N
See NS Package Number M16B or N16A

Function Table

Inputs						Internal Outputs		Output
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

a . . . h = The level of steady-state input at inputs A through H, respectively

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, Q_H, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Gn}, = The level of Q_A, Q_G, respectively, before the most recent ↑ transition of the clock

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74LS166 Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	MHz
	Clock Frequency (Note 2)		0		20	MHz
t_W	Pulse Width (Note 6)	Clock	20			ns
		Clear	20			
t_{SU}	Setup Time (Note 6)	Mode	30			ns
		Data	20			
t_H	Hold Time (Note 6)		0			ns
T_A	Free Air Operating Temperature		0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 5)		22	38	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: With all outputs open, 4.5V applied to the serial input, all other inputs except the CLOCK grounded, I_{CC} is measured after a momentary ground, then 4.5V is applied to the CLOCK.

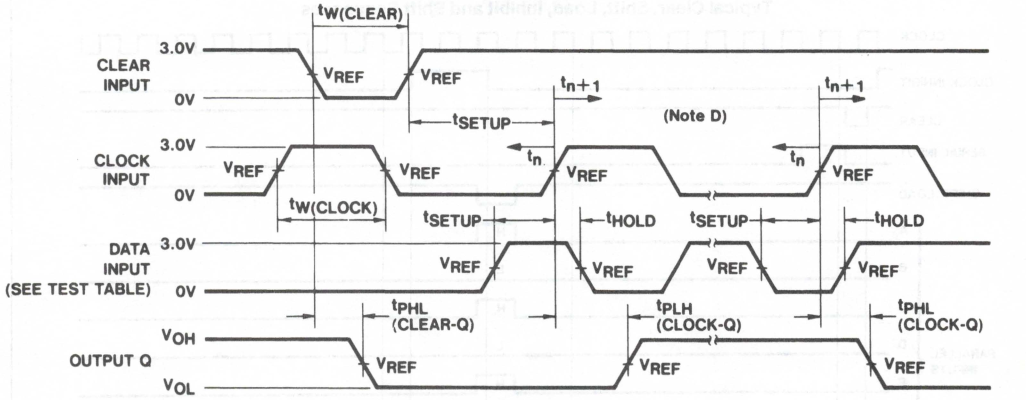
Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\,k\Omega$				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output	8	35		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output	8	35		41	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output	6	30		36	ns

Parameter Measurement Information

Voltage Waveforms



$t_{W(CLEAR)}$
CLEAR INPUT
3.0V
0V
V_{REF}
V_{REF}
t_{n+1}
t_{n+1}
t_{SETUP}
(Note D)
CLOCK INPUT
3.0V
0V
V_{REF}
V_{REF}
t_n
V_{REF}
t_n
V_{REF}
$t_{W(CLOCK)}$
t_{SETUP}
t_{HOLD}
t_{SETUP}
t_{HOLD}
DATA INPUT (SEE TEST TABLE)
3.0V
0V
V_{REF}
V_{REF}
V_{REF}
V_{REF}
t_{PHL} (CLEAR-Q)
t_{PLH} (CLOCK-Q)
t_{PHL} (CLOCK-Q)
OUTPUT Q
V_{OH}
V_{OL}
V_{REF}
V_{REF}
V_{REF}

TL/F/6400–2

Test Table for Synchronous Inputs

Data Input for Test	Shift/Load	Output Tested (See Note C)
H	0V	Q_H at T_{N+1}
Serial Input	4.5V	Q_H at T_{N+8}

Note A: The clock pulse has the following characteristics: $t_{W(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{W(clear)} \geq 20$ ns and t_{HOLD} = 0 ns. When testing f_{MAX}, vary the clock PRR.

Note B: A clear pulse is applied prior to each test.

Note C: Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

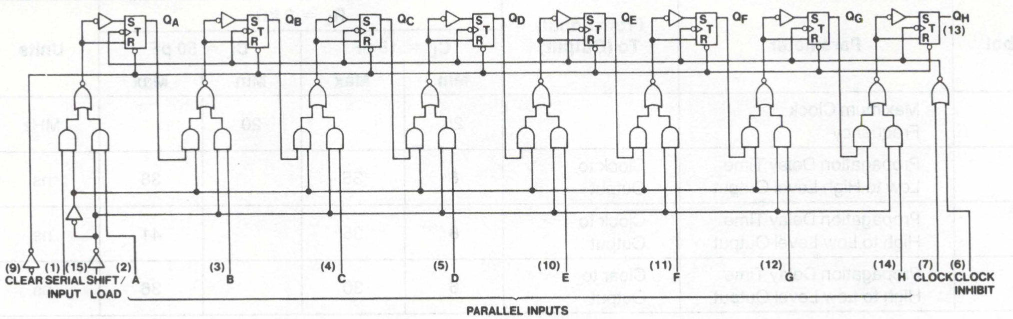
Note D: t_n = bit time before clocking transition

t_{n+1} = bit time after one clocking transition

t_{n+8} = bit time after eight clocking transitions

Note E: V_{REF} = 1.3V.

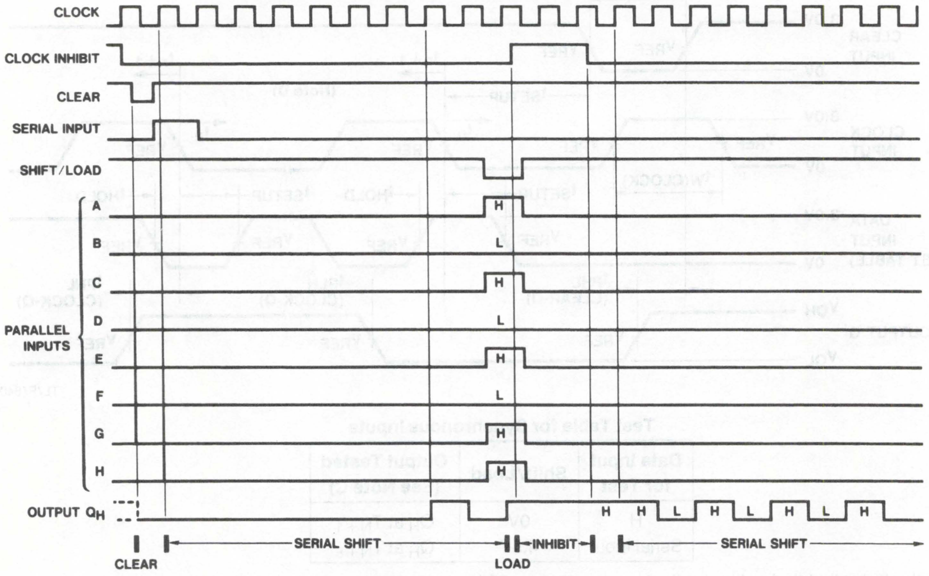
Logic Diagram


S
T
R
QA
QB
QC
QD
QE
QF
QG
QH
(13)
(9)
CLEAR
(1)
SERIAL
INPUT
(15)
SHIFT/
LOAD
(2)
A
(3)
B
(4)
C
(5)
D
(10)
E
(11)
F
(12)
G
(14)
H
(7)
CLOCK
(6)
CLOCK
INHIBIT
PARALLEL INPUTS

TL/F/6400–3

Timing Diagram

Typical Clear, Shift, Load, Inhibit and Shift Sequences


CLOCK
CLOCK INHIBIT
CLEAR
SERIAL INPUT
SHIFT/LOAD
PARALLEL INPUTS
A
B
C
D
E
F
G
H
H
L
H
L
H
L
H
H
OUTPUT QH
H
H
L
H
L
H
L
H
CLEAR
SERIAL SHIFT
LOAD
INHIBIT
SERIAL SHIFT

TL/F/6400–4

National Semiconductor

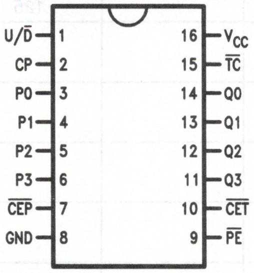
54LS168 Synchronous Bi-Directional BCD Decade Counter

General Description

The 54LS168 is a fully synchronous 4-state up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. It counts in the BCD (8421) sequence and all state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

Connection Diagram

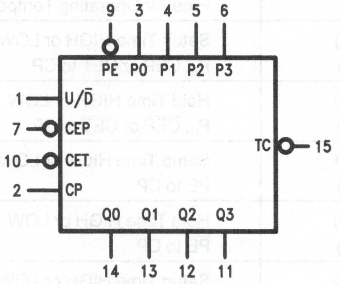
Dual-In-Line Package


U/D̄ 1
CP 2
P0 3
P1 4
P2 5
P3 6
CEP 7
GND 8
16 VCC
15 TC
14 Q0
13 Q1
12 Q2
11 Q3
10 CET
9 PE

TL/F/10207-1

Order Number 54LS168DMQB, 54LS168FMQB or 54LS168LMQB
See NS Package Number E20A, J16A or W16A

Logic Symbol


9
3
4
5
6
PE
P0
P1
P2
P3
1
U/D̄
7
CEP
10
CET
2
CP
TC
15
Q0
Q1
Q2
Q3
14
13
12
11

TL/F/10207-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$\overline{CET}$	Count Enable Trickle Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
P0–P3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
U/$\overline{D}$	Up-Down Count Control Input
Q0–Q3	Flip-Flop Outputs
$\overline{TC}$	Terminal Count Output (Active LOW)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS168			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			4	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n, $\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to CP	15 15			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n, $\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to CP	5 5			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{\text{PE}}$ to CP	20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{\text{PE}}$ to CP	0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW U/$\overline{\text{D}}$ to CP	25 25			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW U/$\overline{\text{D}}$ to CP	0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10.0V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Inputs			20	μA
			$\overline{\text{CET}}$			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Data	−0.5		−400	μA
			CP, $\overline{\text{PE}}$, U/$\overline{\text{D}}$, $\overline{\text{CEP}}$	−30		−400	
			$\overline{\text{CET}}$	−60		−800	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				34	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for test waveforms and output load)

Symbol	Parameter	54LS168		Units
		C_L = 15 pF		
		Min	Max	
f_{Max}	Maximum Clock Frequency	25		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		20 20	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{\text{TC}}$		30 30	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{CET}}$ to $\overline{\text{TC}}$		15 20	ns
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{\text{D}}$ to $\overline{\text{TC}}$		25 25	ns

Functional Description

The 'LS168 uses edge-triggered D-type flip-flops and has no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{\text{PE}}$ is LOW, the data on the P0–P3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{\text{CEP}}$ and $\overline{\text{CET}}$ must be LOW and $\overline{\text{PE}}$ must be HIGH. The U/$\overline{\text{D}}$ input then determines the direction of counting. The Terminal Count ($\overline{\text{TC}}$) output is normally HIGH and goes LOW, provided that $\overline{\text{CET}}$ is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 9 in the COUNT UP mode. The $\overline{\text{TC}}$ output state is not a function of the Count Enable Parallel ($\overline{\text{CEP}}$) input level. The $\overline{\text{TC}}$ output of the 'LS168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'LS168 will return to the legitimate sequence within two counts. Since the $\overline{\text{TC}}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{\text{TC}}$. For this reason the use of $\overline{\text{TC}}$ as a clock signal is not recommended (see logic equation below).

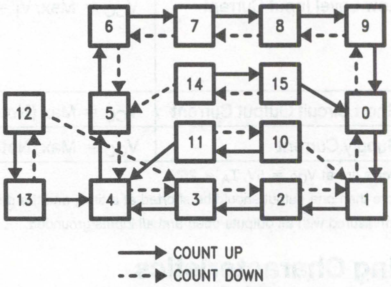
1. Count Enable = $\overline{\text{CEP}} \bullet \overline{\text{CET}} \bullet \overline{\text{PE}}$
2. Up: $\overline{\text{TC}}$ = $\text{Q0} \bullet \text{Q3} \bullet (\text{U}/\overline{\text{D}}) \bullet \overline{\text{CET}}$
3. Down: $\overline{\text{TC}}$ = $\overline{\text{Q0}} \bullet \overline{\text{Q1}} \bullet \overline{\text{Q2}} \bullet \overline{\text{Q3}} \bullet \overline{(\text{U}/\overline{\text{D}})} \bullet \overline{\text{CET}}$

'LS168 Mode Select Table

$\overline{\text{PE}}$	$\overline{\text{CEP}}$	$\overline{\text{CET}}$	U/$\overline{\text{D}}$	Action on Rising Clock Edge
L	X	X	X	Load ($P_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

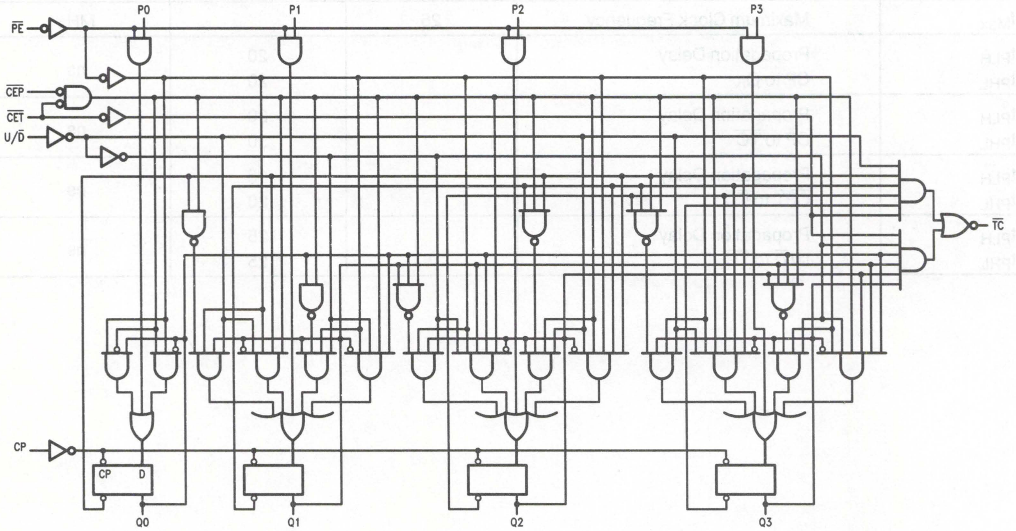
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



TL/F/10207-3

Logic Diagram



TL/F/10207-4

National Semiconductor

54LS169/DM54LS169A/DM74LS169A Synchronous 4-Bit Up/Down Binary Counter

General Description

This synchronous presettable counter features an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs all change at the same time when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising edge of the clock waveform.

This counter is fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count-enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry outputs. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up, and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

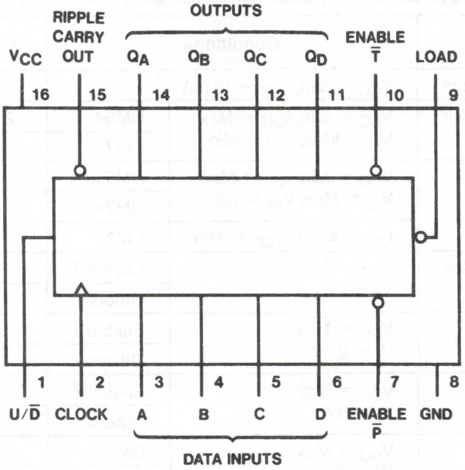
This counter features a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down), which modify the operating mode, have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

- Fully synchronous operation for counting and programming.
- Internal look-ahead for fast counting.
- Carry output for n-bit cascading.
- Fully independent clock circuit
- Alternate Military/Aerospace device (54LS169) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6401–1

Order Number 54LS169DMQB, 54LS169FMQB, 54LS169LMQB, DM54LS169AJ, DM54LS169AW, DM74LS169AM or DM74LS169AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS169A			DM74LS169A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Clock Pulse Width (Note 3)		25			25			ns
t_{SU}	Setup Time (Note 3)	Data	20			20			ns
		Enable $\overline{T}$ or $\overline{P}$	20			20			
		Load	25			25			
		U/D	30			30			
t_H	Hold Time (Note 3)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 2: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		$I_{OL} = 4$ mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max $V_I = 7V$	Enable $\overline{T}$			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max $V_I = 2.7V$	Enable $\overline{T}$			40	µA
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max $V_I = 0.4V$	Enable $\overline{T}$			−0.8	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			20	34	mA

Note 4: All typicals are at $V_{CC} = 5V$ and $T_A = 25°C$.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured after a momentary 4.5V, then ground, is applied to the CLOCK with all other inputs grounded and all the outputs open.

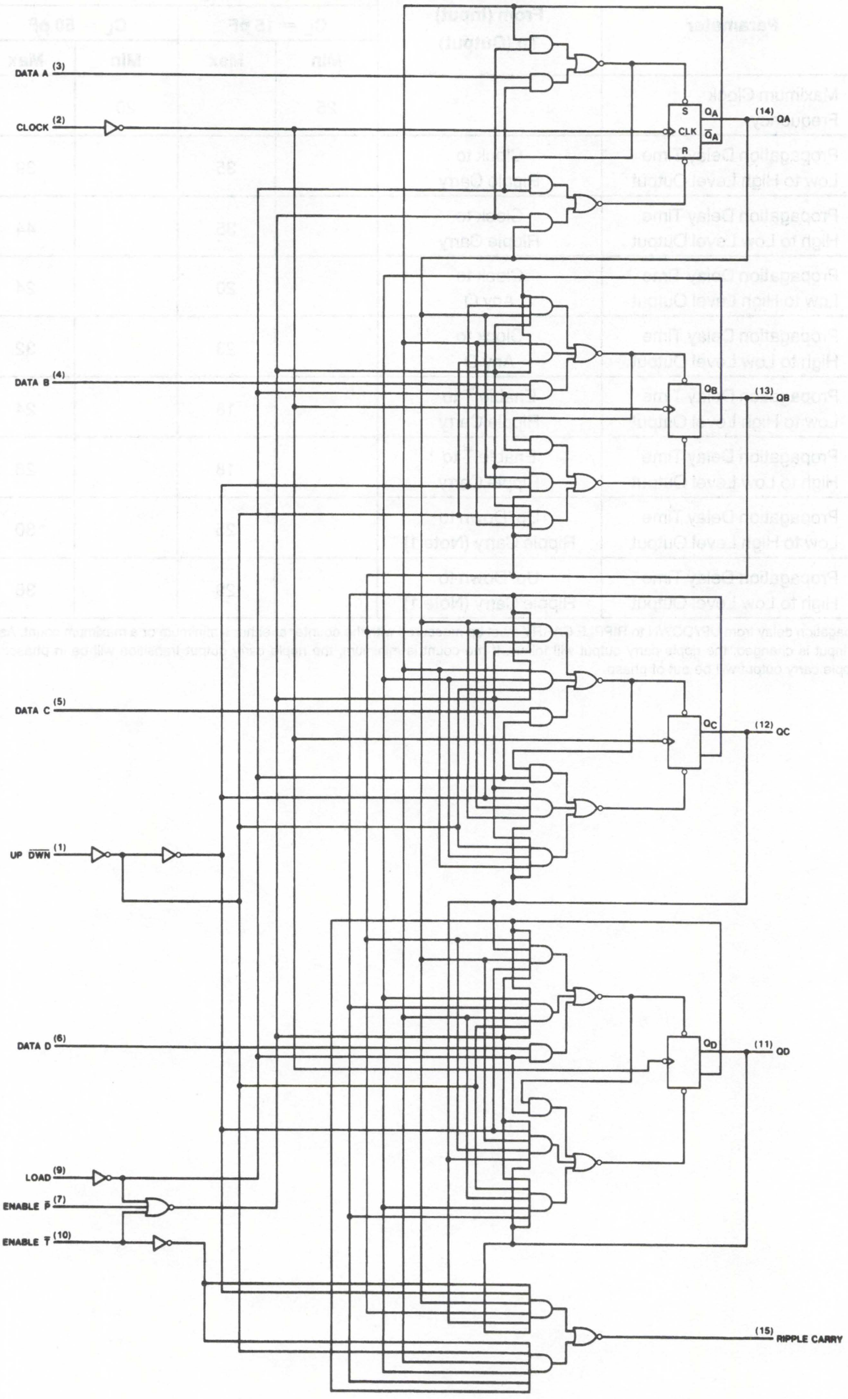
Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		35		39	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		23		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable $\overline{T}$ to Ripple Carry		18		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable $\overline{T}$ to Ripple Carry		18		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Up/Down to Ripple Carry (Note 1)		25		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Up/Down to Ripple Carry (Note 1)		29		38	ns

Note 1: The propagation delay from UP/DOWN to RIPPLE CARRY must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum, the ripple carry output transition will be in phase. If the count is maximum, the ripple carry output will be out of phase.

Logic Diagram

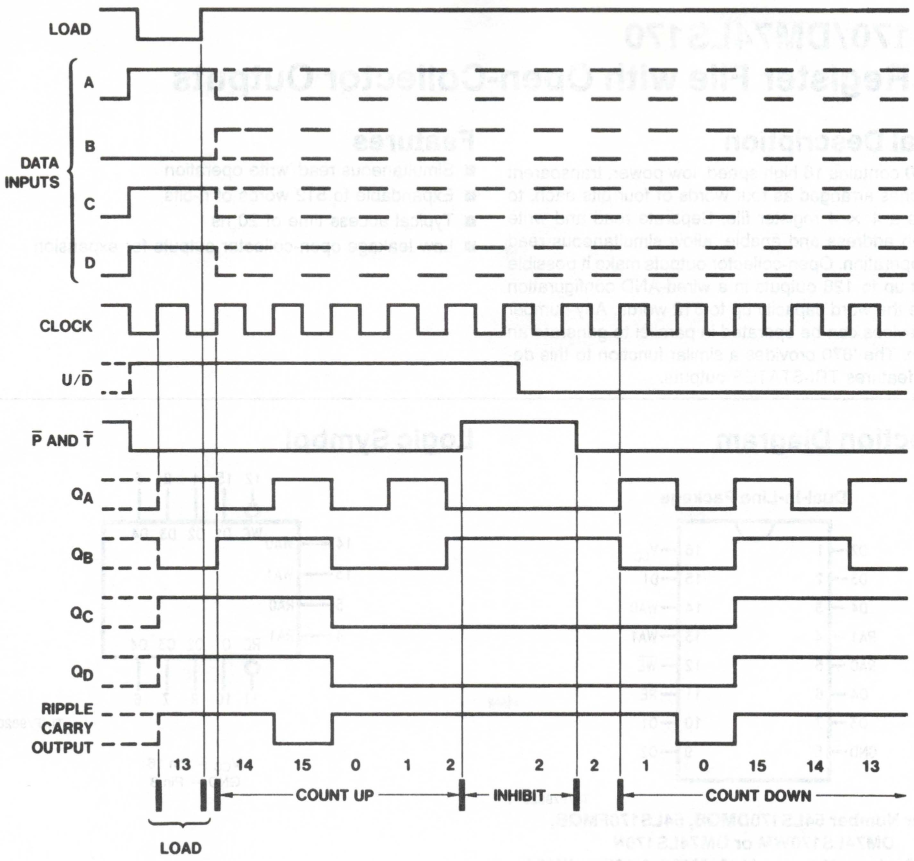
LS169A Binary Counter


DATA A (3)
CLOCK (2)
DATA B (4)
DATA C (5)
UP $\overline{\text{DWN}}$ (1)
DATA D (6)
LOAD (9)
ENABLE $\overline{\text{P}}$ (7)
ENABLE $\overline{\text{T}}$ (10)
S
CLK
R
Q_A
$\overline{Q}_A$
(14) QA
Q_B
(13) QB
Q_C
(12) QC
Q_D
(11) QD
(15) RIPPLE CARRY

TL/F/6401-2

Timing Diagram

LS169A Binary Counters
Typical Load, Count, and Inhibit Sequences


LOAD
DATA INPUTS
A
B
C
D
CLOCK
U/$\overline{D}$
$\overline{P}$ AND $\overline{T}$
Q_A
Q_B
Q_C
Q_D
RIPPLE CARRY OUTPUT
13
14
15
0
1
2
2
2
1
0
15
14
13
COUNT UP
INHIBIT
COUNT DOWN
LOAD

TL/F/6401-3

National Semiconductor

54LS170/DM74LS170
4 x 4 Register File with Open-Collector Outputs

General Description

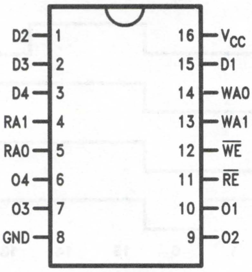
The 'LS170 contains 16 high speed, low power, transparent D-type latches arranged as four words of four bits each, to function as a 4 × 4 register file. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. Open-collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length. The '670 provides a similar function to this device but it features TRI-STATE® outputs.

Features

- Simultaneous read/write operation
- Expandable to 512 words of n-bits
- Typical access time of 20 ns
- Low leakage open-collector outputs for expansion

Connection Diagram

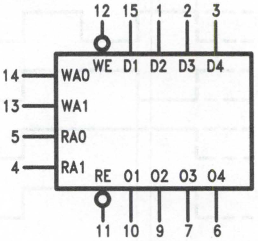
Dual-In-Line Package


D2 1
D3 2
D4 3
RA1 4
RA0 5
O4 6
O3 7
GND 8
16 V$_{CC}$
15 D1
14 WA0
13 WA1
12 $\overline{\text{WE}}$
11 $\overline{\text{RE}}$
10 O1
9 O2

TL/F/9820-1

Order Number 54LS170DMQB, 54LS170FMQB, DM74LS170WM or DM74LS170N
See NS Package Number J16A, M16B, N16E or W16A

Logic Symbol


12
15
1
2
3
WE
D1
D2
D3
D4
14
WA0
13
WA1
5
RA0
4
RA1
RE
O1
O2
O3
O4
11
10
9
7
6

TL/F/9820-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
D1–D4	Data Inputs
WA0–WA1	Write Address Inputs
$\overline{\text{WE}}$	Write Enable Input (Active LOW)
RA0, RA1	Read Address Inputs
$\overline{\text{RE}}$	Read Enable Input (Active LOW)
O1–O4	Data Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS170			DM74LS170			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			20			20	µA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s	Setup Time HIGH or LOW Dn to Rising $\overline{\text{WE}}$	10			10			ns
t_h	Hold Time HIGH or LOW Dn to Rising $\overline{\text{WE}}$	5.0			5.0			ns
t_s	Setup Time HIGH or LOW WAn to Falling $\overline{\text{WE}}$	10			10			ns
t_h	Hold Time HIGH or LOW WAn to Rising $\overline{\text{WE}}$	5.0			5.0			ns
$t_w(L)$	$\overline{\text{WE}}$ or $\overline{\text{RE}}$ Pulse Width LOW	25			25			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Uints
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.0			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V	Dns, RAO, WA0			0.1	mA
			$\overline{\text{WE}}$, $\overline{\text{RE}}$			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Inputs			20	µA
			$\overline{\text{RE}}$, $\overline{\text{WE}}$			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	$\overline{\text{RE}}$, $\overline{\text{WE}}$	−0.06		−0.8	mA
			RA1, WA1	−0.05		−0.4	
			DATA, RA0, WA0	−0.03		−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max, Dn, $\overline{\text{WE}}$, $\overline{\text{RE}}$ = 4.5V, WAn, RAn = GND				40	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

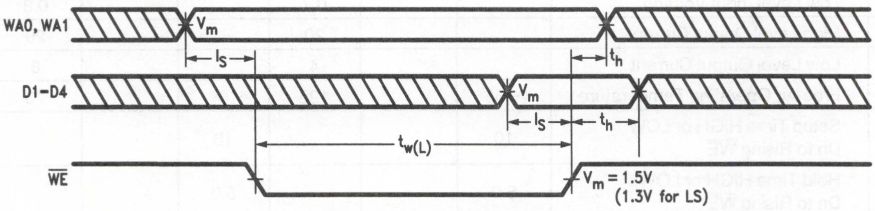
Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C, (See Section 1 for waveforms and load configurations)

Symbol	Parameter	Conditions	R_L = 2k, C_L = 15 pF Min	Max	Units
t_{PLH} t_{PHL}	Propagation Delay* RA0 or RA1 to On			35 35	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{RE}$ to On			30 30	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{WE}$ to On			35 35	ns
t_{PLH} t_{PHL}	Propagation Delay Dn to On			35 35	ns

*Measured at least 25 ns after entry of new data at selected location.

Switching Waveforms



TL/F/9820-4

FIGURE a

Write Function Table

Write Inputs			D Inputs to
$\overline{WE}$	WA1	WA0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (Hold)

Read Function Table

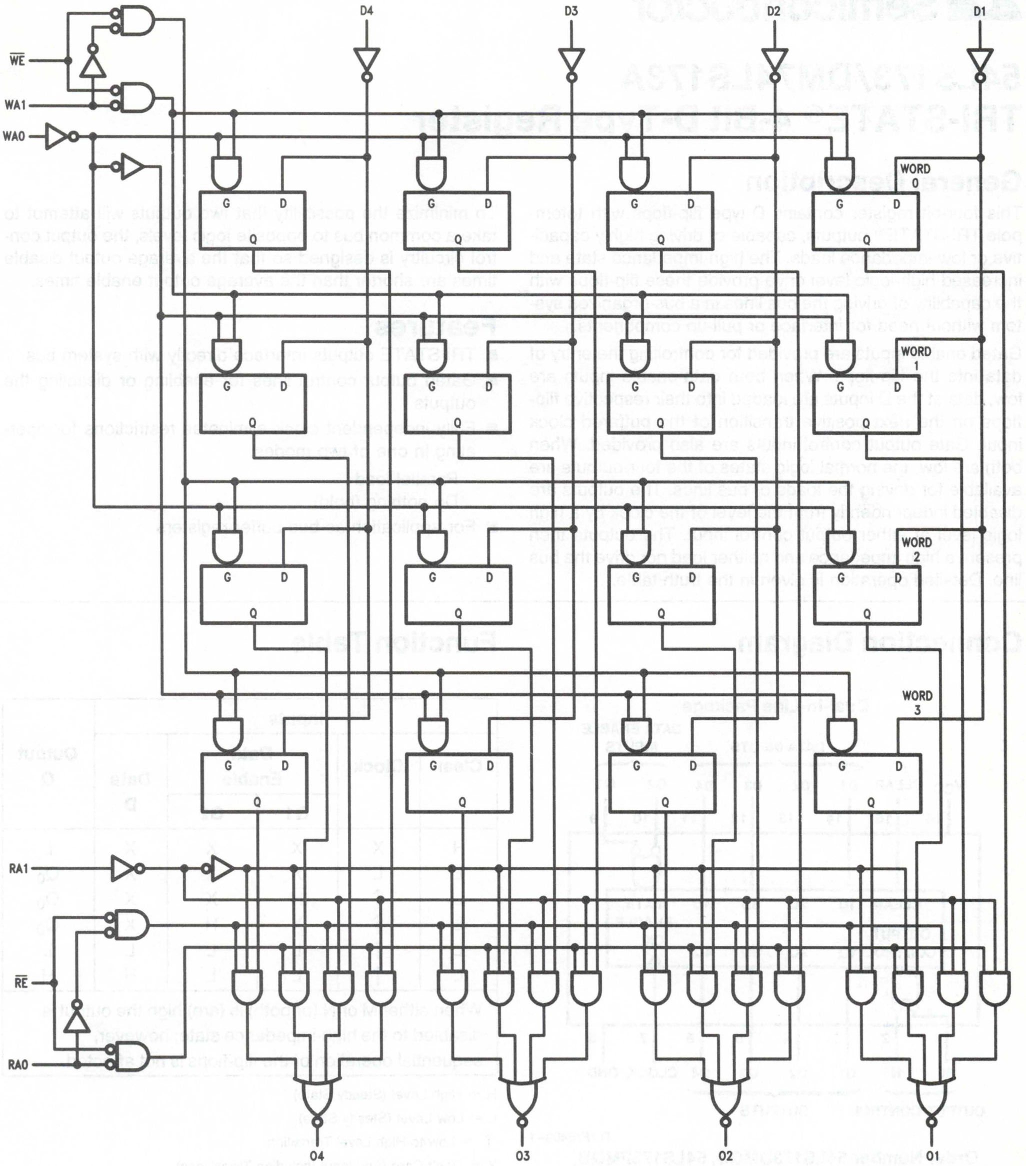
Read Inputs			Outputs from
$\overline{RE}$	RA1	RA0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (High Z)

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



WE
WA1
WA0
D4
D3
D2
D1
WORD 0
WORD 1
WORD 2
WORD 3
G
D
Q
RA1
RE
RA0
O4
O3
O2
O1

TL/F/9820-3

National Semiconductor

54LS173/DM74LS173A TRI-STATE® 4-Bit D-Type Register

General Description

This four-bit register contains D-type flip-flops with totem-pole TRI-STATE® outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the truth table.

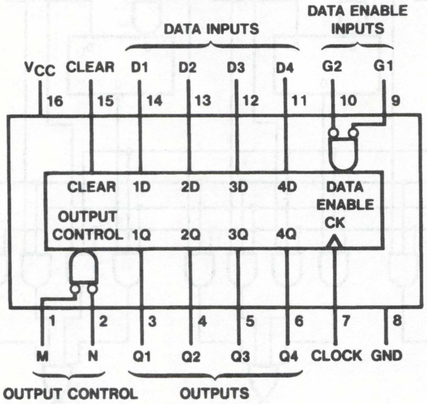
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock eliminates restrictions for operating in one of two modes:
  - Parallel load
  - Do nothing (hold)
- For application as bus buffer registers

Connection Diagram

Dual-In-Line Package



TL/F/6403–1

Order Number 54LS173DMQB, 54LS173FMQB, 54LS173LMQB, DM74LS173AM or DM74LS173AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Inputs					Output Q
Clear	Clock	Data Enable		Data D	
		G1	G2		
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = High Level (Steady State)

L = Low Level (Steady State)

↑ = Low-to-High Level Transition

X = Don't Care (Any Input Including Transitions)

Q_0 = The Level of Q Before the Indicated Steady State Input Conditions Were Established.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		54LS173			DM74LS173A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLK}	Clock Frequency (Note 1)		30			0		30	MHz
	Clock Frequency (Note 2)					0		20	MHz
t_W	Pulse Width (Note 3)	Clock	20			17			ns
		Clear	17			17			
t_{SU}	Setup Time (Note 3)	Enable	17			23			ns
		Data	15			15			
t_H	Hold Time (Note 3)	Enable	0			0			ns
		Data	5			0			
t_{REL}	Clear Release Time		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 45 pF, R_L = 667Ω, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 150 pF, R_L = 667Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 6)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 7)			17	30	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	54LS C_L = 50 pF		DM74LS C_L = 150 pF R_L = 667Ω		Units
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		20		ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		28		34	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		28		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		30		40	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control (M or N) to Any Q		23		34	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control (M or N) to Any Q		28		45	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 8)	Output Control (M or N) to Any Q		17		25	ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 8)	Output Control (M or N) to Any Q		23		25	ns

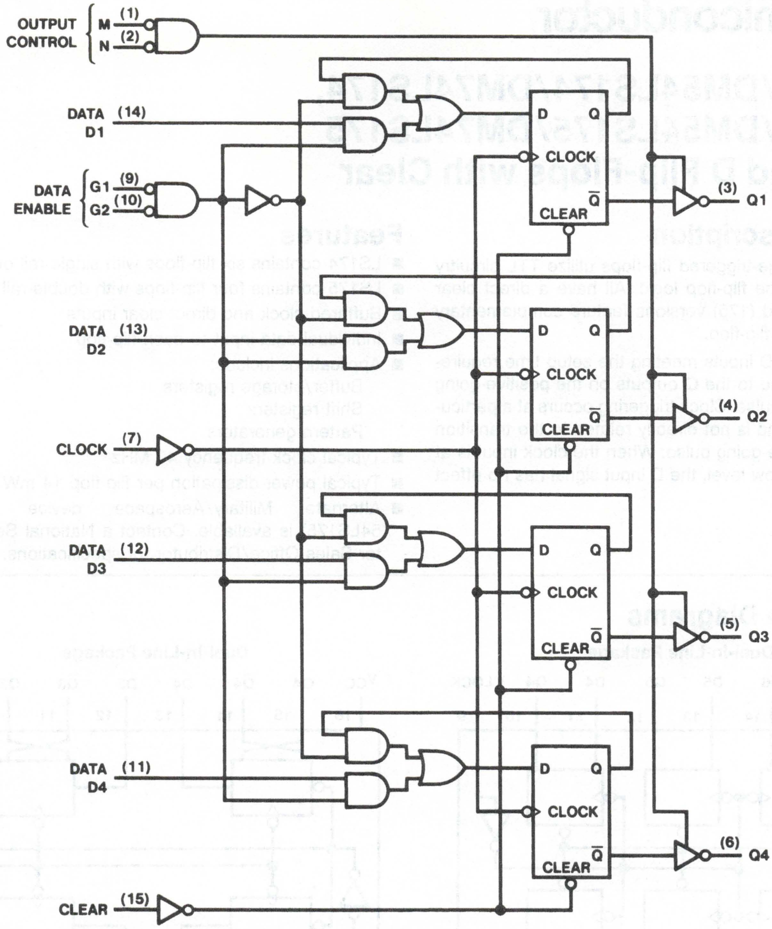
Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all outputs open: Clear grounded after a momentary 4.5V; N, G1, G2 and all data inputs grounded: and the CLOCK and M input at 4.5V.

Note 7: C_L = 5 pF.

Logic Diagram


OUTPUT CONTROL
M (1)
N (2)
DATA D1 (14)
DATA ENABLE
G1 (9)
G2 (10)
DATA D2 (13)
CLOCK (7)
DATA D3 (12)
DATA D4 (11)
CLEAR (15)
D
Q
CLOCK
$\overline{Q}$
CLEAR
(3) Q1
(4) Q2
(5) Q3
(6) Q4

TL/F/6403-2

National Semiconductor

54LS174/DM54LS174/DM74LS174, 54LS175/DM54LS175/DM74LS175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

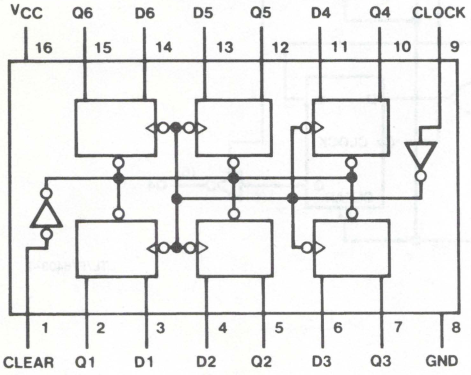
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- LS174 contains six flip-flops with single-rail outputs
- LS175 contains four flip-flops with double-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 40 MHz
- Typical power dissipation per flip-flop 14 mW
- Alternate Military/Aerospace device (54LS174, 54LS175) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

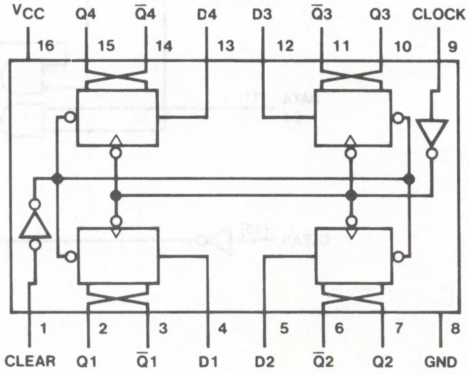
Dual-In-Line Package



TL/F/6404-1

Order Number 54LS174DMQB, 54LS174FMQB, 54LS174LMQB, DM54LS174J, DM54LS174W, DM74LS174M or DM74LS174N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Dual-In-Line Package



TL/F/6404-2

Order Number 54LS175DMQB, 54LS175FMQB, 54LS175LMQB, DM54LS175J DM54LS175W, DM74LS175M or DM74LS175N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = LS175 only

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS174			DM74LS174			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
t_W	Pulse Width (Note 6)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time (Note 6)		20			20			ns
t_H	Data Hold Time (Note 6)		0			0			ns
t_{REL}	Clear Release Time (Note 6)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'LS174 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Clock			−0.4	mA
			Clear			−0.4	
			Data			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			16	26	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the clock.

Note 6: T_A = 25°C and V_{CC} = 5V.

’LS174 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ, C_L = 15 pF Min	R_L = 2 kΩ, C_L = 15 pF Max	R_L = 2 kΩ, C_L = 50 pF Min	R_L = 2 kΩ, C_L = 50 pF Max	Units
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		30		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		30		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		35		42	ns

Recommended Operating Conditions

Symbol	Parameter		DM54LS175 Min	DM54LS175 Nom	DM54LS175 Max	DM74LS175 Min	DM74LS175 Nom	DM74LS175 Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
t_W	Pulse Width (Note 3)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time (Note 3)		20			20			ns
t_H	Data Hold Time (Note 3)		0			0			ns
t_{REL}	Clear Release Time (Note 3)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

'LS175 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Clock			−0.4	mA
			Clear			−0.4	
			Data			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			11	18	mA

'LS175 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

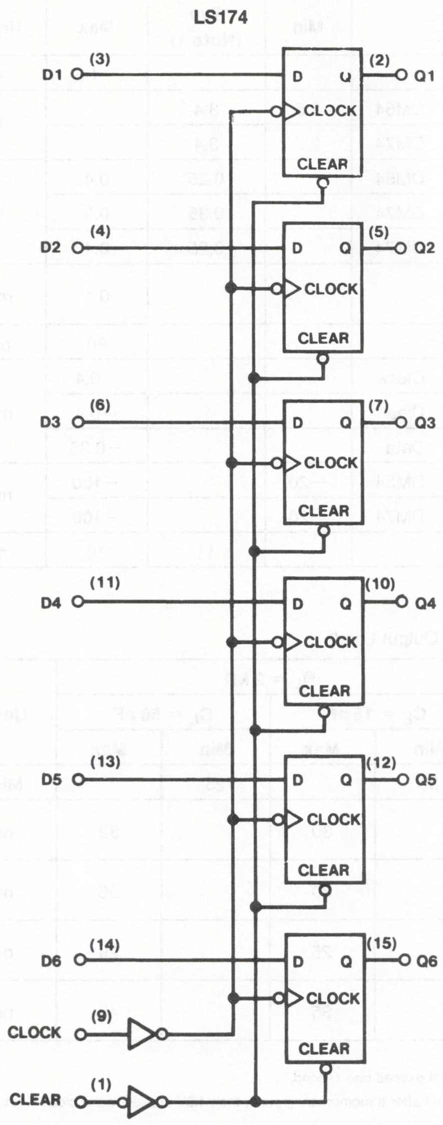
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		30		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		30		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25		29	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		35		42	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

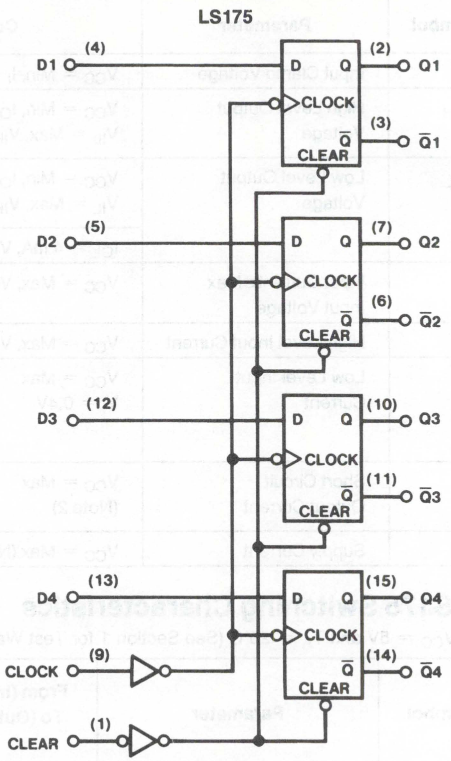
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the clock input.

Logic Diagrams


LS174
D1
(3)
D
Q
(2)
Q1
CLOCK
CLEAR
D2
(4)
(5)
Q2
D3
(6)
(7)
Q3
D4
(11)
(10)
Q4
D5
(13)
(12)
Q5
D6
(14)
(15)
Q6
CLOCK
(9)
CLEAR
(1)

TL/F/6404-3


LS175
D1
(4)
D
Q
(2)
Q1
CLOCK
Q̄
(3)
Q̄1
CLEAR
D2
(5)
(7)
Q2
(6)
Q̄2
D3
(12)
(10)
Q3
(11)
Q̄3
D4
(13)
(15)
Q4
(14)
Q̄4
CLOCK
(9)
CLEAR
(1)

TL/F/6404-4

National Semiconductor

54LS181/DM74LS181
4-Bit Arithmetic Logic Unit

General Description

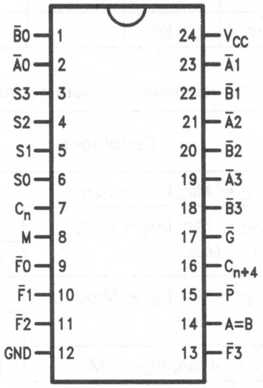
The 'LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations.

Features

- Provides 16 arithmetic operations: add, subtract, compare, double, plus twelve other arithmetic operations
- Provides all 16 logic operations of two variables: exclusive-OR, compare, AND, NAND, OR, NOR, plus ten other logic operations
- Full lookahead for high speed arithmetic operation on long words

Connection Diagram

Dual-In-Line Package


$\overline{B0}$ 1
$\overline{A0}$ 2
S3 3
S2 4
S1 5
S0 6
C_n 7
M 8
$\overline{F0}$ 9
$\overline{F1}$ 10
$\overline{F2}$ 11
GND 12
24 V_{CC}
23 $\overline{A1}$
22 $\overline{B1}$
21 $\overline{A2}$
20 $\overline{B2}$
19 $\overline{A3}$
18 $\overline{B3}$
17 $\overline{G}$
16 C_{n+4}
15 $\overline{P}$
14 A=B
13 $\overline{F3}$

TL/F/9821-1

Order Number 54LS181DMQB, 54LS181FMQB or DM74LS181N
See NS Package Number J24A, N24A or W24C

Pin Names	Description
$\overline{A0}$–$\overline{A3}$	Operand Inputs (Active LOW)
$\overline{B0}$–$\overline{B3}$	Operand Inputs (Active LOW)
S0–S3	Function Select Inputs
M	Mode Control Input
C_n	Carry Input
$\overline{F0}$–$\overline{F3}$	Function Outputs (Active LOW)
A = B	Comparator Output
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)
C_{n+4}	Carry Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS181			DM74LS181			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V	M input $\overline{A}_n$, $\overline{B}_n$ S_n C_n			0.1 0.3 0.4 0.5	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	 $\overline{A}_n$, $\overline{B}_n$ S_n C_n			20 60 80 100	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	 $\overline{A}_n$, $\overline{B}_n$ S_n C_n			−0.4 −1.2 −1.6 −2.0	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max, $\overline{B}_n$, C_n = GND S_n, M, $\overline{A}_n$ = 4.5V	54LS			35	mA
			DM74			37	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	Conditions	54LS/DM74LS		Units
			$C_L = 15$ pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}	M = GND		27 20	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to $\overline{F}$	M = GND		26 20	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$ (Sum)	M, S_1, S_2 = GND; S_1, S_3 = 4.5V		29 23	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$ (Diff)	M, S_0, S_3 = GND; S_1, S_2 = 4.5V		32 26	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$ (Sum)	M, S_1, S_2 = GND; S_0, S_3 = 4.5V		30 30	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$ (Diff)	M, S_0, S_3 = GND; S_1, S_2 = 4.5V		30 33	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$ (Sum)	M, S_1, S_2 = GND; S_0, S_3 = 4.5V		32 25	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$ (Diff)	M, S_0, S_3 = GND; S_1, S_2 = 4.5V		32 33	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F}$ (Logic)	M = 4.5V		33 29	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4} (Sum)	M, S_1, S_2 = GND; S_0, S_3 = 4.5V		38 38	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4} (Diff)	M, S_0, S_3 = GND; S_1, S_2 = 4.5V		41 41	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to A = B	M, S_0, S_3 = GND; S_1, S_2 = 4.5V; R_L = 2 kΩ to 5.0V		50 62	ns

Sum Mode Test Table I

Function Inputs S0 = S3 = 4.5V, S1 = S2 = M = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

Diff Mode Test Table II

Function Inputs S1 = S2 = 4.5V, S0 = S3 = M = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

Logic Mode Test Table III Function Inputs S1 = S2 = M = 4.5V, S0 = S3 = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$

Functional Description

The 'LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S0–S3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the ADD mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the SUBTRACT mode, $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of four 'LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

Function Table

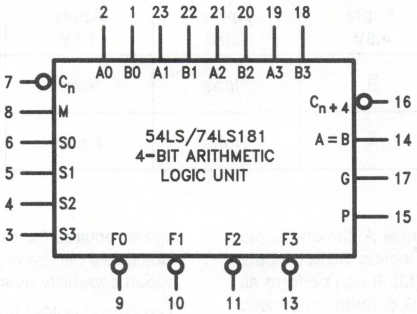
Mode Select Inputs				Active LOW Operands & F_n Outputs		Active HIGH Operands & F_n Outputs	
S3	S2	S1	S0	Logic (M = H)	Arithmetic** (M = L) (C_n = L)	Logic (M = H)	Arithmetic** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A + B}$	A + B
L	L	H	L	$\overline{A + B}$	A$\overline{B}$ minus 1	$\overline{A}$B	A + $\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A + B}$	A plus (A + $\overline{B}$)	$\overline{AB}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A ⊕ B	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$	A$\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}$B	A plus (A + B)	$\overline{A}$ + B	A plus AB
H	L	L	H	A ⊕ B	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H	H	H	L	AB	A$\overline{B}$ minus A	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A	A	A minus 1

*Each bit is shifted to the next move significant position.

**Arithmetic operations expressed in 2s complement notation.

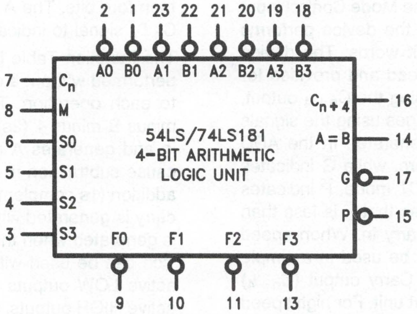
Logic Symbols

Active High Operands


2
1
23
22
21
20
19
18
A0
B0
A1
B1
A2
B2
A3
B3
7
C_n
8
M
6
S0
5
S1
4
S2
3
S3
54LS/74LS181
4-BIT ARITHMETIC
LOGIC UNIT
C_{n+4}
16
A = B
14
G
17
P
15
F0
F1
F2
F3
9
10
11
13

TL/F/9821-3

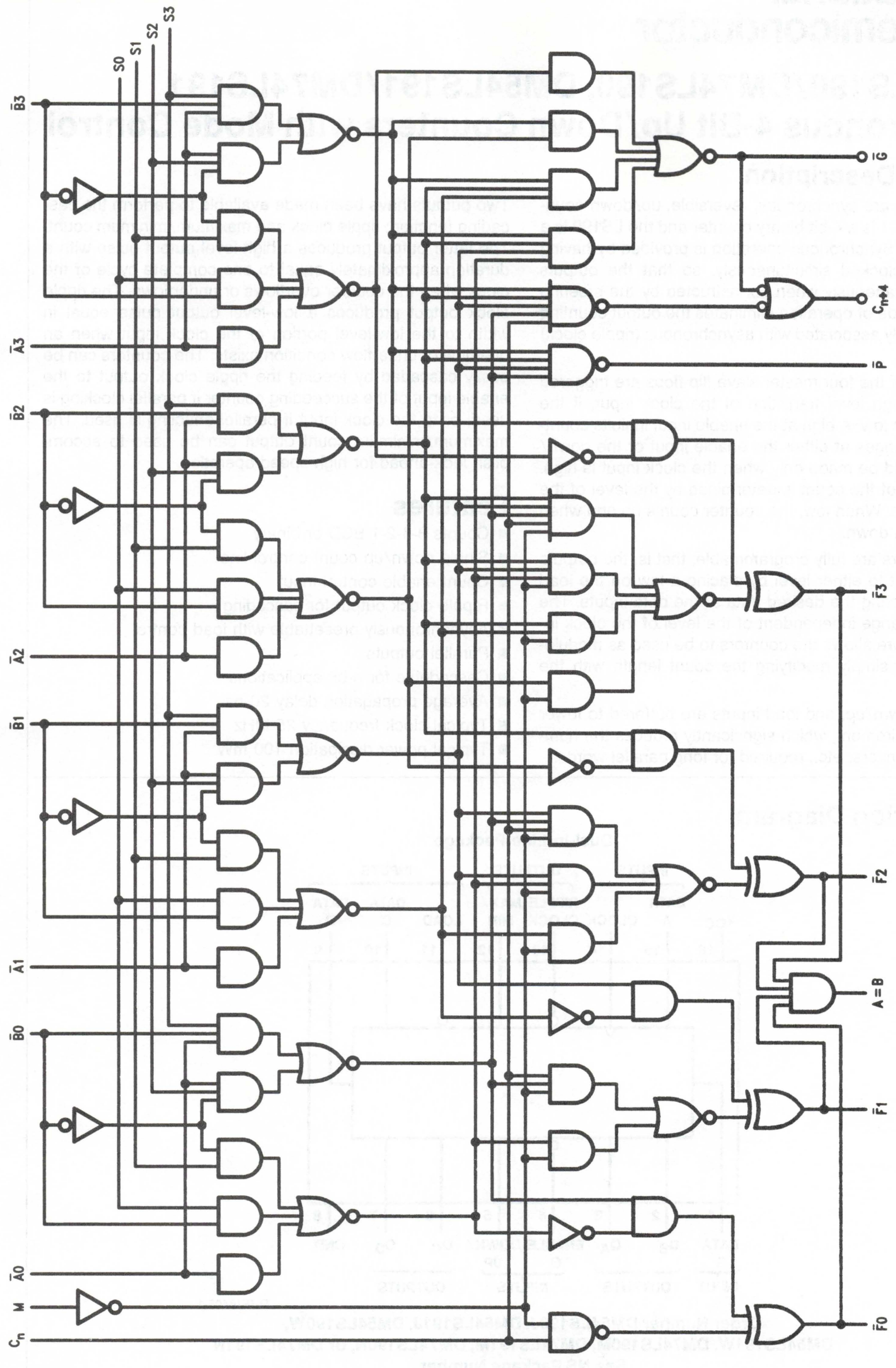
Active Low Operands


2
1
23
22
21
20
19
18
A0
B0
A1
B1
A2
B2
A3
B3
7
C_n
8
M
6
S0
5
S1
4
S2
3
S3
54LS/74LS181
4-BIT ARITHMETIC
LOGIC UNIT
C_{n+4}
16
A = B
14
G
17
P
15
F0
F1
F2
F3
9
10
11
13

TL/F/9821-4

V_{CC} = Pin 24
GND = Pin 12

Logic Diagram



B̄3
A̅3
B̄2
A̅2
B̄1
A̅1
B̄0
A̅0
M
Cn
S0
S1
S2
S3
G̅
Cn+4
P̅
F̅3
F̅2
A=B
F̅1
F̅0
TL/F/9821-5

National Semiconductor

DM54LS190/DM74LS190, DM54LS191/DM74LS191 Synchronous 4-Bit Up/Down Counters with Mode Control

General Description

These circuits are synchronous, reversible, up/down counters. The LS191 is a 4-bit binary counter and the LS190 is a BCD counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

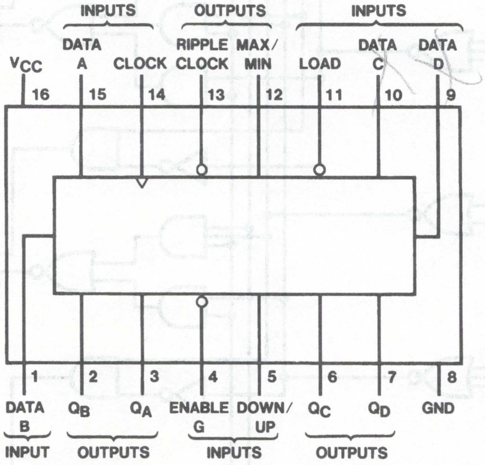
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Counts 8-4-2-1 BCD or binary
- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications
- Average propagation delay 20 ns
- Typical clock frequency 25 MHz
- Typical power dissipation 100 mW

Connection Diagram

Dual-In-Line-Package



TL/F/6405-1

Order Number DM54LS190J, DM54LS191J, DM54LS190W, DM54LS191W, DM74LS190M, DM74LS191M, DM74LS190N, or DM74LS191N
See NS Package Number
J16A, M16A, N16A or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 7V
Input Voltage 7V
Operating Free Air Temperature Range
DM54LS −55°C to +125°C
DM74LS 0°C to +70°C
Storage Temperature Range −65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS190, LS191			DM74LS190, LS191			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 4)		0		20	0		20	MHz
t_W	Pulse Width (Note 4)	Clock	25			25			ns
		Load	35			35			
t_{SU}	Data Setup Time (Note 4)		20			20			ns
t_H	Data Hold Time (Note 4)		0			0			ns
t_{EN}	Enable Time to Clock (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'LS190 and 'LS191 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	Enable			0.3	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Enable			60	μA
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Enable			−1.08	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			20	35	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: T_A = 25°C and V_{CC} = 5V.

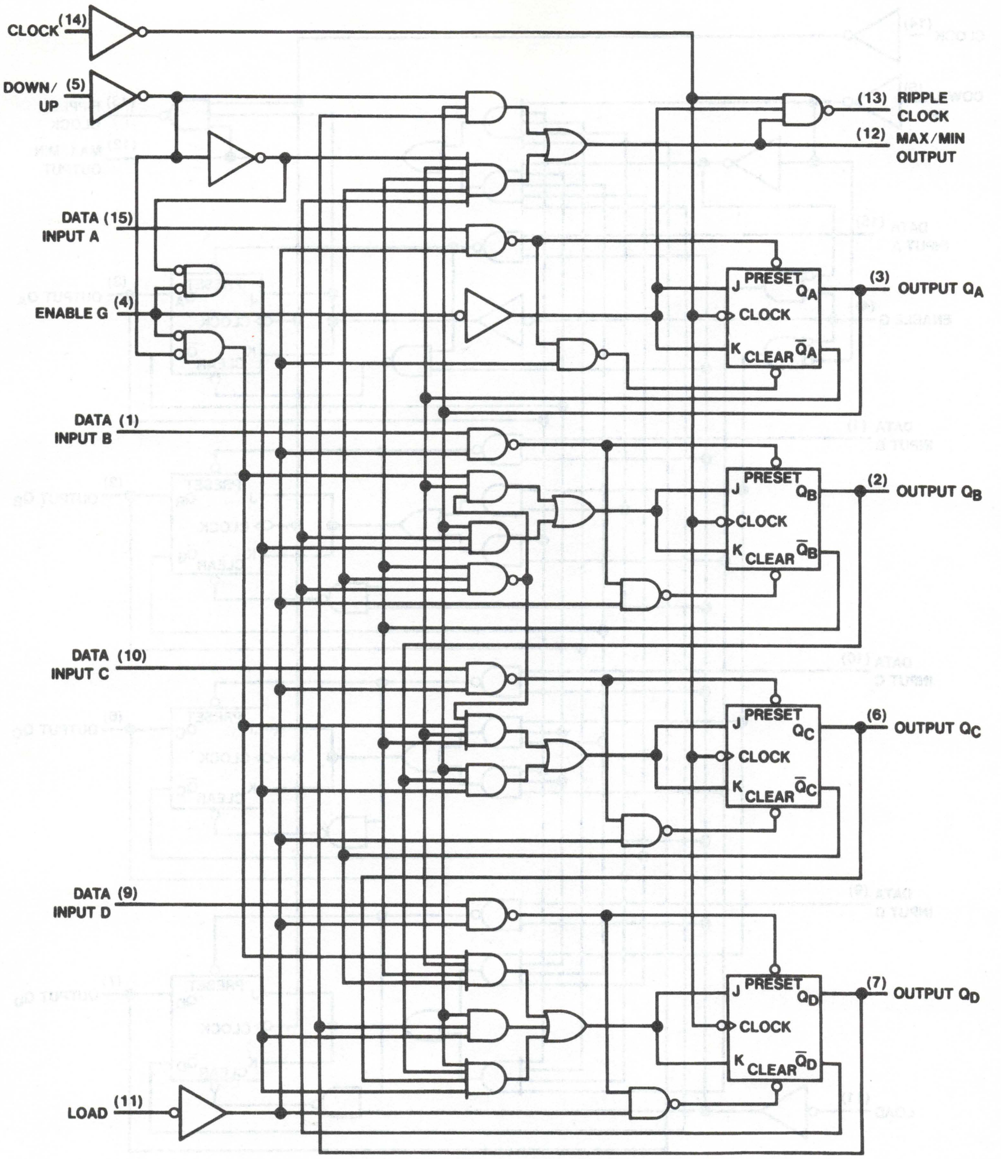
'LS190 and 'LS191 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		20		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		33		43	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		50		59	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Any Q		22		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Any Q		50		62	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Clock		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Clock		24		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		24		29	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		36		45	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Max/Min		42		47	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Max/Min		52		65	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Up/Down to Ripple Clock		45		50	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Up/Down to Ripple Clock		45		54	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Down/Up to Max/Min		33		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Down/Up to Max/Min		33		42	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Ripple Clock		33		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Ripple Clock		33		42	ns

Logic Diagrams

LS190 Decade Counters

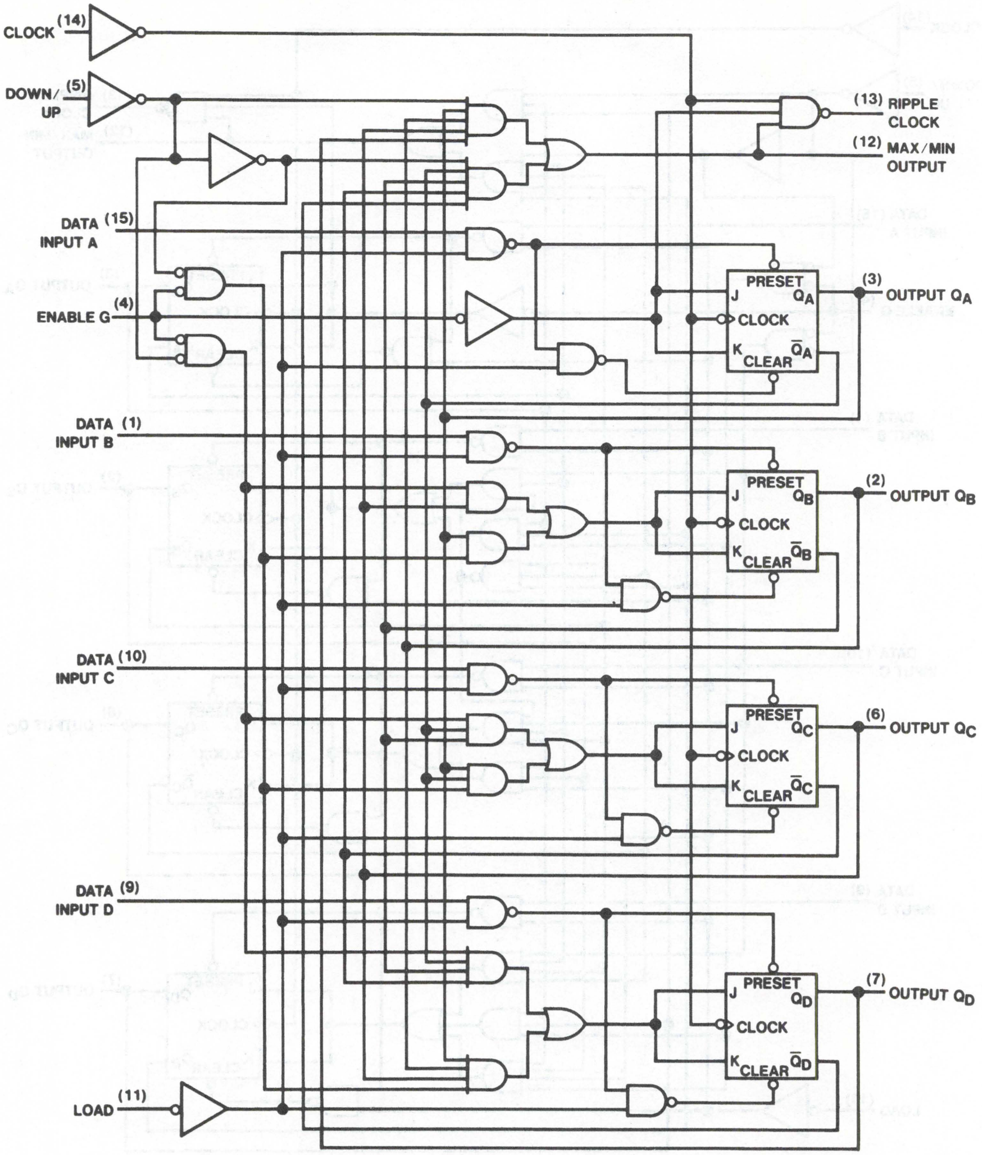

CLOCK (14)
DOWN/UP (5)
DATA INPUT A (15)
ENABLE G (4)
DATA INPUT B (1)
DATA INPUT C (10)
DATA INPUT D (9)
LOAD (11)
(13) RIPPLE CLOCK
(12) MAX/MIN OUTPUT
(3) OUTPUT Q_A
(2) OUTPUT Q_B
(6) OUTPUT Q_C
(7) OUTPUT Q_D
PRESET
J
CLOCK
K
CLEAR
Q_A
$\overline{Q}_A$
Q_B
$\overline{Q}_B$
Q_C
$\overline{Q}_C$
Q_D
$\overline{Q}_D$

Pin (16) = V_{CC}, Pin (8) = GND

TL/F/6405–2

Logic Diagrams (Continued)

LS191 Binary Counters


CLOCK (14)
DOWN/UP (5)
DATA INPUT A (15)
ENABLE G (4)
DATA INPUT B (1)
DATA INPUT C (10)
DATA INPUT D (9)
LOAD (11)
(13) RIPPLE CLOCK
(12) MAX/MIN OUTPUT
PRESET
J
CLOCK
K
CLEAR
Q_A
$\overline{Q}_A$
(3) OUTPUT Q_A
Q_B
$\overline{Q}_B$
(2) OUTPUT Q_B
Q_C
$\overline{Q}_C$
(6) OUTPUT Q_C
Q_D
$\overline{Q}_D$
(7) OUTPUT Q_D

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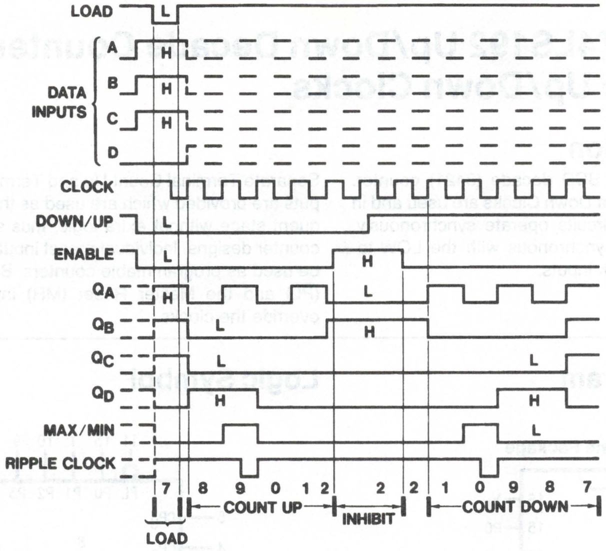
Pin (16) = V_{CC}, Pin (8) = GND

Timing Diagrams

LS190 Decade Counters
Typical Load, Count, and Inhibit Sequences


LOAD
L
DATA INPUTS
A
H
B
H
C
H
D
CLOCK
DOWN/UP
L
ENABLE
L
H
QA
H
L
QB
L
H
QC
L
L
QD
H
H
MAX/MIN
L
RIPPLE CLOCK
7
8
9
0
1
2
2
2
1
0
9
8
7
COUNT UP
INHIBIT
COUNT DOWN
LOAD

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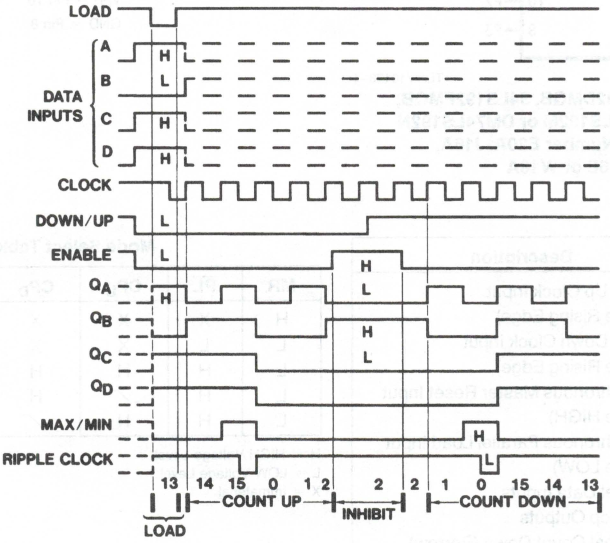
LS191 Binary Counters
Typical Load, Count, and Inhibit Sequences


LOAD
DATA INPUTS
A
H
B
L
C
H
D
H
CLOCK
DOWN/UP
L
ENABLE
L
H
QA
H
L
QB
H
QC
L
QD
MAX/MIN
H
RIPPLE CLOCK
L
13
14
15
0
1
2
2
2
1
0
15
14
13
COUNT UP
INHIBIT
COUNT DOWN
LOAD

TL/F/6405-5

National Semiconductor

54LS192/DM74LS192 Up/Down Decade Counter with Separate Up/Down Clocks

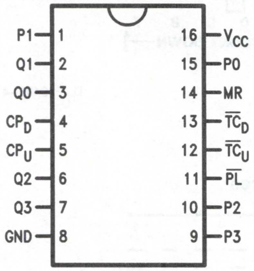
General Description

The 'LS192 is an up/down BCD decade (8421) counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

Connection Diagram

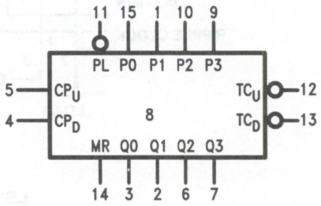
Dual-In-Line Package



TL/F/10178-1

Order Number 54LS192DMQB, 54LS192FMQB, 54LS192LMQB, DM74LS192M or DM74LS192N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Logic Symbol



TL/F/10178-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
CP_U	Count Up Clock Input (Active Rising Edge)
CP_D	Count Down Clock Input (Active Rising Edge)
MR	Asynchronous Master Reset Input (Active HIGH)
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
P0–P3	Parallel Data Inputs
Q0–Q3	Flip-Flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)

Mode Select Table

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↗	H	Count Up
L	H	H	↗	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS192			DM74LS192			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Voltage			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW Pn to $\overline{PL}$	20 20			20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW Pn to $\overline{PL}$	3 3			3 3			ns
t_w (L)	CP Pulse Width LOW	17			17			ns
t_w (L)	$\overline{PL}$ Pulse Width LOW	20			20			ns
t_w (H)	MR Pulse Width HIGH	15			15			ns
t_{rec}	Recovery Time, MR to CP	3			3			ns
t_{rec}	Recovery Time, $\overline{PL}$ to CP	10			10			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max, MR, $\overline{PL}$ = GND Other Inputs = 4.5V				31	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characterisitcs

$V_{CC} = +0.5V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$R_L = 2k$ $C_L = 15$ pF		Units
		Min	Max	
f_{max}	Maximum Count Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n		31 28	ns
t_{PLH} t_{PHL}	Propagation Delay CP_U to $\overline{TC}_U$		16 21	ns
t_{PLH} t_{PHL}	Propagation Delay CP_D to $\overline{TC}_D$		16 24	
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		20 30	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		32 30	ns
t_{PHL}	Propagation Delay, MR to Q_n		25	

Functional Description

The '192 is an asynchronously presettable decade and 4-bit binary synchronous up/down (reversible) counter. The operating modes of the '192 decade counter and the '193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagram. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up, and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

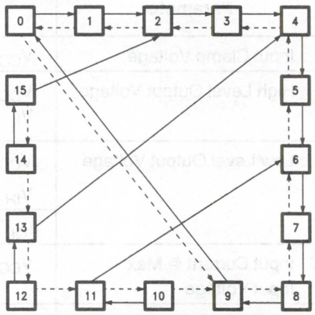
The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the '192, 15 for the '193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q0 \bullet Q3 \bullet \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q0} \bullet \overline{Q1} \bullet \overline{Q2} \bullet \overline{Q3} \bullet \overline{CP}_D$$

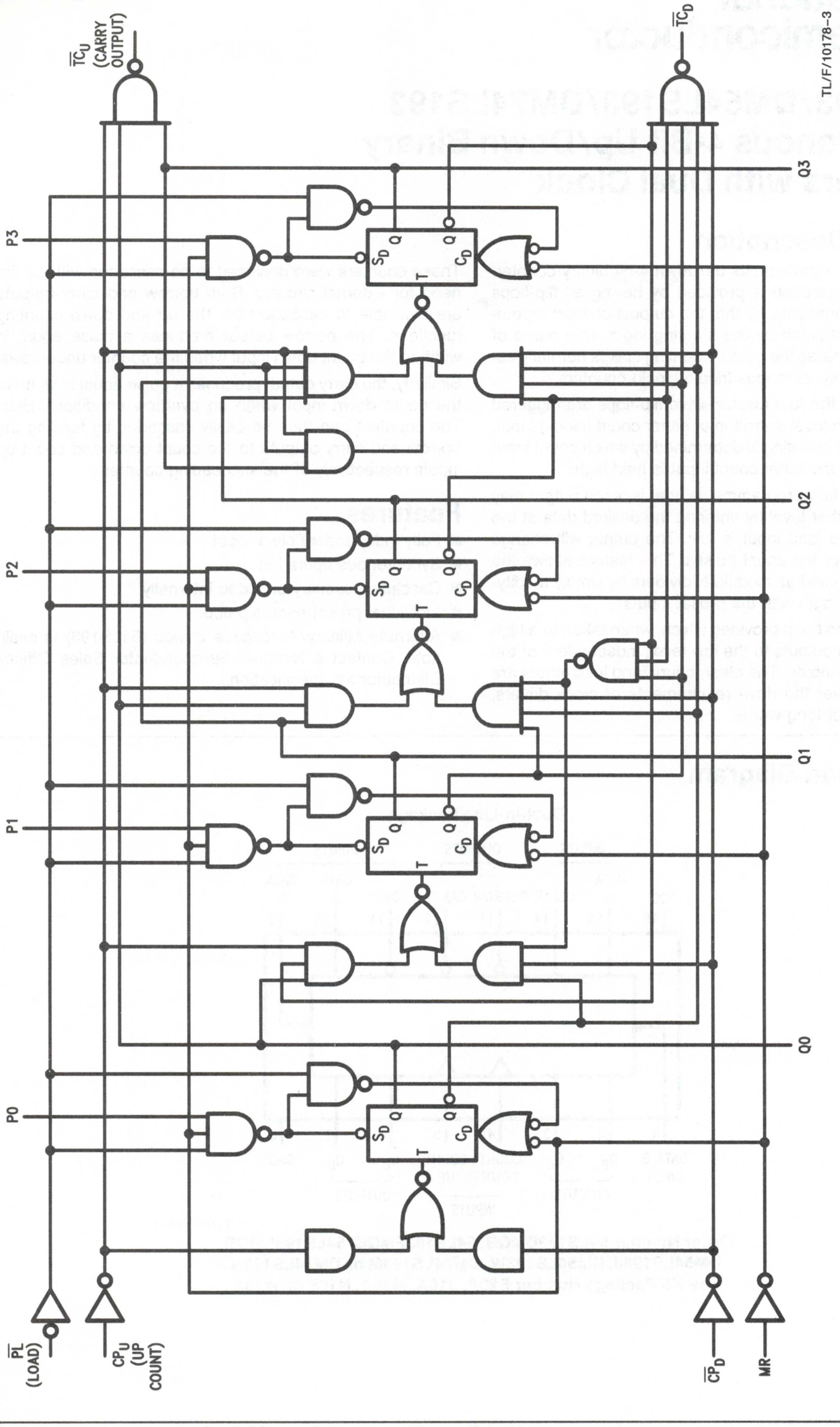
Each circuit has an asynchronous parallel load capability permitting the counter to be reset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P0–P3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

State Diagram



TL/F/10178-4

Logic Diagram


$\overline{TC}_U$ (CARRY OUTPUT)
$\overline{TC}_D$
P3
P2
P1
P0
Q3
Q2
Q1
Q0
S_D
C_D
Q
$\overline{Q}$
T
$\overline{PL}$ (LOAD)
CP_U (UP COUNT)
$\overline{CP}_D$
MR

TL/F/10178-3

National Semiconductor

54LS193/DM54LS193/DM74LS193 Synchronous 4-Bit Up/Down Binary Counters with Dual Clock

General Description

This circuit is a synchronous up/down 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is held high.

The counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

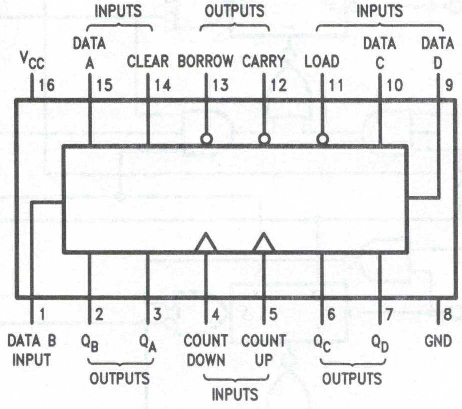
These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop
- Alternate Military/Aerospace device (54LS193) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6406–1

Order Number 54LS193DMQB, 54LS193FMQB, 54LS193LMQB, DM54LS193J, DM54LS193W, DM74LS193M or DM74LS193N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65° C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS193			DM74LS193			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
f_{CLK}	Clock Frequency (Note 1)	0		25	0		25	MHz
	Clock Frequency (Note 2)	0		20	0		20	MHz
t_W	Pulse Width of Any Input (Note 6)	20			20			ns
t_{SU}	Data Setup Time (Note 6)	20			20			ns
t_H	Data Hold Time (Note 6)	0			0			ns
t_{REL}	Release Time (Note 6)	40			40			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			19	34	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, I_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, I_A = 25°C and V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

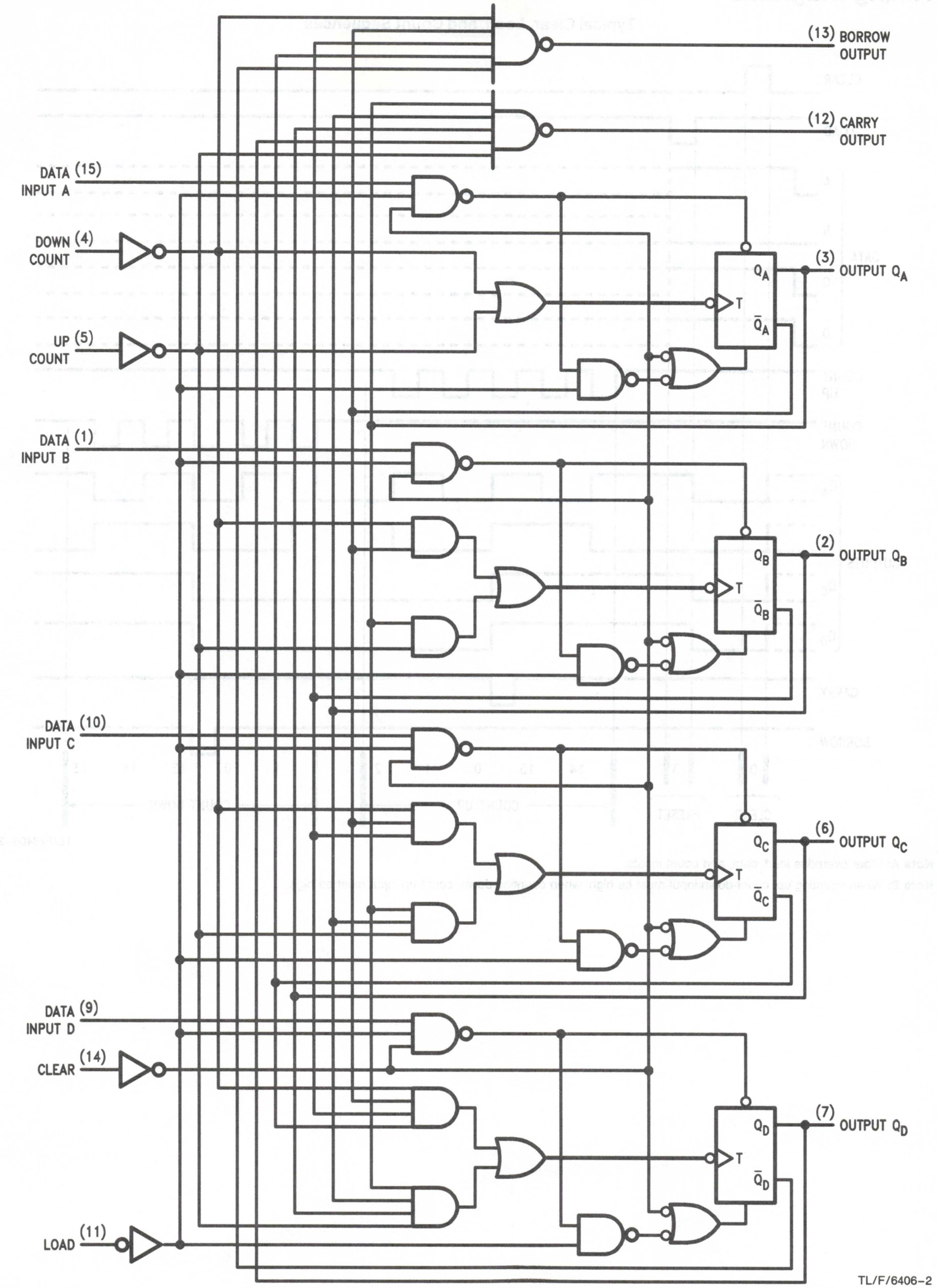
Note 5: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Count Up to Carry		26		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Count Up to Carry		24		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Count Down to Borrow		24		29	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Count Down to Borrow		24		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Either Count to Any Q		38		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Either Count to Any Q		47		54	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		40		41	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		40		47	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		35		44	ns

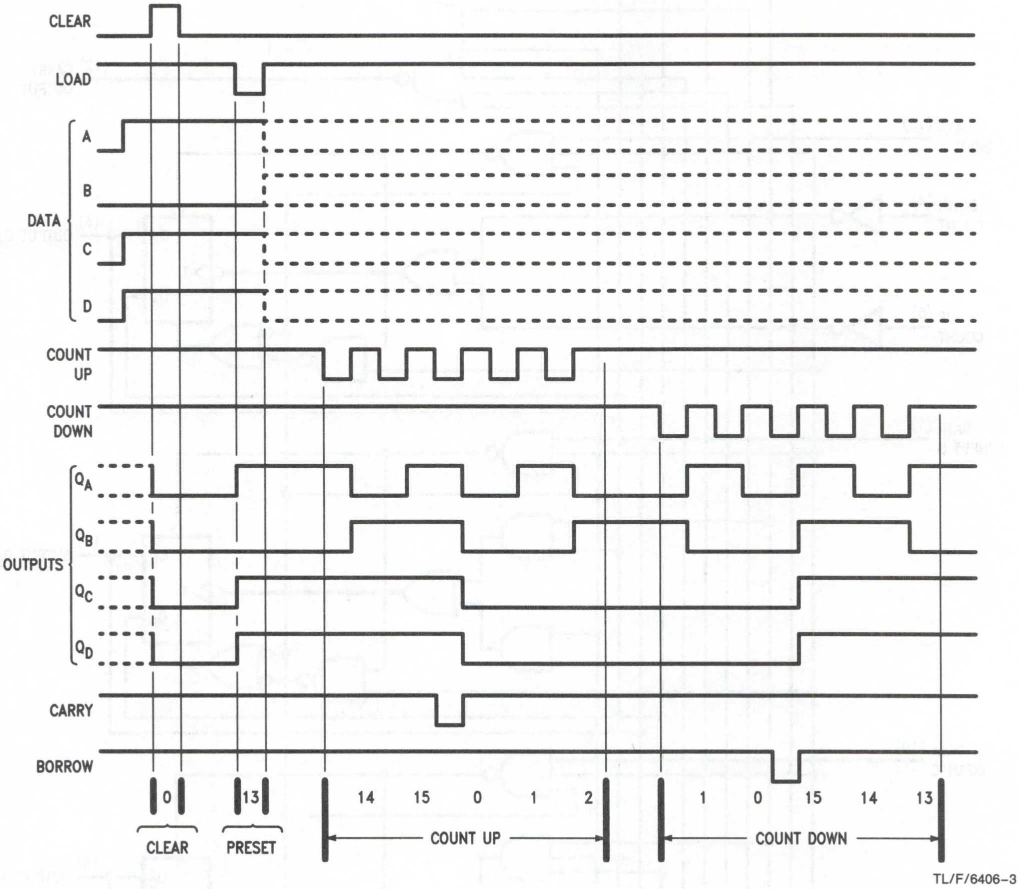
Logic Diagram


(13) BORROW OUTPUT
(12) CARRY OUTPUT
DATA INPUT A (15)
DOWN COUNT (4)
UP COUNT (5)
DATA INPUT B (1)
DATA INPUT C (10)
DATA INPUT D (9)
CLEAR (14)
LOAD (11)
(3) OUTPUT Q_A
(2) OUTPUT Q_B
(6) OUTPUT Q_C
(7) OUTPUT Q_D
Q_A
$\bar{Q}_A$
Q_B
$\bar{Q}_B$
Q_C
$\bar{Q}_C$
Q_D
$\bar{Q}_D$
T

TL/F/6406–2

Timing Diagrams

Typical Clear, Load, and Count Sequences


CLEAR
LOAD
DATA
A
B
C
D
COUNT UP
COUNT DOWN
OUTPUTS
Q_A
Q_B
Q_C
Q_D
CARRY
BORROW
0
13
14
15
0
1
2
1
0
15
14
13
CLEAR
PRESET
COUNT UP
COUNT DOWN
TL/F/6406–3

Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

National Semiconductor

54LS194A/DM74LS194A 4-Bit Bidirectional Universal Shift Register

General Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

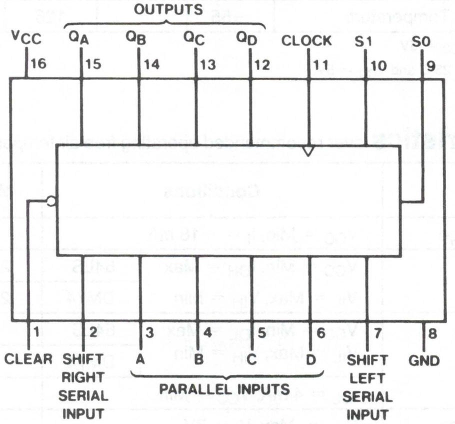
Clocking of the flip-flop is inhibited when both mode control inputs are low.

Features

- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear

Connection Diagram

Dual-In-Line Package



TL/F/6407–1

Order Number 54LS194ADMQB, 54LS194AFMQB, 54LS194ALMQB, DM74LS194AM or DM74LS194AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		54LS194A			DM74LS194A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		30		0	0		25	MHz
	Clock Frequency (Note 2)		22		0	0		20	
t_W	Pulse Width (Note 3)	Clock	17			20			ns
		Clear	12			20			
t_{SU}	Setup Time (Note 3)	Mode	25			30			ns
		Data	16			20			
t_H	Hold Time (Note 3)		0			0			ns
t_{REL}	Clear Release Time (Note 3)		18			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 2: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min				0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			15	23	mA

Note 4: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I_{CC} is tested with momentary ground, then 4.5V applied to CLOCK.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

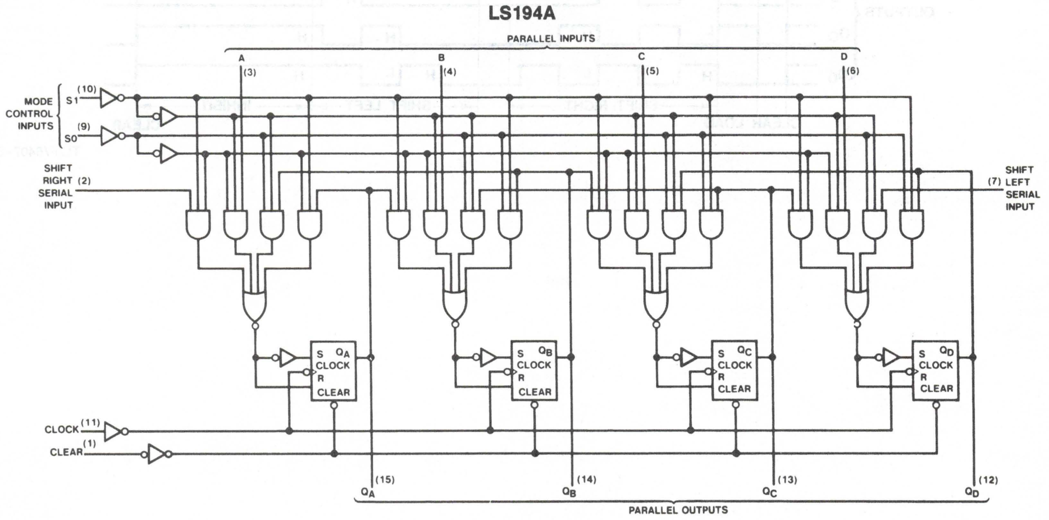
Symbol	Parameter	From (Input) To (Output)	54LS C_L = 15 pF		DM74LS C_L = 50 pF R_L = 2 kΩ		Units
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		21		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		24		35	ns
t_{PHL}	Propagation Delay Time High to Low Output	Clear to Any Q		26		38	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I_{CC} is tested with momentary ground, then 4.5V applied to CLOCK.

Logic Diagram


LS194A
PARALLEL INPUTS
A
(3)
B
(4)
C
(5)
D
(6)
MODE CONTROL INPUTS
S1
(10)
(9)
S0
SHIFT RIGHT SERIAL INPUT
(2)
SHIFT LEFT SERIAL INPUT
(7)
S
CLOCK
R
CLEAR
QA
QB
QC
QD
CLOCK
(11)
CLEAR
(1)
(15)
(14)
(13)
(12)
PARALLEL OUTPUTS

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Function Table

Inputs										Outputs			
Clear	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S0		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

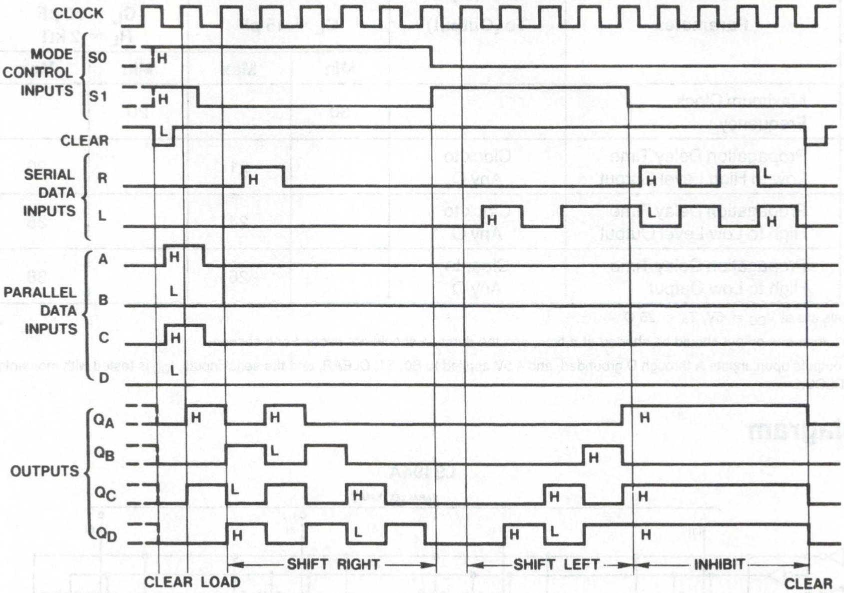
a, b, c, d = The level of steady state input at inputs A, B, C or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

Timing Diagram

Typical Clear, Load, Right-Shift, Left-Shift, Inhibit, and Clear Sequences


CLOCK
MODE CONTROL INPUTS
S0
S1
H
H
CLEAR
L
SERIAL DATA INPUTS
R
L
H
H
L
H
L
H
PARALLEL DATA INPUTS
A
B
C
D
H
L
H
L
OUTPUTS
Q_A
Q_B
Q_C
Q_D
H
H
L
L
H
H
L
H
H
H
H
L
H
SHIFT RIGHT
SHIFT LEFT
INHIBIT
CLEAR
LOAD
CLEAR

TL/F/6407–3

National Semiconductor

54LS195A/DM74LS195A
4-Bit Parallel Access Shift Register

General Description

This 4-bit register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load

Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

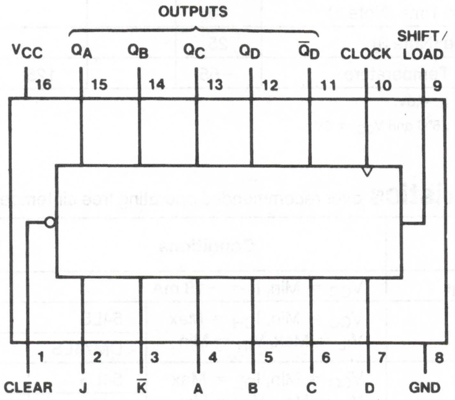
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T-type flip-flop as shown in the truth table.

Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- For use in high-performance:
  - accumulators/processors
  - serial-to-parallel, parallel-to-serial converters
- Typical clock frequency 39 MHz
- Typical power dissipation 70 mW

Connection Diagram

Dual-In-Line Package



TL/F/6408–1

Order Number 54LS195ADMQB, 54LS195AFMQB, 54LS195ALMQB, DM74LS195AM or DM74LS195AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		54LS195A			DM74LS195A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		30		0	0		30	MHz
	Clock Frequency (Note 2)		30		0	0		25	MHz
t_W	Pulse Width (Note 3)	Clock	16			16			ns
		Clear	14			12			
t_{SU}	Setup Time (Note 3)	Shift/Load	25			25			ns
		Data	15			15			
t_H	Hold Time (Note 3)		0			0			ns
t_{REL}	Shift/Load Release Time (Note 3)		10			10			ns
	Clear Release Time (Note 3)		25			25			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 2: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	54LS	2.5			V
			DM74LS	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74LS		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	54LS	−20		−100	mA
			DM74LS	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max, (Note 6)			14	21	mA

Note 4: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all inputs open, SHIFT/LOAD grounded, and 4.5V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, then 4.5V to the CLEAR and then applying a momentary ground then 4.5V to the CLOCK.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	54LS C_L = 15 pF		DM74LS R_L = 2 kΩ C_L = 50 pF		Units
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		21		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		24		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		26		38	ns

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

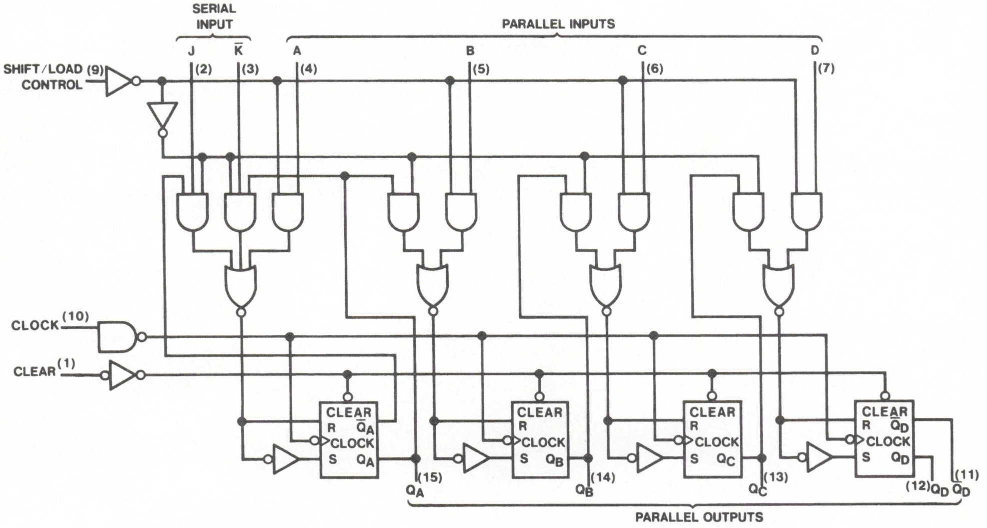
↑ = Transition from low to high level

a, b, c, d = The level of steady state input at A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent transition of the clock.

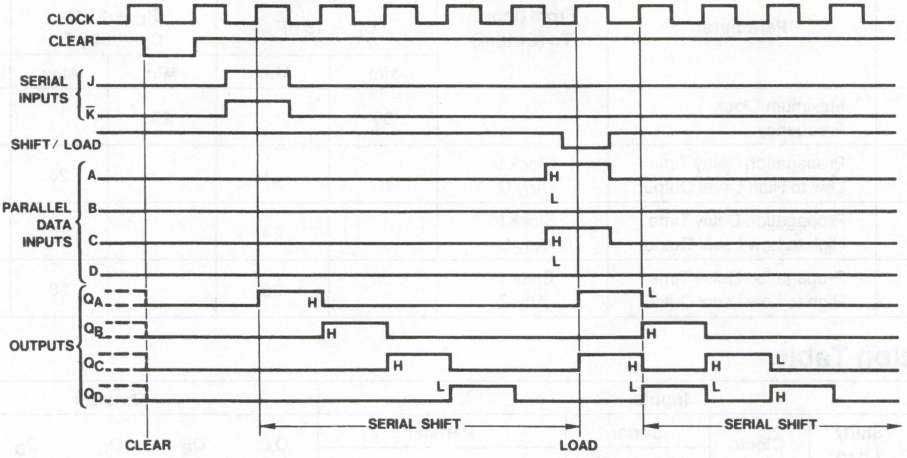
Logic Diagram


SERIAL INPUT
PARALLEL INPUTS
J
K̄
A
B
C
D
(2)
(3)
(4)
(5)
(6)
(7)
SHIFT/LOAD CONTROL (9)
CLOCK (10)
CLEAR (1)
CLEAR
R
Q̄A
CLOCK
S
QA
QB
QC
Q̄D
QD
(15)
(14)
(13)
(12)
(11)
PARALLEL OUTPUTS

TL/F/6408–2

Timing Diagram

Typical Clear, Shift, and Load Sequences


CLOCK
CLEAR
SERIAL INPUTS
J
K̄
SHIFT/ LOAD
PARALLEL DATA INPUTS
A
B
C
D
H
L
H
L
OUTPUTS
Q_A
Q_B
Q_C
Q_D
H
H
H
L
L
H
L
H
L
H
L
H
SERIAL SHIFT
SERIAL SHIFT
CLEAR
LOAD

TL/F/6408–3

National Semiconductor

DM74LS196
Presettable Decade Counter

General Description

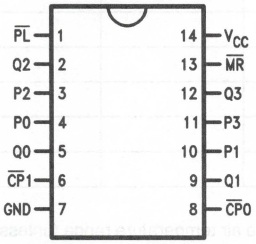
The 'LS196 decade ripple counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8421) sequence or in a bi-quinary mode producing a 50% duty cycle output. Both circuit types have a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (Pn) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH. In the counting modes, state changes are initiated by the falling edge of the clock.

Features

- High counting rates—typically 60 MHz
- Choice of counting modes—BCD, bi-quinary, binary
- Asynchronous preset and master reset

Connection Diagram

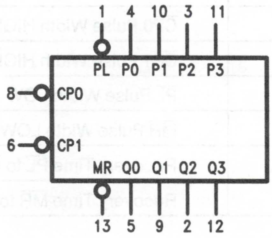
Dual-In-Line Package



TL/F/10179–1

Order Number DM74LS196M or DM74LS196N
See NS Package Number M14A or N14A

Logic Symbol



TL/F/10179–2

V_{CC} = Pin 14
GND = Pin 7

Pin Names	Description
$\overline{CP0}$	÷2 Section Clock Input (Active Falling Edge)
$\overline{CP1}$	÷5 Section Clock Input (Active Falling Edge)
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
P0–P3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
Q0–Q3	Flip-Flop Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS196			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW Pn to $\overline{\text{PL}}$	8 12			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW Pn to $\overline{\text{PL}}$	0 6			ns
t_w (H)	$\overline{\text{CP0}}$ Pulse Width HIGH	12			ns
t_w (H)	$\overline{\text{CP1}}$ Pulse Width HIGH	24			ns
t_w (L)	$\overline{\text{PL}}$ Pulse Width LOW	18			ns
t_w (L)	$\overline{\text{MR}}$ Pulse Width LOW	12			ns
t_{rec}	Recovery Time $\overline{\text{PL}}$ to $\overline{\text{CPn}}$	16			ns
t_{rec}	Recovery Time $\overline{\text{MR}}$ to $\overline{\text{CPn}}$	18			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 5.5V, $\overline{\text{CP1}}$			40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max, V_{IN} = GND			20	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	R_L = 2k C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Count Frequency at $\overline{CP}0$	45		MHz
f_{max}	Maximum Count Frequency at $\overline{CP}1$	22.5		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}0$ to Q0		15 15	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}1$ to Q1		15 15	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}1$ to Q2		34 34	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}1$ to Q3		15 21	ns
t_{PLH} t_{PHL}	Propagation Delay Pn to Qn		25 35	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Qn		31 37	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Qn		42	ns

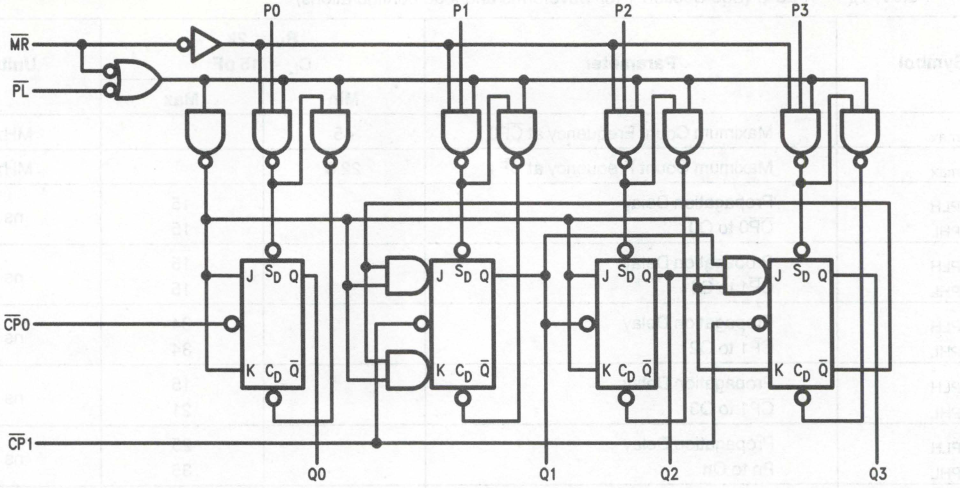
Functional Description

The '196 and '197 are asynchronous presettable decade and binary ripple counters. The '196 decade counter is partitioned into divide-by-two and divide-by-five sections while the '197 is partitioned into divide-by-two and divide-by-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH-to-LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP}0$ input serves the Q0 flip-flop in both circuit types while the $\overline{CP}1$ input serves the divide-by-five or divide-by-eight section. The Q0 output is designed and specified to drive the rated fan-out plus the $\overline{CP}1$ input. With the input frequency connected to $\overline{CP}0$ and with Q0 driving $\overline{CP}1$, the '197 forms a straight forward modulo-16 counter, with Q0 the least significant output and Q3 the most significant output.

The '196 decade counter can be connected up to operate in two different count sequences. With the input frequency connected to $\overline{CP}0$ and with Q0 driving $\overline{CP}1$, the circuit counts in the BCD (8421) sequence. With the input frequency connected to $\overline{CP}1$ and Q3 driving $\overline{CP}0$, Q0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

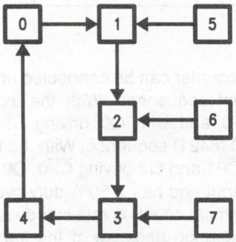
The '196 and '197 have an asynchronous active LOW Master Reset input ($\overline{MR}$) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input ($\overline{PL}$) overrides the clock inputs and loads the data from Parallel Data (P0–P3) inputs into the flip-flops. While $\overline{PL}$ is LOW, the counters act as transparent latches and any change in the Pn inputs will be reflected in the outputs. In order for the intended parallel data to be entered and stored, the recommended setup and hold times with respect to the rising edge of $\overline{PL}$ should be observed.

Logic Diagram


P0
P1
P2
P3
$\overline{MR}$
$\overline{PL}$
$\overline{CP0}$
$\overline{CP1}$
J
S_D
Q
K
C_D
$\overline{Q}$
Q0
Q1
Q2
Q3

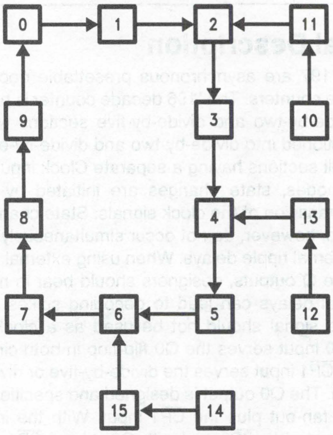
TL/F/10179-3

÷5 State Diagram



TL/F/10179-4

BCD State Diagram


0
1
2
11
9
3
10
8
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13
7
6
5
12
15
14

TL/F/10179-5

Mode Select Table

Inputs			Response
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Qn forced LOW
H	L	X	Pn → Qn
H	H	⎺╲⎽	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

National Semiconductor

DM74LS197 Presettable Binary Counters

General Description

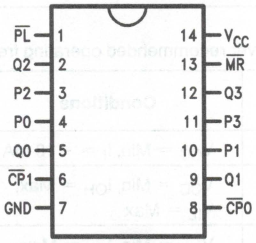
The 'LS197 ripple counter contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. State changes are initiated by the falling edge of the clock. The 'LS197 has a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuit usable as a programmable counter. The circuit can also be used as a 4-bit latch, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH. For detail specifications and functional description, please refer to the 'LS196 data sheet.

Features

- High counting rates—Typically 70 MHz
- Asynchronous preset
- Asynchronous master reset

Connection Diagram

Dual-In-Line Package



TL/F/10180-1

Order Number DM74LS197M or DM74LS197N
See NS Package Number M14A or N14A

Pin Names	Description
$\overline{CP0}$	÷2 Section Clock Input (Active Falling Edge)
$\overline{CP1}$	÷8 Section Clock Input (Active Falling Edge)
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
P0–P3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
Q0	÷2 Section Output*
Q1–Q3	÷8 Section Outputs

*Q0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP1}$ input.

Mode Select Table

Inputs			Response
$\overline{MR}$	$\overline{PL}$	CP	
L	X	X	Qn Forced LOW
H	L	X	Pn → Qn
H	H	↘	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	74LS197			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Voltage			−0.4	mA
I_{OL}	Low Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

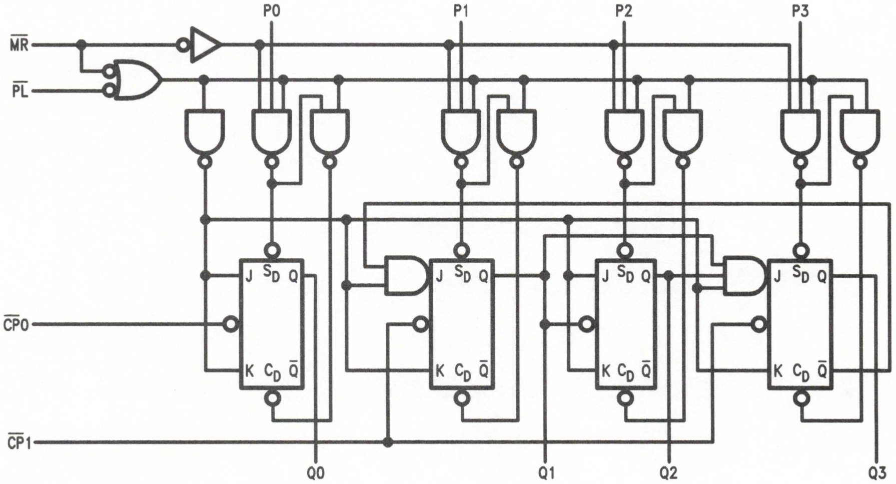
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for Test Waveforms and Output Loads)

Symbol	Parameter	$R_L = 2\ k\Omega$ $C_L = 15\ pF$		Units
		Min	Max	
f_{MAX}	Max CLK Frequency	55		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{CP0}}$ to Q0		15 15	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{CP1}}$ to Q2		34 34	ns
t_{PLH} t_{PHL}	Propagation Delay P2 to Q2		27 44	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{PL}}$ to Q2		39 45	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{CP1}}$ to Q1		15 17	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{CP1}}$ to Q3		55 63	ns
t_{PHL}	Propagation Delay $\overline{\text{MR}}$ to Q3		42	ns

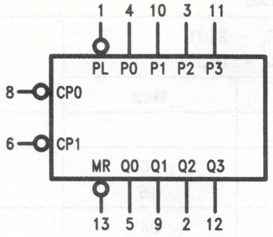
Logic Diagram



TL/F/10180-4

2

Logic Symbol


1
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PL
P0
P1
P2
P3
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CP0
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CP1
MR
Q0
Q1
Q2
Q3
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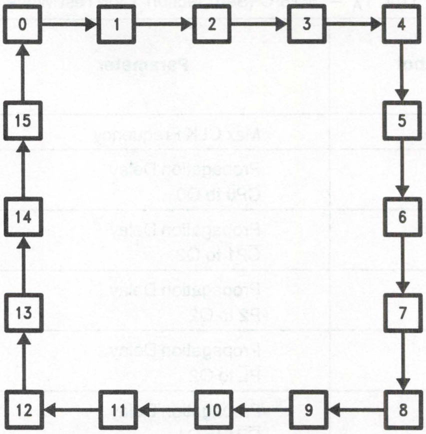
TL/F/10180-2

V_{CC} = Pin 14

GND = Pin 7

÷ 16 State Diagram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TL/F/10180-3

National Semiconductor

DM74LS221 Dual Non-Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM74LS221 is a dual monostable multivibrator with Schmitt-trigger input. Each device has three inputs permitting the choice of either leading-edge or trailing-edge triggering. Pin (A) is an active-low trigger transition input and pin (B) is an active-high transition Schmitt-trigger input that allows jitter free triggering for inputs with transition rates as slow as 1 volt/second. This provides the input with excellent noise immunity. Additionally an internal latching circuit at the input stage also provides a high immunity to V_{CC} noise. The clear (CLR) input can terminate the output pulse at a predetermined time independent of the timing components. This (CLR) input also serves as a trigger input when it is pulsed with a low level pulse transition (⊔). To obtain the best and trouble free operation from this device please read operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

Features

- A dual, highly stable one-shot
- Compensated for V_{CC} and temperature variations
- Pin-out identical to 'LS123 (Note 1)
- Output pulse width range from 30 ns to 70 seconds
- Hysteresis provided at (B) input for added noise immunity
- Direct reset terminates output pulse
- Triggerable from CLEAR input
- DTL, TTL compatible
- Input clamp diodes

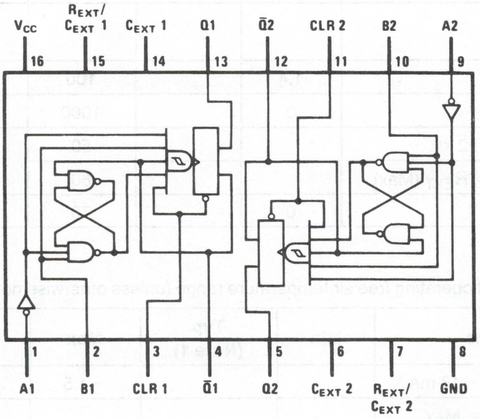
Note 1: The pin-out is identical to 'LS123 but, functionally it is not; refer to Operating Rules #10 in this datasheet.

Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width is independent of further input transitions and is a function of the timing components, or it may be reduced or terminated by use of the active low CLEAR input. Stable output pulse width ranging from 30 ns to 70 seconds is readily obtainable.

Connection Diagram

Dual-In-Line Package



TL/F/6409–1

Order Number DM74LS221M or DM74LS221N
See NS Package Number M16A or N16A

Function Table

Inputs			Outputs	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
* ↑	L	H	⊓	⊔

H = High Logic Level

L = Low Logic Level

X = Can Be Either Low or High

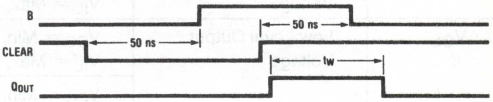
↑ = Positive Going Transition

↑ = Negative Going Transition

⊓ = A Positive Pulse

⊔ = A Negative Pulse

*This mode of triggering requires first the B input be set from a low to high level while the CLEAR input is maintained at logic low level. Then with the B input at logic high level, the CLEAR input whose positive transition from low to high will trigger an output pulse.



TL/F/6409–2

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74LS221			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage at the A Input (V_{CC} = Min)				2	V
V_{T-}	Negative-Going Input Threshold Voltage at the A Input (V_{CC} = Min)		0.8	1		V
V_{T+}	Positive-Going Input Threshold Voltage at the B Input (V_{CC} = Min)			1	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the B Input (V_{CC} = Min)		0.8	0.9		V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
t_W	Pulse Width (Note 1)	Data	40			ns
		Clear	40			
t_{REL}	Clear Release Time (Note 1)		15			ns
$\frac{dV}{dt}$	Rate of Rise or Fall of Schmitt Input (B) (Note 1)				1	$\frac{V}{s}$
$\frac{dV}{dt}$	Rate of Rise or Fall of Logic Input (A) (Note 1)				1	$\frac{V}{\mu s}$
R_{EXT}	External Timing Resistor (Note 1)		1.4		100	kΩ
C_{EXT}	External Timing Capacitance (Note 1)		0		1000	µF
DC	Duty Cycle (Note 1)	$R_T = 2\ k\Omega$			50	%
		$R_T = R_{EXT}$ (Max)			60	
T_A	Free Air Operating Temperature		0		70	°C

Note 1: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		V_{CC} = Min, I_{OL} = 4 mA			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	A1, A2			−0.4	mA
			B			−0.8	
			Clear			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max	Quiescent		4.7	11	mA
			Triggered		19	27	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	A1, A2 to Q	C_{EXT} = 80 pF R_{EXT} = 2 kΩ C_L = 15 pF R_L = 2 kΩ		70	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q			55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A1, A2 to Q			80	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to $\overline{Q}$			65	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$			65	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q			55	ns
$t_{W(out)}$	Output Pulse Width Using Zero Timing Capacitance	A1, A2 to Q, $\overline{Q}$	C_{EXT} = 0 R_{EXT} = 2 kΩ R_L = 2 kΩ C_L = 15 pF	20	70	ns
$t_{W(out)}$	Output Pulse Width Using External Timing Resistor	A1, A2 to Q, $\overline{Q}$	C_{EXT} = 100 pF R_{EXT} = 10 kΩ R_L = 2 kΩ C_L = 15 pF	600	750	ns
			C_{EXT} = 1 μF R_{EXT} = 10 kΩ R_L = 2 kΩ C_L = 15 pF	6	7.5	ms
			C_{EXT} = 80 pF R_{EXT} = 2 kΩ R_L = 2 kΩ C_L = 15 pF	70	150	ns

Operating Rules

1. An external resistor (R_X) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to approximately 1000 μF. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitor may be used. For large time constants use tantalum or special aluminum capacitors. If timing capacitor has leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current. This switching diode is not needed for the 'LS221 one-shot and should not be used.
3. For $C_X >> 1000$ pF, the output pulse width (T_W) is defined as follows:

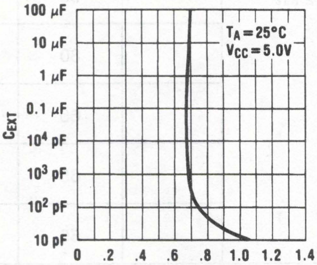
   $T_W = KR_X C_X$

   where [R_X is in kΩ]

   [C_X is in pF]

   [T_W is in ns]

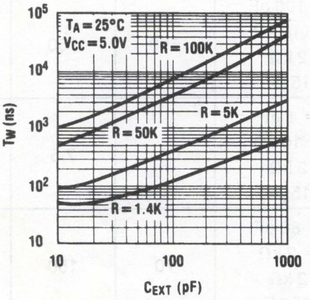
   $K \approx \text{Ln}2 = 0.70$
4. The multiplicative factor K is plotted as a function of C_X below for design considerations:



TL/F/6409-3

FIGURE 1

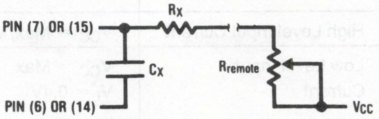
5. For $C_X < 1000$ pF see *Figure 2* for T_W vs C_X family curves with R_X as a parameter:



TL/F/6409-4

FIGURE 2

6. To obtain variable pulse widths by remote trimming, the following circuit is recommended:

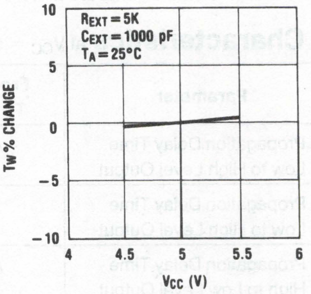


TL/F/6409-5

Note: "R_{remote}" should be as close to the one-shot as possible.

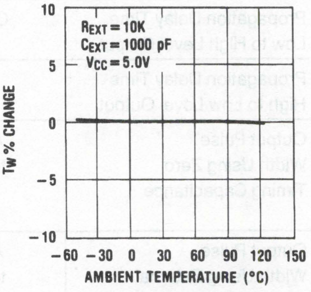
FIGURE 3

7. Output pulse width versus V_{CC} and temperatures: *Figure 4* depicts the relationship between pulse width variation versus V_{CC}. *Figure 5* depicts pulse width variation versus temperatures.



TL/F/6409-6

FIGURE 4



TL/F/6409-7

FIGURE 5

8. Duty cycle is defined as $T_W/T \times 100$ in percentage, if it goes above 50% the output pulse width will become shorter. If the duty cycle varies between low and high values, this causes output pulse width to vary, or jitter (a function of the R_{EXT} only). To reduce jitter, R_{EXT} should be as large as possible, for example, with $R_{EXT} = 100$k jitter is not appreciable until the duty cycle approaches 90%.

Operating Rules (Continued)

9. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.
10. Although the 'LS221's pin-out is identical to the 'LS123 it should be remembered that they are not functionally identical. The 'LS123 is a retriggerable device such that the output is dependent upon the input transitions when its output "Q" is at the "High" state. Furthermore, it is recommended for the 'LS123 to externally ground the C_{EXT} pin for improved system performance. However, this pin on the 'LS221 is not an internal connection to the device ground. Hence, if substitution of an 'LS221 onto an 'LS123 design layout where the C_{EXT} pin is wired to the ground, the device will not function.
11. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 μF to 0.10 μF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC}-pin as space permits.

For further detailed device characteristics and output performance, please refer to the NSC one-shot application note AN-366.

National Semiconductor

54LS240/DM54LS240/DM74LS240, 54LS241/DM54LS241/DM74LS241 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

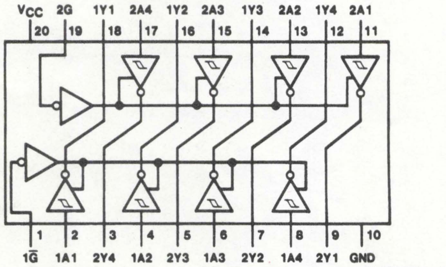
These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at data inputs improves noise margins
- Typical I_{OL} (sink current)
    - 54LS 12 mA
    - 74LS 24 mA
- Typical I_{OH} (source current)
    - 54LS −12 mA
    - 74LS −15 mA
- Typical propagation delay times
    - Inverting 10.5 ns
    - Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
    - Inverting 130 mW
    - Noninverting 135 mW
- Alternate Military/Aerospace devices (54LS240/54LS241) are available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

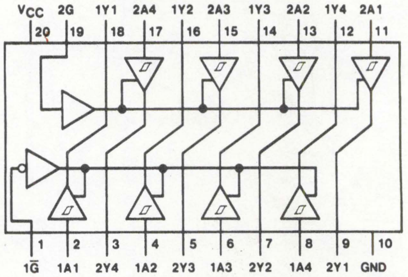
Dual-In-Line Package


VCC
2G
1Y1
2A4
1Y2
2A3
1Y3
2A2
1Y4
2A1
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
1G̅
1A1
2Y4
1A2
2Y3
1A3
2Y2
1A4
2Y1
GND

TL/F/6411-1

Order Number 54LS240DMQB, 54LS240FMQB, 54LS240LMQB, DM54LS240J, DM74LS240WM or DM74LS240N
See NS Package Number E20A, J20A, M20B, N20A or W20A

Dual-In-Line Package


VCC
2G
1Y1
2A4
1Y2
2A3
1Y3
2A2
1Y4
2A1
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
1G̅
1A1
2Y4
1A2
2Y3
1A3
2Y2
1A4
2Y1
GND

TL/F/6411-2

Order Number 54LS241DMQB, 54LS241FMQB, 54LS241LMQB, DM54LS241J, DM74LS241WM or DM74LS241N
See NS Package Number E20A, J20A, M20B, N20A or W20A

Function Tables

LS240

Inputs		Output
$\overline{G}$ 1	A	Y
L	L	H
L	H	L
H	X	Z

LS241

Inputs				Outputs	
G	$\overline{G}$	1A	2A	1Y	2Y
X	L	L	X	L	
X	L	H	X	H	
X	H	X	X	Z	
H	X	X	L		L
H	X	X	H		H
L	X	X	X		Z

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Z = High Impedance

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS, 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS240, 241			DM74LS240, 241			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$) Data Inputs Only	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −3 mA		DM54/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min V_{IL} = 0.5V, I_{OH} = Max		DM54/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = Max V_{IH} = Min	I_{OL} = 12 mA	DM74			0.4	V
			I_{OL} = Max	DM54			0.4	
				DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max V_{IL} = Max V_{IH} = Min	V_O = 2.7V				20	µA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−20	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V (DM74) V_I = 10V (DM54)					0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	Outputs High	LS240, LS241		13	23	mA
			Outputs Low	LS240		26	44	
				LS241		27	46	
			Outputs Disabled	LS240		29	50	
				LS241		32	54	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions		DM54LS Max	DM74LS Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF R_L = 667Ω	LS240	18	14	ns
			LS241	18	18	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 45 pF R_L = 667Ω	LS240	18	18	ns
			LS241	18	18	
t_{PZL}	Output Enable Time to Low Level	C_L = 45 pF R_L = 667Ω	LS240	30	30	ns
			LS241	30	30	
t_{PZH}	Output Enable Time to High Level	C_L = 45 pF R_L = 667Ω	LS240	23	23	ns
			LS241	23	23	
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF R_L = 667Ω	LS240	25	25	ns
			LS241	25	25	
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF R_L = 667Ω	LS240	18	18	ns
			LS241	18	18	
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 150 pF R_L = 667Ω	LS240		18	ns
			LS241		21	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 150 pF R_L = 667Ω	LS240		22	ns
			LS241		22	
t_{PZL}	Output Enable Time to Low Level	C_L = 150 pF R_L = 667Ω	LS240		33	ns
			LS241		33	
t_{PZH}	Output Enable Time to High Level	C_L = 150 pF R_L = 667Ω	LS240		26	ns
			LS241		26	

Note: 54LS Output load is C_L = 50 pF for t_{PLH}, t_{PHL}, t_{PZL} and t_{PZH}.

National Semiconductor

DM74LS243 Quadruple Bus Transceiver

General Description

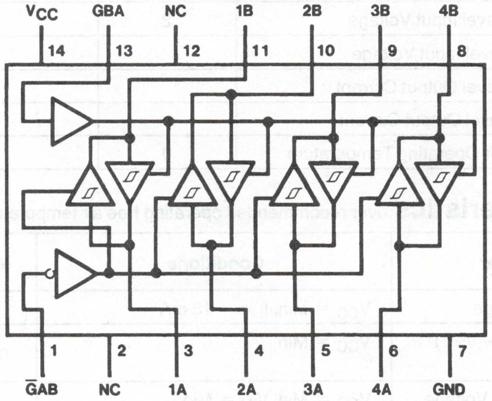
This four data line transceiver is designed for asynchronous two-way communications between data buses. It can be used to drive terminated lines down to 133Ω.

Features

- Two-way asynchronous communication between data buses
- PNP inputs reduce DC loading on bus line
- Hysteresis at data inputs improves noise margin

Connection Diagram

Dual-In-Line Package



TL/F/6412–1

Order Number DM74LS243WM or DM74LS243N
See NS Package Number M14B or N14A

Function Table

Control Inputs		Data Port Status	
$\overline{GAB}$	GBA	A	B
H	H	O	I
L	H	*	*
H	L	ISOLATED	
L	L	I	O

*Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.

I = Input, O = Output.

H = High Logic Level, L = Low Logic Level.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Any G	7V
A or B	5.5V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS243			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$) (Data Inputs Only)	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −1 mA			2.7			V
		V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −3 mA			2.4	3.4		
		V_{CC} = Min, V_{IH} = Min V_{IL} = 0.5V, I_{OH} = Max			2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = Max V_{IH} = Min	I_{OL} = 12 mA				0.4	V
			I_{OL} = Max				0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max V_{IL} = Max V_{IH} = Min	V_O = 2.7V				40	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−200	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V	A or B			0.1	mA
			V_I = 7V	Any G			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	V_{CC} = Max Outputs Open	Outputs High			22	38	mA
			Outputs Low			29	50	
			Outputs Disabled			32	54	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 45\ pF$ $R_L = 667\Omega$		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 45\ pF$ $R_L = 667\Omega$		18	ns
t_{PZL}	Output Enable Time to Low Level	$C_L = 45\ pF$ $R_L = 667\Omega$		30	ns
t_{PZH}	Output Enable Time to High Level	$C_L = 45\ pF$ $R_L = 667\Omega$		23	ns
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5\ pF$ $R_L = 667\Omega$		25	ns
t_{PHZ}	Output Disable Time from High Level	$C_L = 5\ pF$ $R_L = 667\Omega$		18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 150\ pF$ $R_L = 667\Omega$		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 150\ pF$ $R_L = 667\Omega$		22	ns
t_{PZL}	Output Enable Time to Low Level	$C_L = 150\ pF$ $R_L = 667\Omega$		33	ns
t_{PZH}	Output Enable Time to High Level	$C_L = 150\ pF$ $R_L = 667\Omega$		26	ns

National Semiconductor

54LS244/DM74LS244 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

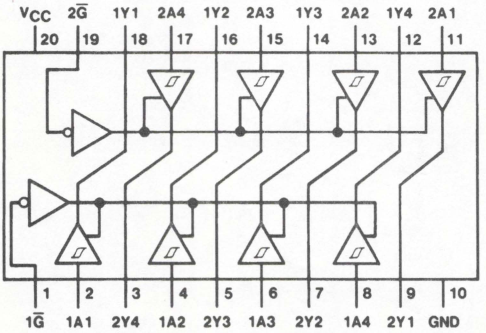
These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at data inputs improves noise margins
- Typical I_{OL} (sink current)
  - 54LS 12 mA
  - 74LS 24 mA
- Typical I_{OH} (source current)
  - 54LS −12 mA
  - 74LS −15 mA
- Typical propagation delay times
  - Inverting 10.5 ns
  - Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
  - Inverting 130 mW
  - Noninverting 135 mW

Connection Diagram

Dual-In-Line Package



TL/F/8442-1

Order Number 54LS244DMQB, 54LS244FMQB, 54LS244LMQB, DM74LS244WM or DM74LS244N
See NS Package Number E20A, J20A, M20B, N20A or W20A

Function Table

Inputs		Output
G̅	A	Y
L	L	L
L	H	H
H	X	Z

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Z = High Impedance

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS244			DM74LS244			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$) Data Inputs Only	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −3 mA		54LS/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min V_{IL} = 0.5V, I_{OH} = Max		54LS/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = Max V_{IH} = Min	I_{OL} = 12 mA	54LS/DM74			0.4	V
			I_{OL} = Max	DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max V_{IL} = Max V_{IH} = Min	V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 7V (DM74) V_I = 10V (54LS)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V		−0.5		−200	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		54LS	−50		−225	mA
				DM74	−40			
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	Outputs High			13	23	mA
			Outputs Low			27	46	
			Outputs Disabled			32	54	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $V_{CC} = 5V$, $T_A = 25°C$ (see Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	54LS Max	DM74LS Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 45$ pF $R_L = 667\Omega$	18	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 45$ pF $R_L = 667\Omega$	18	18	ns
t_{PZL}	Output Enable Time to Low Level	$C_L = 45$ pF $R_L = 667\Omega$	30	30	ns
t_{PZH}	Output Enable Time to High Level	$C_L = 45$ pF $R_L = 667\Omega$	23	23	ns
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5$ pF $R_L = 667\Omega$	25	25	ns
t_{PHZ}	Output Disable Time from High Level	$C_L = 5$ pF $R_L = 667\Omega$	18	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 150$ pF $R_L = 667\Omega$		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 150$ pF $R_L = 667\Omega$		22	ns
t_{PZL}	Output Enable Time to Low Level	$C_L = 150$ pF $R_L = 667\Omega$		33	ns
t_{PZH}	Output Enable Time to High Level	$C_L = 150$ pF $R_L = 667\Omega$		26	ns

Note: 54LS Output Load is $C_L = 50$ pF for t_{PLH}, t_{PHL}, t_{PZL} and t_{PZH}.

National Semiconductor

54LS245/DM54LS245/DM74LS245 TRI-STATE® Octal Bus Transceiver

General Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

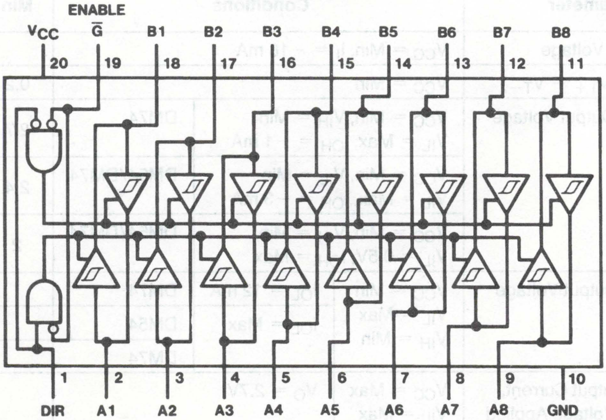
The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

Features

- Bi-Directional bus transceiver in a high-density 20-pin package
- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at bus inputs improve noise margins
- Typical propagation delay times, port-to-port 8 ns
- Typical enable/disable times 17 ns
- I_{OL} (sink current)
  - 54LS 12 mA
  - 74LS 24 mA
- I_{OH} (source current)
  - 54LS −12 mA
  - 74LS −15 mA
- Alternate Military/Aerospace device (54LS245) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6413–1

Order Number 54LS245DMQB, 54LS245FMQB, 54LS245LMQB, DM54LS245J, DM54LS245W, DM74LS245WM or DM74LS245N
See NS Package Number E20A, J20A, M20B, N20A or W20A

Function Table

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High Level, L = Low Level, X = Irrelevant

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
DIR or $\overline{G}$	7V
A or B	5.5V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS245			DM74LS245			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IL} = Min V_{IL} = Max, I_{OH} = −3 mA		DM54/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min V_{IL} = 0.5V, I_{OH} = Max		DM54/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = Max V_{IH} = Min	I_{OL} = 12 mA	DM74			0.4	V
			I_{OL} = Max	DM54			0.4	
				DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max V_{IL} = Max V_{IH} = Min	V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−200	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	A or B	V_I = 5.5V			0.1	mA
			DIR or $\overline{G}$	V_I = 7V			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	Outputs High		V_{CC} = Max		48	70	mA
		Outputs Low				62	90	
		Outputs at Hi-Z				64	95	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, not to exceed one second duration

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	DM54/74 LS245 Min	DM54/74 LS245 Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	$C_L = 45$ pF $R_L = 667\Omega$		12	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			12	ns
t_{PZL}	Output Enable Time to Low Level			40	ns
t_{PZH}	Output Enable Time to High Level			40	ns
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5$ pF $R_L = 667\Omega$		25	ns
t_{PHZ}	Output Disable Time from High Level			25	ns
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	$C_L = 150$ pF $R_L = 667\Omega$		16	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			17	ns
t_{PZL}	Output Enable Time to Low Level			45	ns
t_{PZH}	Output Enable Time to High Level			45	ns

National Semiconductor

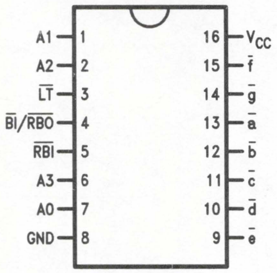
54LS247/DM74LS247
BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

General Description

The 'LS247 has active LOW open-collector outputs guaranteed to sink 12 mA (Military) or 24 mA (Commercial). It has the same electrial characteristics and pin connections as the 'LS47. The only difference is that the 'LS247 will ight the top bar (segment a) for numeral 6 and the bottom bar (segment d) for number 9. For detailed description and specifications please refer to the 'LS47 data sheet.

Connection Diagram

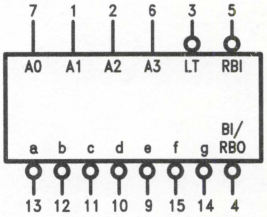
Dual-In-Line Package


A1 1
A2 2
$\overline{LT}$ 3
$\overline{BI}/\overline{RBO}$ 4
$\overline{RBI}$ 5
A3 6
A0 7
GND 8
16 V_{CC}
15 $\overline{f}$
14 $\overline{g}$
13 $\overline{a}$
12 $\overline{b}$
11 $\overline{c}$
10 $\overline{d}$
9 $\overline{e}$

TL/F/9822-1

Order Number 54LS247DMQB, 54LS247FMQB, DM74LS247M or DM74LS247N
See NS Package Number J16A, M16A, N16E or W16A

Logic Symbol


7 1 2 6 3 5
A0 A1 A2 A3 LT RBI
a b c d e f g BI/RBO
13 12 11 10 9 15 14 4

TL/F/9822-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI}/\overline{RBO}$	Blanking Input (Avtive LOW) or Ripple Blanking Output (Active LOW)
$\overline{a}$–$\overline{g}$	Segment Outputs (Active LOW)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS247			DM74LS247			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−50			−50	μa
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	54LS	2.4			V
			DM74LS	2.4	3.4		
I_{OFF}	Output High Current Segement Outputs	V_{CC} = 5.5V, V_M = 15V				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS			0.5	V
			DM74LS		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74LS		0.25	0.5	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
		V_{CC} = Max, V_I = 0.4V $\overline{BI}/\overline{RBO}$ Input				−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−0.3		−2.0	mA
			DM74LS	−0.3		−2.0	
I_{CC}	Supply Current	V_{CC} = Max				13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = +5V$, $T_A = +25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 2\ k\Omega$ (54LS = 665Ω) $C_L = 15\ pF$ Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output		100	ns
t_{PLH}	Propagation Delay Time High to Low Level Output		100	ns

National Semiconductor

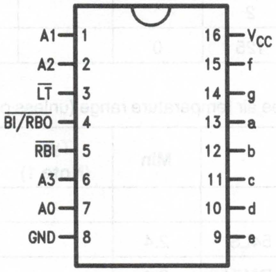
54LS248/DM74LS248 BCD to 7-Segment Decoder (with 2 kΩ Pull-Up Resistors)

General Description

The 'LS248 has active HIGH outputs with internal 2 kΩ pull-up resistors. It has the same electrical characteristics and pin connections as the 'LS48. The only difference is that the 'LS248 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9. For detailed description and specifications please refer to the 'LS48 data sheet.

Connection Diagram

Dual-In-Line Package

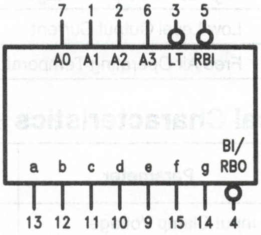


A1 1
A2 2
$\overline{LT}$ 3
$\overline{BI}/\overline{RBO}$ 4
$\overline{RBI}$ 5
A3 6
A0 7
GND 8
16 V_{CC}
15 f
14 g
13 a
12 b
11 c
10 d
9 e

TL/F/10181–1

Order Number 54LS248DMQB, 54LS248FMQB, DM74LS248M or DM74LS248N
See NS Package Number J16A, M16A, N16E or W16A

Logic Symbol



7 1 2 6 3 5
A0 A1 A2 A3 LT RBI
BI/RBO
a b c d e f g
13 12 11 10 9 15 14 4

TL/F/10181–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI}/\overline{RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
a–g	Segment Outputs (Active HIGH)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS248			DM74LS248			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Voltage			−0.1			−0.1	mA
I_{OL}	Low Level Output Current			2			6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.4			V
			DM74	2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 3.2 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−0.3		−2.0	mA
			DM74	−0.3		−2.0	
I_{CC}	Supply Current	V_{CC} = Max				38	mA
I_{OFF}	Output High Current	Segment Inputs, V_O = 0.85V		−1.3			µA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		100	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		100	ns

National Semiconductor

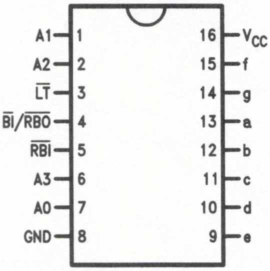
54LS249/DM74LS249
BCD to 7-Segment Decoder (with Open-Collector Outputs)

General Description

The 'LS249 has active HIGH open-collector outputs and incorporates the Lamp Test and $\overline{\text{BI}/\text{RBO}}$ inputs. Additionally, the 'LS249 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9.

Connection Diagram

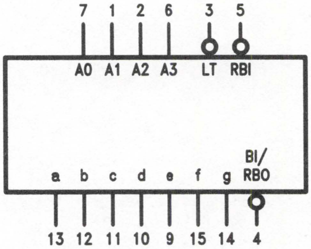
Dual-In-Line Package


A1 1
A2 2
$\overline{\text{LT}}$ 3
$\overline{\text{BI}}/\overline{\text{RBO}}$ 4
$\overline{\text{RBI}}$ 5
A3 6
A0 7
GND 8
16 V_{CC}
15 f
14 g
13 a
12 b
11 c
10 d
9 e

TL/F/10213-1

Order Number 54LS249DMBQ, 54LS249FMBQ or DM74LS249N
See NS Package Number J16A, N16E or W16A

Logic Symbol


7
1
2
6
3
5
A0
A1
A2
A3
LT
RBI
a
b
c
d
e
f
g
BI/ RBO
13
12
11
10
9
15
14
4

TL/F/10213-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A_0–A_3	BCD Inputs
$\overline{\text{BI}}$	Blanking Input (Active LOW)
$\overline{\text{LT}}$	Lamp Test Input (Active LOW)
$\overline{\text{BI}/\text{RBO}}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
a–g	Segment Outputs (Active HIGH)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS249			DM74LS249			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.25			−0.25	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.4			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Inputs	−0.03		−0.4	mA
			BI/$\overline{\text{RBO}}$	−0.09		−1.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−0.3		−2.0	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max, V_{IN} = 4.5V				15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

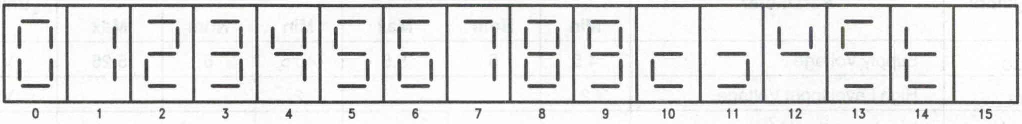
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = +5.0V, T_A = +25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 2\ k\Omega$		Units
		$C_L = 15\ pF$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Time A_n to a–g (54LS $R_L = 2\ k\Omega$)		100 100	ns
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{BI}$ to a–g (54LS $R_L = 6\ k\Omega$)		100 100	ns

Numerical Designations—Resultant Displays



TL/F/10213-3

Truth Table

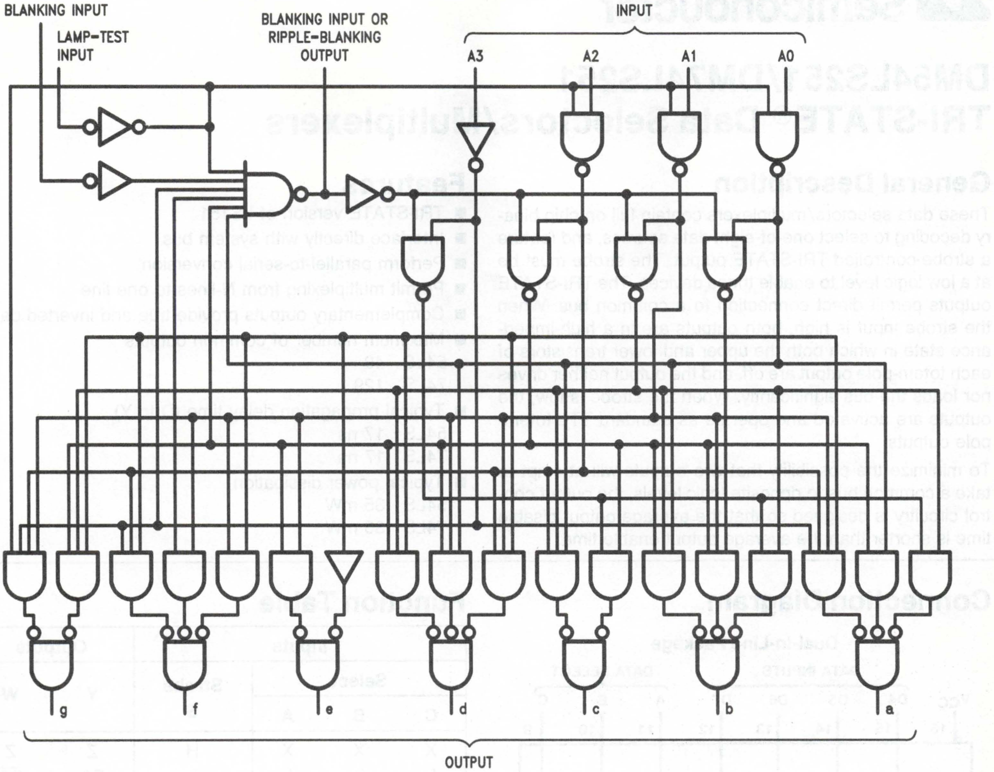
Decimal or Function	Inputs						Outputs							Note
	$\overline{LT}$	A_3	A_2	A_1	A_0	$\overline{BI/RBO}$	a	b	c	d	e	f	g	
0	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	H	L	L	L	L	L	L	L	
$\overline{BI}$	X	X	X	X	X	L	L	L	L	L	L	L	L	2
$\overline{LT}$	L	X	X	X	X	H	H	H	H	H	H	H	H	3

Note 1: $\overline{BI/RBO}$ is wired-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired. X = input may be HIGH or LOW.

Note 2: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.

Note 3: When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a HIGH level.

Logic Diagram


BLANKING INPUT
LAMP-TEST INPUT
BLANKING INPUT OR RIPPLE-BLANKING OUTPUT
INPUT
A3
A2
A1
A0
g
f
e
d
c
b
a
OUTPUT

TL/F/10213–4

National Semiconductor

DM54LS251/DM74LS251
TRI-STATE® Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

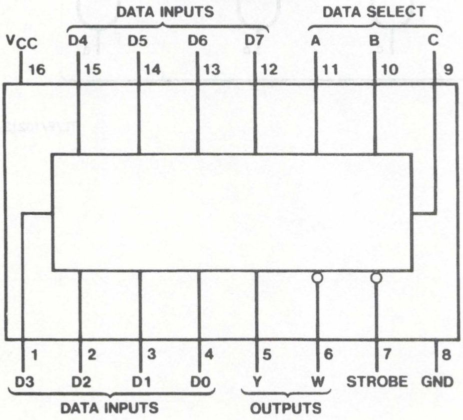
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

Features

- TRI-STATE version of LS151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data
- Maximum number of common outputs
  54LS 49
  74LS 129
- Typical propagation delay time (D to Y)
  54LS 17 ns
  74LS 17 ns
- Typical power dissipation
  54LS 35 mW
  74LS 35 mW

Connection Diagram

Dual-In-Line Package



TL/F/6415–1

Order Number DM54LS251J, DM54LS251W, DM74LS251M or DM74LS251N
See NS Package Number J16A, M16A, N16E or W16A

Function Table

Inputs				Outputs	
Select			Strobe S	Y	W
C	B	A			
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level,
X = Don't Care, Z = High Impedance (Off)
D0, D1 . . . D7 = The level of the respective D input

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS251			DM74LS251			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			6.1	10	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			7.1	12	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with the outputs open, STROBE grounded, and all other inputs at 4.5V.

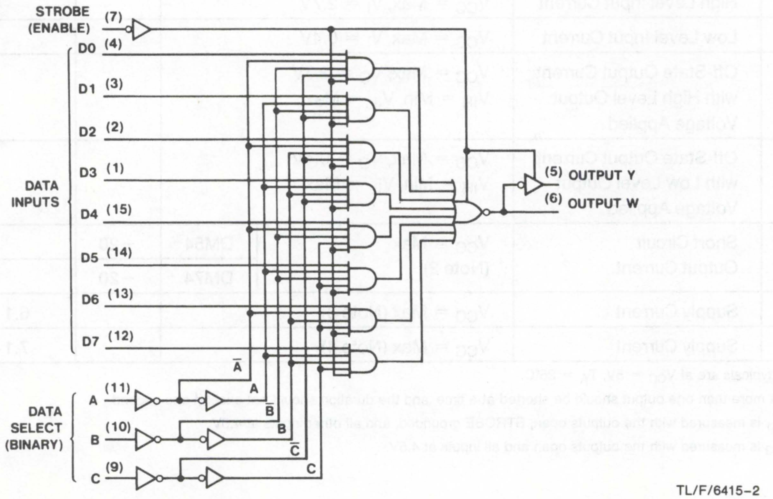
Note 4: I_{CC2} is measured with the outputs open and all inputs at 4.5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) to (Output)	R_L = 667Ω C_L = 45 pF Min	 Max	 C_L = 150 pF Min	 Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C (4 Levels) to Y		45		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C (4 Levels) to Y		45		53	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C (3 Levels) to W		33		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C (3 Levels) to W		33		42	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to Y		28		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to Y		28		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to W		15		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to W		15		25	ns
t_{PZH}	Output Enable Time to High Level Output	Strobe to Y		45		60	ns
t_{PZL}	Output Enable Time to Low Level Output	Strobe to Y		40		51	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)	Strobe to Y		45			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)	Strobe to Y		25			ns
t_{PZH}	Output Enable Time to High Level Output	Strobe to W		27		40	ns
t_{PZL}	Output Enable Time to Low Level Output	Strobe to W		40		47	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)	Strobe to W		55			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)	Strobe to W		25			ns

Note 1: C_L = 5 pF

Logic Diagram



TL/F/6415-2

National Semiconductor

54LS253/DM54LS253/DM74LS253 TRI-STATE® Data Selectors/Multiplexers

General Description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

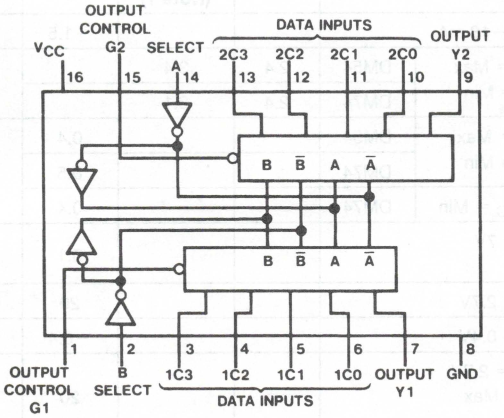
The TRI-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level.

Features

- TRI-STATE version of LS153 with same pinout
- Schottky-diode-clamped transistors
- Permit multiplexing from N-lines to one line
- Performs parallel-to-serial conversion
- Strobe/output control
- High fanout totem-pole outputs
- Typical propagation delay
  - Data to output 12 ns
  - Select to output 21 ns
- Typical power dissipation 35 mW
- Alternate Military/Aerospace device (54LS253) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6416-1

Order Number 54LS253DMQB, 54LS253FMQB, 54LS253LMQB, DM54LS253J, DM54LS253W, DM74LS253M or DM74LS253N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address Inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance (off).

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS253			DM74LS253			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74			0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4 V_{IH} = Min, V_{IL} = Max				−20	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			7	12	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			8.5	14	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, and all the inputs grounded.

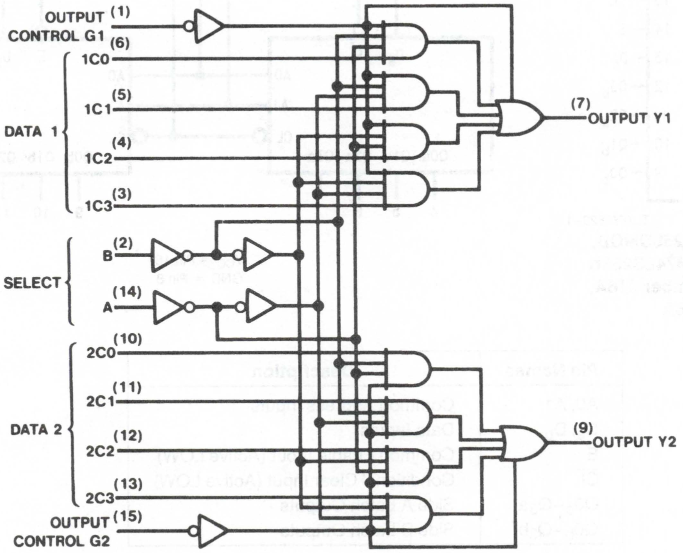
Note 4: I_{CC2} is measured with the outputs open, OUTPUT CONTROL at 4.5V and all other inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		20		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		45		54	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		32		44	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		18		32	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		23		35	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)	Output Control to Y		41			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)	Output Control to Y		27			ns

Note 1: C_L = 5 pF.

Logic Diagram


OUTPUT CONTROL G1 (1)
(6) 1C0
(5) 1C1
DATA 1
(4) 1C2
(3) 1C3
(7) OUTPUT Y1
SELECT
(2) B
(14) A
(10) 2C0
(11) 2C1
DATA 2
(12) 2C2
(13) 2C3
(9) OUTPUT Y2
OUTPUT CONTROL G2 (15)

TL/F/6416–2

National Semiconductor

54LS256/DM74LS256 Dual 4-Bit Addressable Latch

General Description

The 'LS256 is a dual 4-bit addressable latch with common control inputs; these include two Address inputs (A0, A1), an active LOW enable input ($\overline{E}$) and an active LOW Clear input ($\overline{CL}$). Each latch has a Data input (D) and four outputs (Q0–Q3).

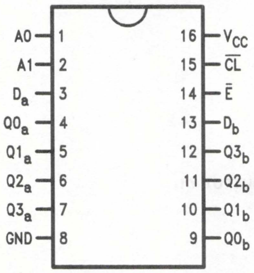
When the Enable ($\overline{E}$) is HIGH and the Clear input ($\overline{CL}$) is LOW, all outputs (Q0–Q3) are LOW. Dual 4-channel demultiplexing occurs when the $\overline{CL}$ and $\overline{E}$ are both LOW. When $\overline{CL}$ is HIGH and $\overline{E}$ is LOW, the selected output (Q0–Q3), determined by the Address inputs, follows D. When the $\overline{E}$ goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$ = LOW, $\overline{CL}$ = HIGH), changing more than one bit of the Address (A0, A1) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ($\overline{E}$ = $\overline{CL}$ = HIGH).

Features

- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Active low common clear

Connection Diagram

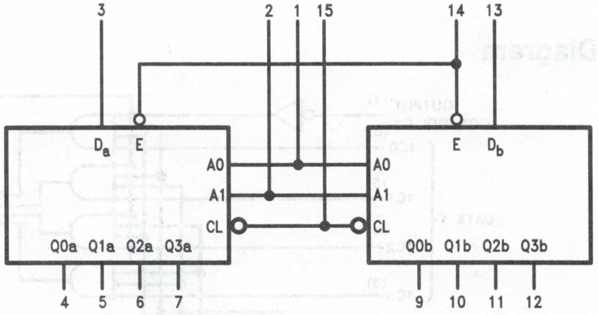
Dual-In-Line Package



TL/F/9823-1

Order Number 54LS256DMQB, 54LS256FMQB or DM74LS256N
See NS Package Number J16A, N16E or W16A

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

TL/F/9823-2

Pin Names	Description
A0, A1	Common Address Inputs
D_a, D_b	Data Inputs
$\overline{E}$	Common Enable Input (Active LOW)
$\overline{CL}$	Conditional Clear Input (Active LOW)
$Q0_a$–$Q3a$	Side A Latch Outputs
$Q0_b$–$Q3b$	Side B Latch Outputs

Truth Table

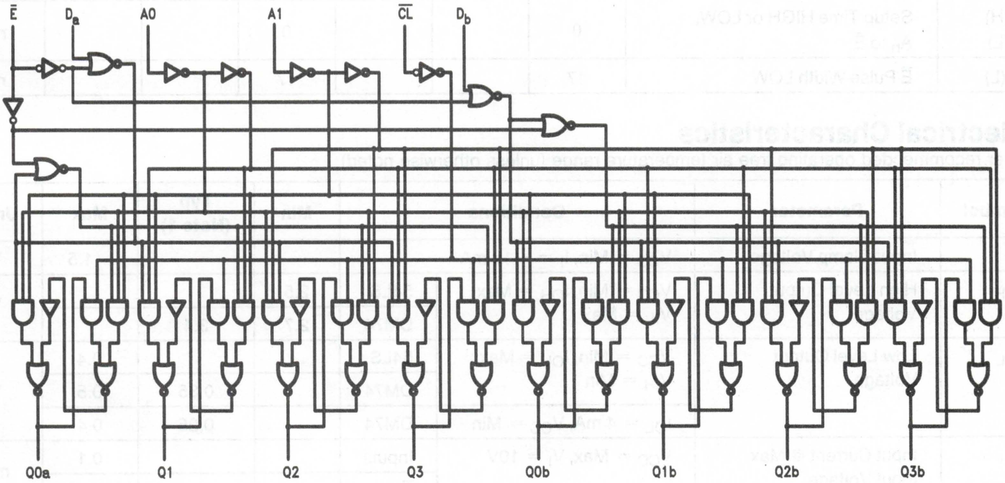
Inputs				Outputs				Mode
$\overline{CL}$	$\overline{E}$	A0	A1	Q0	Q1	Q2	Q3	
L	H	X	X	L	L	L	L	Clear
L	L	L	L	D	L	L	L	Demultiplex
L	L	H	L	L	D	L	L	
L	L	L	H	L	L	D	L	
L	L	H	H	L	L	L	D	
H	H	X	X	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Memory
H	L	L	L	D	Q_{t-1}	Q_{t-1}	Q_{t-1}	Addressable Latch
H	L	H	L	Q_{t-1}	D	Q_{t-1}	Q_{t-1}	
H	L	L	H	Q_{t-1}	Q_{t-1}	D	Q_{t-1}	
H	L	H	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	D	

t−1 = Bit time before address change or rising edge of $\overline{E}$
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Mode Selection

$\overline{E}$	$\overline{CL}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 4-Channel Demultiplexers
H	L	Clear

Logic Diagram



TL/F/9823-3

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS256			DM74LS256			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H)	Setup Time HIGH, D_n to $\overline{E}$	20			20			ns
t_h (H)	Hold Time HIGH, D_n to $\overline{E}$	0			0			ns
t_s (L)	Setup Time LOW, D_n to $\overline{E}$	15			15			ns
t_h (L)	Hold Time LOW, D_n to $\overline{E}$	0			0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW, A_n to $\overline{E}$	0			0			ns
t_w (L)	$\overline{E}$ Pulse Width LOW	17			17			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V	Inputs			0.1	mA
			$\overline{E}$			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Inputs			20	μA
			$\overline{E}$			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Inputs			−0.4	mA
			$\overline{E}$			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				25	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$R_L = 2\ k\Omega$ $C_L = 15\ pF$ Max	Units
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n	27 24	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n	30 20	ns
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n	30 29	ns
t_{PLH}	Propagation Delay CL to Q_n	18	ns

National Semiconductor

54LS257A/DM54LS257B/DM74LS257B, 54LS258A/DM54LS258B/DM74LS258B TRI-STATE® Quad 2-Data Selectors/Multiplexers

General Description

These Schottky-clamped high-performance multiplexers feature TRI-STATE outputs that can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times.

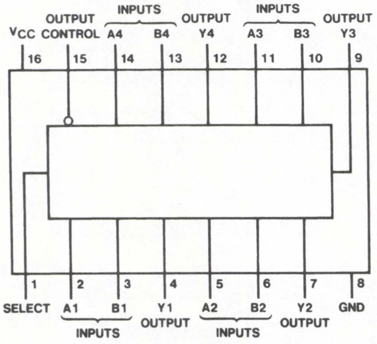
This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Features

- TRI-STATE versions LS157 and LS158 with same pinouts
- Schottky-clamped for significant improvement in A-C performance
- Provides bus interface from multiple sources in high-performance systems
- Average propagation delay from data input 12 ns
- Typical power dissipation
  - LS257B 50 mW
  - LS258B 35 mW
- Alternate military/aerospace devices (54LS257A/54LS258A) are available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

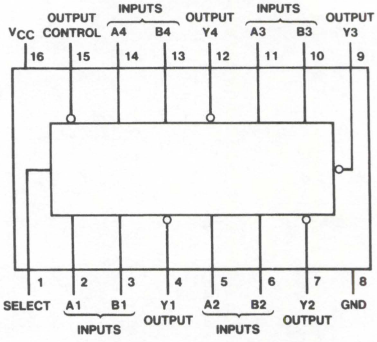
Dual-In-Line Package


VCC
OUTPUT CONTROL
INPUTS
A4
B4
OUTPUT
Y4
INPUTS
A3
B3
OUTPUT
Y3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
SELECT
A1
B1
INPUTS
Y1
OUTPUT
A2
B2
INPUTS
Y2
OUTPUT
GND

TL/F/6417-1

Order Number 54LS257ADMQB, 54LS257AFMQB, 54LS257ALMQB, DM54LS257BJ, DM54LS257BW, DM74LS257BM or DM74LS257BN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Dual-In-Line Package


VCC
OUTPUT CONTROL
INPUTS
A4
B4
OUTPUT
Y4
INPUTS
A3
B3
OUTPUT
Y3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
SELECT
A1
B1
INPUTS
Y1
OUTPUT
A2
B2
INPUTS
Y2
OUTPUT
GND

TL/F/6417-2

Order Number 54LS258ADMQB, 54LS258AFMQB, 54LS258ALMQB, DM54LS258BJ, DM54LS258BW, DM74LS258BM or DM74LS258BN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Inputs				Output Y	
Output Control	**Select**	**A**	**B**	**LS257**	**LS258**
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care,
Z = High Impedance (off)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS257B			DM74LS257B			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS257B Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Select			0.2	mA
			Other			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Select			40	µA
			Other			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Select			−0.8	mA
			Other			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			5.9	10	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 3)			9.2	16	mA
I_{CCZ}	Supply Current with Outputs Disabled	V_{CC} = Max (Note 3)			12	19	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

'LS257B Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω C_L = 45 pF Min	 C_L = 45 pF Max	 C_L = 150 pF Min	 C_L = 150 pF Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		18		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		28		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		35		42	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		15		27	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		28		38	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)	Output Control to Y		26			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)	Output Control to Y		25			ns

Note 1: C_L = 5 pF.

Recommended Operating Conditions

Symbol	Parameter	DM54LS258B Min	 Nom	 Max	DM74LS258B Min	 Nom	 Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS258B Electrical Characteristics

over recommended operating free air temperature range (unless noted otherwise)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Select			0.2	mA
			Other			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Select			40	μA
			Other			20	

’LS258B Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Select			−0.8	mA
			Other			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			4.1	7	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 3)			9	14	mA
I_{CCZ}	Supply Current with Outputs Disabled	V_{CC} = Max (Note 3)			12	19	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

’LS258B Switching Characteristics

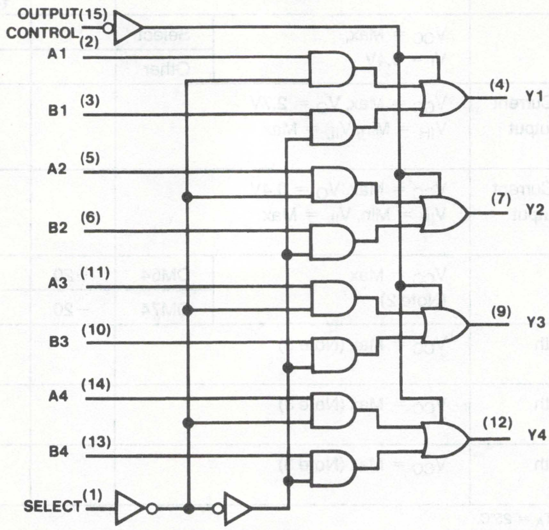
at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		18		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		28		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		35		42	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		15		27	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		28		38	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 4)	Output Control to Y		26			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 4)	Output Control to Y		25			ns

Note 4: C_L = 5 pF.

Logic Diagrams

LS257B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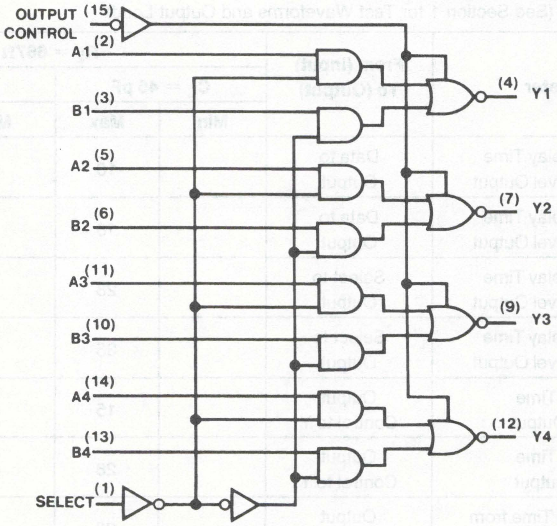
A1
(2)
B1
(3)
A2
(5)
B2
(6)
A3
(11)
B3
(10)
A4
(14)
B4
(13)
SELECT
(1)
(4)
Y1
(7)
Y2
(9)
Y3
(12)
Y4

TL/F/6417–3

LS258B


OUTPUT CONTROL
(15)
A1
(2)
B1
(3)
A2
(5)
B2
(6)
A3
(11)
B3
(10)
A4
(14)
B4
(13)
SELECT
(1)
(4)
Y1
(7)
Y2
(9)
Y3
(12)
Y4

TL/F/6417–4

National Semiconductor

54LS259/DM74LS259 8-Bit Addressable Latches

General Description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

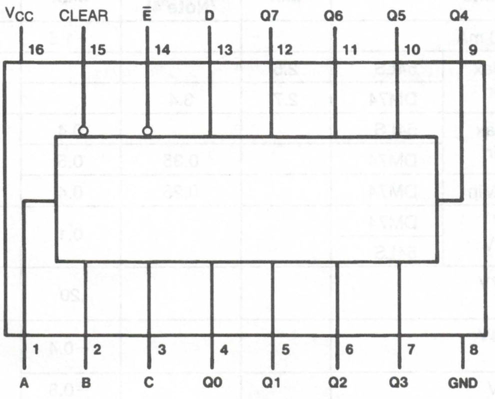
Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

Features

- 8-Bit parallel-out storage register performs serial-to-parallel conversion with storage
- Asynchronous parallel clear
- Active high decoder
- Enable/disable input simplifies expansion
- Direct replacement for Fairchild 9334
- Expandable for N-bit applications
- Four distinct functional modes
- Typical propagation delay times:
  - Enable-to-output 18 ns
  - Data-to-output 16 ns
  - Address-to-output 21 ns
  - Clear-to-output 17 ns
- Fan-out
  - I_{OL} (sink current)
    - 54LS259 4 mA
    - 74LS259 8 mA
  - I_{OH} (source current) −0.4 mA
- Typical I_{CC} 22 mA

Connection Diagram

Dual-In-Line Package



TL/F/6418-1

Order Number 54LS259DMQB, 54LS259FMQB, 54LS259LMQB, DM74LS259WM or DM74LS259N
See NS Package Number E20A, J16A, M16B, N16E or W16A

Function Table

Inputs		Output of Addressed Latch	Each Other Output	Function
Clear	$\overline{E}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

Latch Selection Table

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = High Level, L = Low Level

D = the Level of the Data Input

Q_{i0} = the Level of Q_i (i = 0, 1, . . . 7, as Appropriate) before the Indicated Steady-State Input Conditions Were Established.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		54LS259			DM74LS259			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
t_W	Pulse Width (Note 7)	Enable	17			15			ns
		Clear	17			15			
t_{SU}	Setup Time (Notes 1, 2, 3 & 7)	Data	20 ↑			15 ↑			ns
		Select	15 ↓			15 ↓			
t_H	Hold Time (Notes 1, 2 & 7)	Data	5 ↑			0 ↑			ns
		Select	0 ↑			0 ↑			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_I = 10V	54LS				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
	Enable	V_{CC} = 5.0, V_I = 0.4V				−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			22	36	mA

Note 1: The symbols (↓, ↑) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

Note 2: Setup and hold times are with reference to the enable input.

Note 3: The select-to-enable setup time is the time before the High-to-Low enable transition that the select must be stable so that the correct latch is selected and the others not affected.

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all inputs at 4.5V, and all outputs open.

Note 7: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	54LS		DM74LS		Units
			C_L = 15 pF		C_L = 50 pF R_L = 2 kΩ		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output		27		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output		24		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		30		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		20		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		30		41	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		29		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		18		36	ns

National Semiconductor

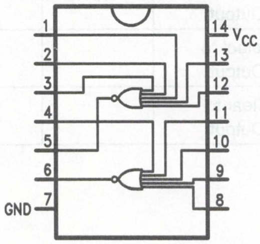
54LS260/DM74LS260 Dual 5-Input NOR Gate

General Description

This device contains two individual five input gates, each of which perform the logic NOR function.

Connection Diagram

Dual-In-Line Package



TL/F/9824-1

Order Number 54LS260DMQB, 54LS260FMQB,
54LS260LMQB, DM74LS260M or DM74LS260N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS260			DM74LS260			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	54LS			−0.40	mA
			DM74			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max, V_{IN} = GND				4.0	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max, V_{IN} = Open				5.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5V, T_A = +25°C (See Section 1 for Test Waveforms and Ouput Load)

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		12	ns

National Semiconductor

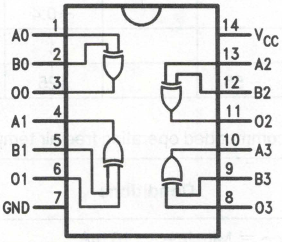
54LS266/DM74LS266 Quad 2-Input Exclusive-NOR Gate with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic exclusive-OR function. Outputs are open collector.

Connection Diagram

Dual-In-Line Package


A0
B0
O0
A1
B1
O1
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8
VCC
A2
B2
O2
A3
B3
O3

TL/F/10182–1

Order Number 54LS266DMQB, 54LS266FMQB, DM74LS266M or DM74LS266N
See NS Package Number J14A, M14A, N14A or W14B

Truth Table

Inputs		Outputs
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS266			DM74LS266			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.1			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				13	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 2\ k\Omega$ $C_L = 15\ pF$		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		23	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

54LS273/DM74LS273
8-Bit Register with Clear

General Description

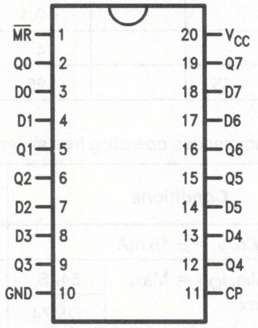
The 'LS273 is a high speed 8-bit register, consisting of eight D-type flip-flops with a common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch row spacing.

Features

- Edge-triggered
- 8-bit high speed register
- Parallel in and out
- Common clock and master reset

Connection Diagram

Dual-In-Line Package


$\overline{MR}$ 1
Q0 2
D0 3
D1 4
Q1 5
Q2 6
D2 7
D3 8
Q3 9
GND 10
20 V_{CC}
19 Q7
18 D7
17 D6
16 Q6
15 Q5
14 D5
13 D4
12 Q4
11 CP

TL/F/9825-1

Order Number 54LS273DMQB, 54LS273FMQB, 54LS273LMQB, DM74LS273M or DM74LS273N
See NS Package Number E20A, J20A, M20B, N20A or W20A

Pin Names	Description
CP	Clock Pulse Input (Active Rising Edge)
D0–D7	Data Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
Q0–Q7	Flip-Flop Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS273			DM74LS273			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW D_n to CP	15 15			15 15			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW D_n to CP	5 5			5 5			ns
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	20 20			20 20			ns
$t_w(L)$	$\overline{MR}$ Pulse Width LOW	20			20			ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	15			15			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15$ pF				Units
		54LS		DM74LS $R_L = 2$ kΩ		
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	30		30		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		32 32		24 24	ns
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n		32		27	ns

Functional Description

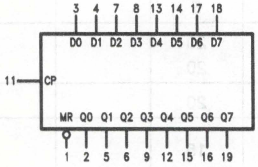
The 'LS273 is an 8-bit parallel register with a common Clock and common Master Reset. When the $\overline{MR}$ input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

Truth Table

Inputs			Outputs
MR	CP	D_n	Q_n
L	X	X	L
H	↗	H	H
H	↗	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

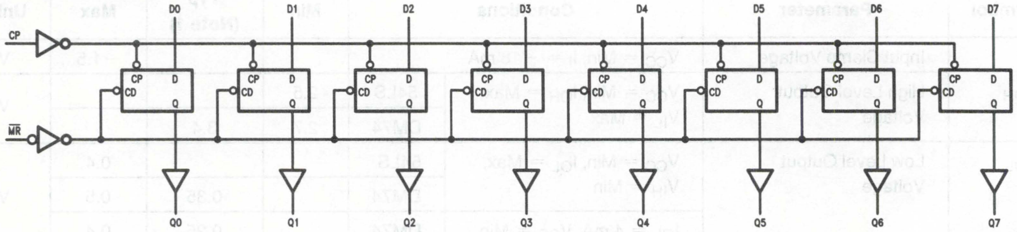
Logic Symbol


3 4 7 8 13 14 17 18
D0 D1 D2 D3 D4 D5 D6 D7
11
CP
MR Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
1 2 5 6 9 12 15 16 19

TL/F/9825-2

V_{CC} = Pin 20
GND = Pin 10

Logic Diagram


D0
D1
D2
D3
D4
D5
D6
D7
CP
$\overline{MR}$
CP
D
CD
Q
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7

TL/F/9825-3

National Semiconductor

54LS279/DM54LS279/DM74LS279 Quad $\overline{S}$-$\overline{R}$ Latches

General Description

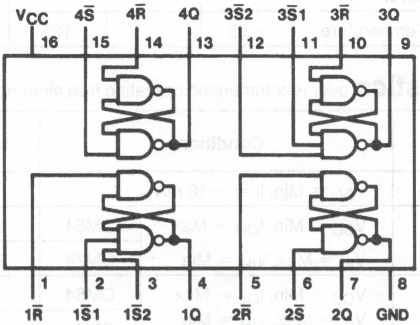
The 'LS279 consists of four individual and independent Set-Reset Latches with active low inputs. Two of the four latches have an additonal $\overline{S}$ input ANDed with the primary $\overline{S}$ input. A low on any $\overline{S}$ input while the $\overline{R}$ input is high will be stored in the latch and appear on the corresponding Q output as a high. A low on the $\overline{R}$ input while the $\overline{S}$ input is high will clear the Q output to a low. Simultaneous transistion of the $\overline{R}$ and $\overline{S}$ inputs from low to high will cause the Q output to be indeterminate. Both inputs are voltage level triggered and are not affected by transition time of the input data.

Features

- Alternate military/aerospace device (54LS279) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



V$_{CC}$
4$\overline{S}$
4$\overline{R}$
4Q
3$\overline{S}$2
3$\overline{S}$1
3$\overline{R}$
3Q
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
1$\overline{R}$
1$\overline{S}$1
1$\overline{S}$2
1Q
2$\overline{R}$
2$\overline{S}$
2Q
GND

TL/F/6420-1

Order Number 54LS279DMQB, 54LS279FMQB, 54LS279LMQB, DM54LS279J, DM74LS279M or DM74LS279N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Inputs		Output
$\overline{S}$(1)	$\overline{R}$	Q
L	L	H*
L	H	H
H	L	L
H	H	Q_0

H = High Level

L = Low Level

Q_0 = The Level of Q before the indicated input conditions were established.

*This output level is pseudo stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.

Note 1: For latches with double $\overline{S}$ inputs:

H = both $\overline{S}$ inputs high

L = one or both $\overline{S}$ inputs low

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS279			DM74LS279			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.5		V
			DM74	2.7	3.5		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			3.8	7	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all $\overline{R}$ inputs grounded, all $\overline{S}$ inputs at 4.5V and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	$\overline{S}$ to Q		22		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{S}$ to Q		15		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{R}$ to Q		27		33	ns

National Semiconductor

54LS283/DM54LS283/DM74LS283
4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

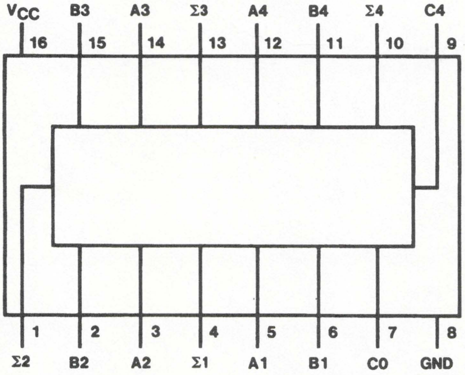
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  - Two 8-bit words 25 ns
  - Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW
- Alternate Military/Aerospace device (54LS283) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6421-1

Order Number 54LS283DMQB, 54LS283FMQB, 54LS283LMQB, DM54LS283J, DM54LS283W, DM74LS283M or DM74LS283N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS283			DM74LS283			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	A, B			0.2	mA
			C0			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	A, B			40	μA
			C0			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	A, B			−0.8	mA
			C0			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			19	34	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			22	39	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, all B inputs low and all other inputs at 4.5V, or all inputs at 4.5V.

Note 4: I_{CC2} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ1, Σ2		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ1, Σ2		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ3		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ3		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ4		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ4		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i or B_i to Σ_i		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i or B_i to Σ_i		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to C4		17		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i or B_i to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i or B_i to C4		17		26	ns

Function Table

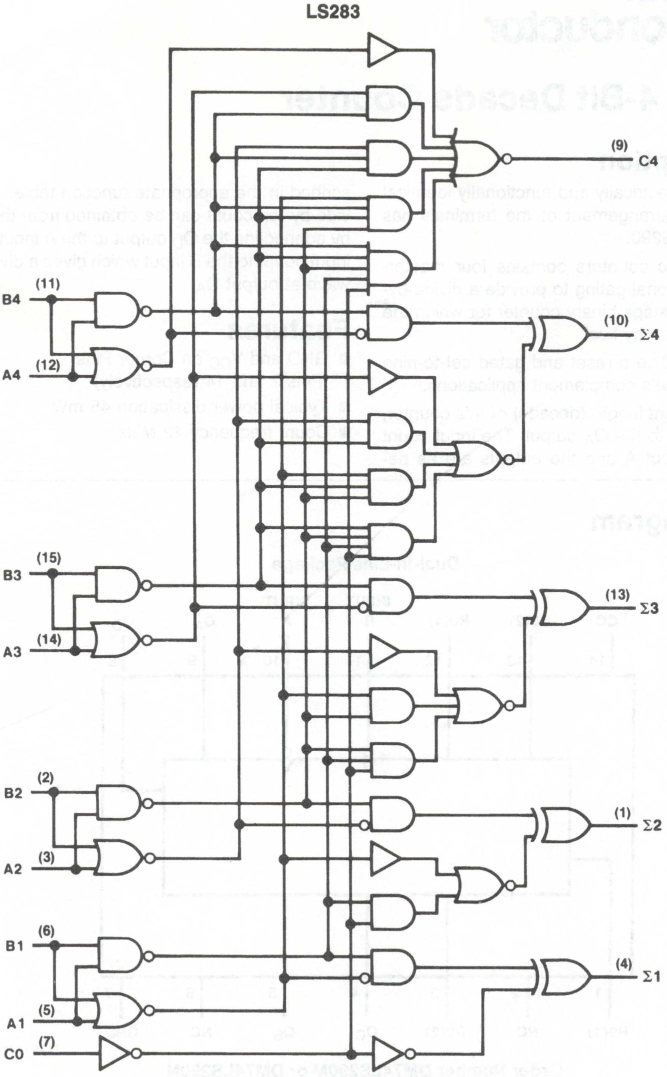
Input				Outputs					
				When C0 = L			When C0 = H		
				When C2 = L			When C2 = H		
A1 A3	B1 B3	A2 A4	B2 B4	Σ1 Σ3	Σ2 Σ4	C2 C4	Σ1 Σ3	Σ2 Σ4	C2 C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

TL/F/6421-3

H = High Level, L = Low Level

Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Logic Diagram


LS283
B4
(11)
A4
(12)
B3
(15)
A3
(14)
B2
(2)
A2
(3)
B1
(6)
A1
(5)
C0
(7)
(9)
C4
(10)
Σ4
(13)
Σ3
(1)
Σ2
(4)
Σ1

TL/F/6421–2

National Semiconductor

DM74LS290 4-Bit Decade Counter

General Description

The 'LS290 counter is electrically and functionally identical to the 'LS90. Only the arrangement of the terminals has been changed for the 'LS290.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

This counter has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

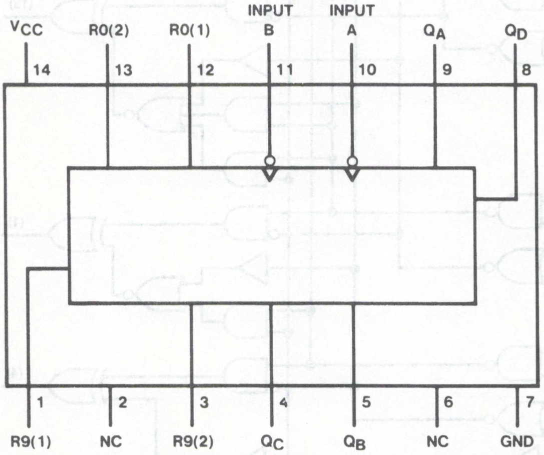
To use the maximum count length (decade) of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the 'LS290 counter by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

- GND and V_{CC} on Corner Pins (Pins 7 and 14 respectively)
- Typical power dissipation 45 mW
- Count frequency 42 MHz

Connection Diagram

Dual-In-Line Package



TL/F/6422–1

Order Number DM74LS290M or DM74LS290N
See NS Package Number M14A or N14A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74LS290			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Freq. (Note 1)	A to Q_A	0		32	MHz
		B to Q_B	0		16	
f_{CLK}	Clock Freq. (Note 2)	A to Q_A	0		20	MHz
		B to Q_B	0		10	
t_W	Pulse Width (Note 6)	A	15			ns
		B	30			
		Reset	15			
t_{REL}	Reset Release Time (Note 6)		25			ns
T_A	Free Air Operating Temperature		0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
			A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	μA
			A			40	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			9	15	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		48		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		50		68	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		53	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		32		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		35		53	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		30		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		40		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		53	ns

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A =25°C and V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 6: T_A = 25°C and V_{CC} 5V.

Function Tables

BCD Count Sequence
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Note A: Output Q_A is connected to input B for BCD count

H = High Logic Level

L = Low Logic Level

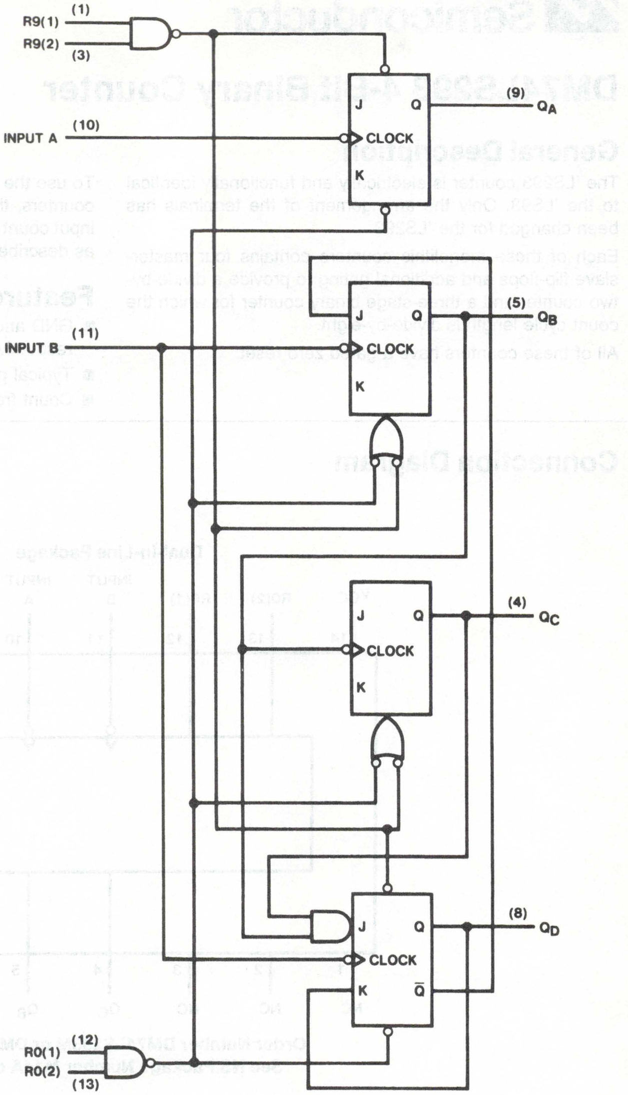
X = Either Low or High Logic Level

Bi-Quinary (5-2)
(See Note B)

Count	Output			
	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Note B: Output Q_D is connected to input A for bi-quinary count.

Logic Diagram



(1)
R9(1)
R9(2)
(3)
J
Q
(9)
QA
INPUT A
(10)
CLOCK
K
J
Q
(5)
QB
INPUT B
(11)
CLOCK
K
J
Q
(4)
QC
CLOCK
K
J
Q
(8)
QD
CLOCK
K
Q̄
(12)
R0(1)
R0(2)
(13)

TL/F/6422-2

Reset/Count Truth Table

Reset Inputs				Outputs			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

National Semiconductor

DM74LS293 4-Bit Binary Counter

General Description

The 'LS293 counter is electrically and functionally identical to the 'LS93. Only the arrangement of the terminals has been changed for the 'LS293.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

All of these counters have a gated zero reset.

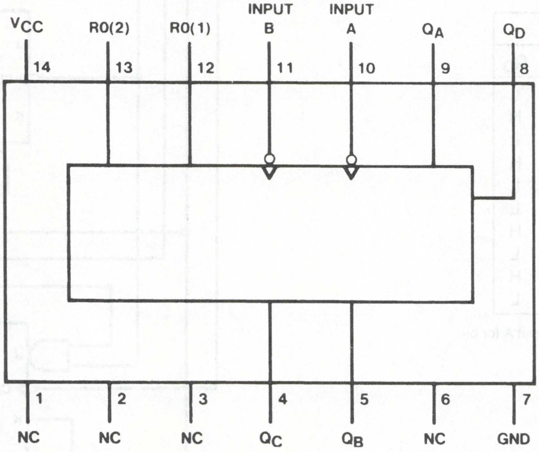
To use the maximum count length (four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.

Features

- GND and V_{CC} on Corner Pins (Pins 7 and 14 respectively)
- Typical power dissipation 45 mW
- Count frequency 42 MHz

Connection Diagram

Dual-In-Line Package



TL/F/6423–1

Order Number DM74LS293M or DM74LS293N
See NS Package Number M14A or N14A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74LS293			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 1)	A to Q_A	0		32	MHz
		B to Q_B	0		16	
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		20	MHz
		B to Q_B	0		10	
t_W	Pulse Width (Note 6)	A	15			ns
		B	30			
		Reset	15			
t_{REL}	Reset Release Time (Note 6)		25			ns
T_A	Free Air Operating Temperature		0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	Reset			0.1	mA
			A			0.2	
			B			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Reset			20	µA
			A			40	
			B			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			9	15	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		70		87	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		70		93	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		53	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		51		71	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		51		71	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		53	ns

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 6: T_A = 25°C and V_{CC} = 5V.

Function Tables

Count Sequence (See Note C)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

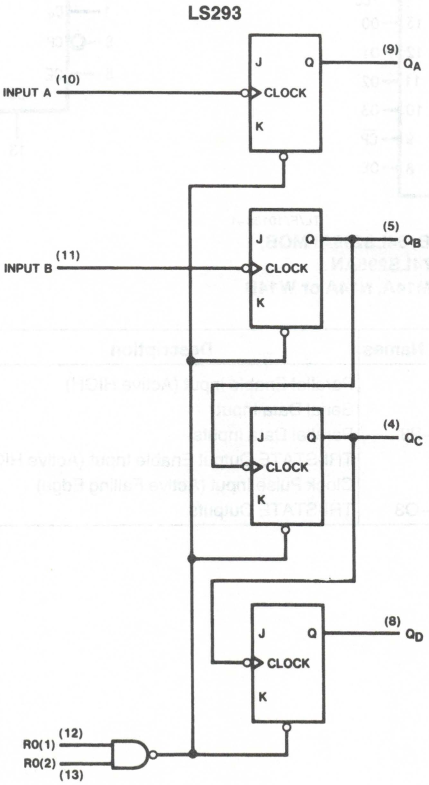
Note C: Output Q_A is connected to input B.

Reset/Count Truth Table

Reset Inputs		Outputs			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

H = High Level, L = Low Level, X = Don't Care.

Logic Diagram



LS293
INPUT A
(10)
INPUT B
(11)
J
Q
CLOCK
K
(9)
Q_A
(5)
Q_B
(4)
Q_C
(8)
Q_D
R0(1)
(12)
R0(2)
(13)

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Note: The J and K inputs shown without connection are for reference only and are functionally at a high level.

National Semiconductor

54LS295A/DM74LS295A 4-Bit Shift Register with TRI-STATE® Outputs

General Description

The 'LS295A is a 4-bit shift register with serial and parallel synchronous operating modes, and independent TRI-STATE output buffers. The Parallel Enable input (PE) controls the shift-right or parallel load operation. All data transfers and shifting occur synchronous with the HIGH-to-LOW clock transition.

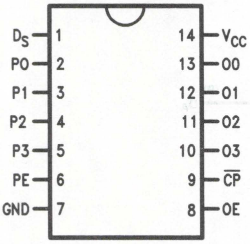
The TRI-STATE output buffers are controlled by an active HIGH Output Enable input (OE). Disabling the output buffers does not affect the shifting or loading of input data, but it does inhibit serial expansion. The device is fabricated with the Schottky barrier diode process for high speed.

Features

- Fully synchronous serial or parallel data transfers
- Negative edge-triggered clock input
- Parallel enable mode control input
- TRI-STATE bussable output buffers

Connection Diagram

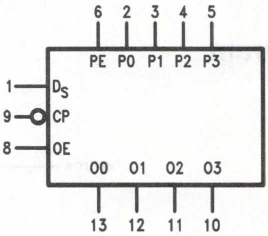
Dual-In-Line Package



TL/F/10183-1

Order Number 54LS295ADMQB, 54LS295AFMQB, DM74LS295AM or DM74LS295AN
See NS Package Number J14A, M14A, N14A or W14B

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

TL/F/10183-2

Pin Names	Description
PE	Parallel Enable Input (Active HIGH)
D_S	Serial Data Input
P0–P3	Parallel Data Inputs
OE	TRI-STATE Output Enable Input (Active HIGH)
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)
O0–O3	TRI-STATE Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS295A			DM74LS295A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Current			−1.0			−2.6	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_S, P_n to $\overline{CP}$	20 20			20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_S, P_n to $\overline{CP}$	10 10			10 10			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW PE to $\overline{CP}$	20 20			20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW PE to $\overline{CP}$	0 0			0 0			ns
t_w (L)	$\overline{CP}$ Pulse Width LOW	20			20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.4			V
			DM74	2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current Outputs ON	V_{CC} = Max, P_n = GND PE, DS, OE = 4.5V, $\overline{CP}$ = ‾_				23	mA
	Outputs OFF	V_{CC} = Max, PE, DS = 4.5V P_n, OE, $\overline{CP}$ = GND				25	mA

Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max			20	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−20	µA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 3 for waveforms and load configurations)

Symbol	Parameter	54/74LS		Units
		R_L = 2 kΩ, C_L = 15 pF		
		Min	Max	
f_{max}	Maximum Shift Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n		30 26	ns
t_{PZH} t_{PZL}	Output Enable Time		18 20	ns
t_{PHZ} t_{PLZ}	Output Disable Time		24 20	ns

Functional Description

This device is a 4-bit shift register with serial and parallel synchronous operating modes. It has a Serial Data (D_S) and four Parallel Data (P0–P3) inputs and four parallel TRI-STATE output buffers (O0–O3). When the Parallel Enable (PE) input is HIGH, data is transferred from the Parallel Data inputs (P0–P3) into the register synchronous with the HIGH-to-LOW transition of the Clock ($\overline{CP}$). When the PE is LOW, a HIGH-to-LOW transition on the clock transfers the serial data on the D_S input to the register Q0, and shifts data from Q0 to Q1, Q1 to Q2 and Q2 to Q3. The input data and parallel enable are fully edge-triggered and must be stable only one setup time before the HIGH-to-LOW clock transition.

The TRI-STATE output buffers are controlled by an active HIGH Output Enable input (OE). When the OE is HIGH, the four register outputs appear at the O0–O3 outputs. When OE is LOW, the outputs are forced to a high impedance OFF state. The TRI-STATE output buffers are completely independent of the register operation, i.e., the input transitions on the OE input do not affect the serial or parallel data transfers of the register. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Mode Select Table

Operating Mode	Inputs				Outputs			
	PE	$\overline{CP}$	D_S	P_n	Q0	Q1	Q2	Q3
Shift Right	l	↘	l	X	L	q_0	q_1	q_2
	l	↘	h	X	H	q_0	q_1	q_2
Parallel Load	h	↘	X	p_n	p0	p1	p2	p3

*The indicated data appears at the Q outputs when OE is HIGH. When OE is LOW, the indicated data is loaded into the register, but the outputs are all forced to the high impedance OFF state.

p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

l = LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.

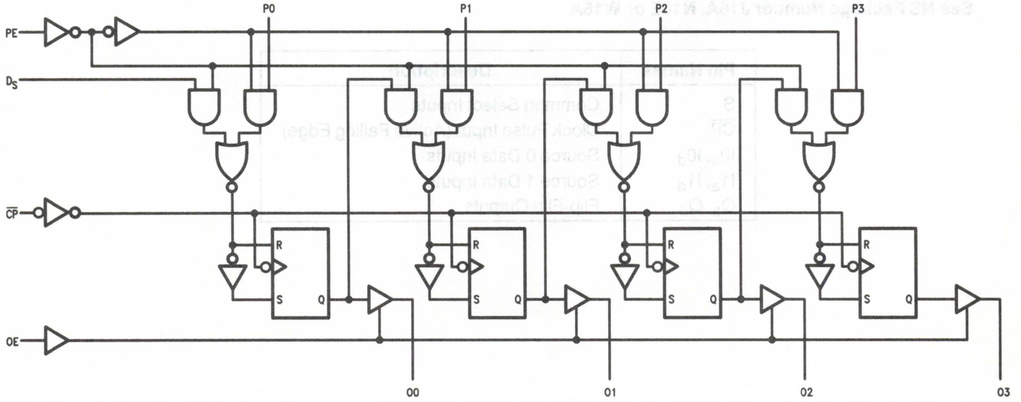
h = HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



TL/F/10183-3

National Semiconductor

54LS298/DM74LS298 Quad 2-Port Register Multiplexer with Storage

General Description

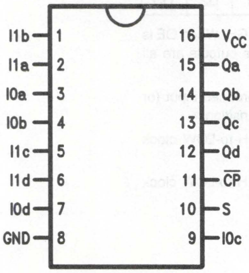
The 'LS298 is a quad 2-port register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronous with the HIGH-to-LOW transition of the Clock input.

Features

- Select from two data sources
- Fully edge-triggered operation
- Typical power dissipation of 65 mW

Connection Diagram

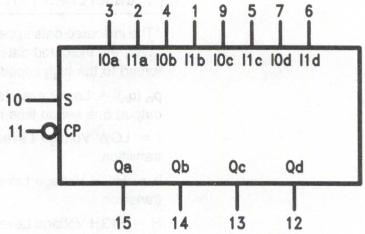
Dual-In-Line Package


I1b 1
I1a 2
I0a 3
I0b 4
I1c 5
I1d 6
I0d 7
GND 8
16 VCC
15 Qa
14 Qb
13 Qc
12 Qd
11 CP
10 S
9 I0c

TL/F/9826-1

Order Number 54LS298DMQB, 54LS298FMQB, DM74LS298M or DM74LS298N
See NS Package Number J16A, N16E or W16A

Logic Symbol


3 2 4 1 9 5 7 6
I0a I1a I0b I1b I0c I1c I0d I1d
10 S
11 CP
Qa Qb Qc Qd
15 14 13 12

TL/F/9826-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
S	Common Select Inputs
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)
$I0_a$, $I0_d$	Source 0 Data Inputs
$I1_a$, $I1_d$	Source 1 Data Inputs
Q_a, Q_d	Flip-Flip Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS298			DM74LS298			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW S to $\overline{CP}$	25 25			25 25			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW S to $\overline{CP}$	0 0			0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW $I0_x$ or $I1_x$ to $\overline{CP}$	15 15			15 15			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $I0_x$ or $I1_x$ to $\overline{CP}$	5.0 5.0			5.0 5.0			ns
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width HIGH or LOW	20 20			20 20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max, $I0_n$, $I1_n$, S = GND, $\overline{CP}$ = ‾_				21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = +5V and T_A = +25°C (See Section 1 for test waveforms and output load)

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output $\overline{CP}$ to Q_n		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output $\overline{CP}$ to Q_n		25	ns

Functional Description

This device is a high speed quad 2-port register. It selects four bits of data from two sources (ports) under the control of a Common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). The 4-bit output register is fully edge-triggered. The Data inputs (I_{nx}) and Select input (S) need be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

Truth Table

Inputs			Output
S	$I0_x$	$I1_x$	Q_x
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

l = LOW Voltage Level one setup time prior to the HIGH-to-LOW clock transition.

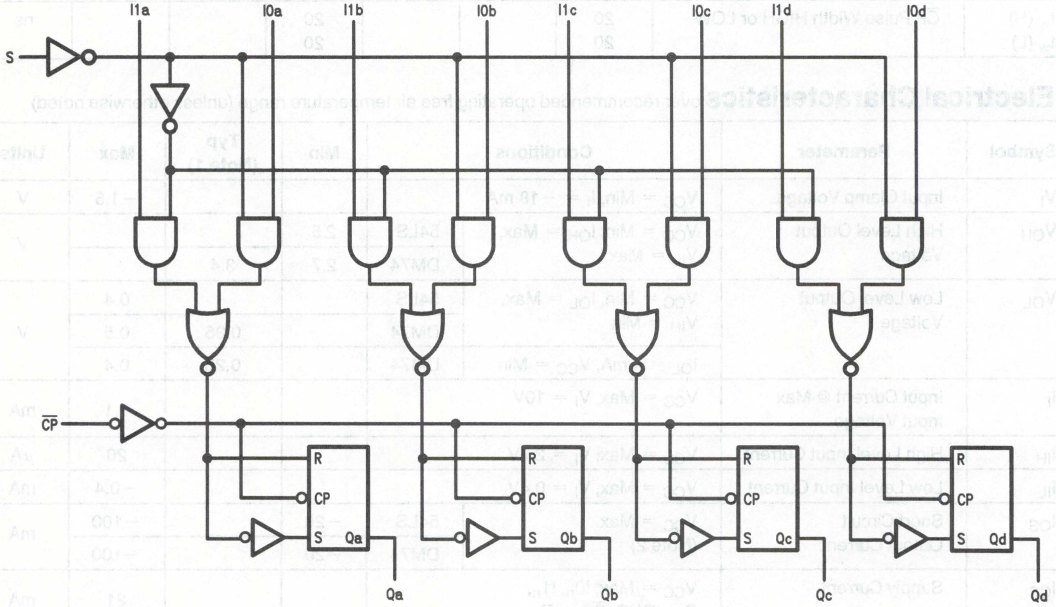
h = HIGH Voltage Level one setup time prior to the HIGH-to-LOW clock transition.

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



TL/F/9826-3

National Semiconductor

54LS299/DM74LS299 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

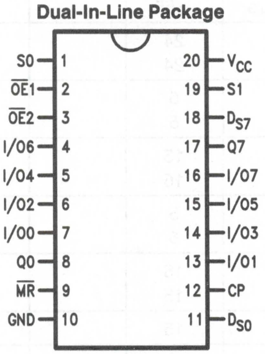
General Description

The 'LS299 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q0 and Q7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

Features

- Common I/O for reduced pin count
- Four operation modes: shift left, shift right, load and store
- Separate shift right serial input and shift left serial input for easy cascading
- TRI-STATE outputs for bus oriented applications

Connection Diagram



TL/F/9827-1

Order Number 54LS299DMQB, 54LS299FMQB,
54LS299LMQB, DM74LS299WM or DM74LS299N
See NS Package Number E20A, J20A, M20B, N20A or W20A

Pin Names	Description
CP	Clock Pulse Input (Active Rising Edge)
D_{S0}	Serial Data Input for Right Shift
D_{S7}	Serial Data Input for Left Shift
S0, S1	Mode Select Inputs
$\overline{\text{MR}}$	Asynchronous Master Reset Input (Active LOW)
$\overline{\text{OE}}$1, $\overline{\text{OE}}$2	TRI-STATE Output Enable Inputs (Active LOW)
I/O0–I/O7	Parallel Data Inputs or TRI-STATE Parallel Outputs
Q0–Q7	Serial Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS299			DM74LS299			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW S0 or S1 to CP	24 24			24 24			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW S0 or S1 to CP	5 5			0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW I/O$_n$, D$_{S0}$, D$_{S7}$ to CP	15 15			10 10			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW I/O$_n$, D$_{S0}$, D$_{S7}$ to CP	5 5			0 0			ns
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	15 15			15 15			ns
$t_w(L)$	$\overline{MR}$ Pulse Width LOW	15			15			ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	10			10			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.55	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V	Inputs			0.1	mA
			Sn			0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Sn			40	μA
			Inputs			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Sn			−0.8	mA
			Inputs			−0.4	mA

Electrical Characteristics (Continued)

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max, $\overline{OE}$ = 4.5V				60	mA
I_{OZH}	TRI-STATE Output Off Current High	$V_{CC} = V_{CCH}$ V_{OZH} = 2.7V				40	μA
I_{OZL}	TRI-STATE Output Off Current Low	$V_{CC} = V_{CCH}$ V_{OZL} = 0.4V				−400	μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

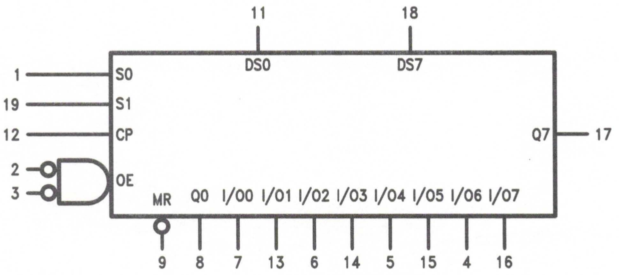
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	R_L = 2 kΩ C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Input Frequency	35		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q0 or Q7		26 28	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		25 35	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q0 or Q7		28	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n		35	ns
t_{PZH} t_{PZL}	Output Enable Time		18 25	ns
t_{PHZ} t_{PLZ}	Output Disable Time		15 20	ns

Logic Symbol



TL/F/9827-2

V_{CC} = Pin 20
GND = Pin 10

Functional Description

The 'LS299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by the S0 and S1, as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q0 and Q7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

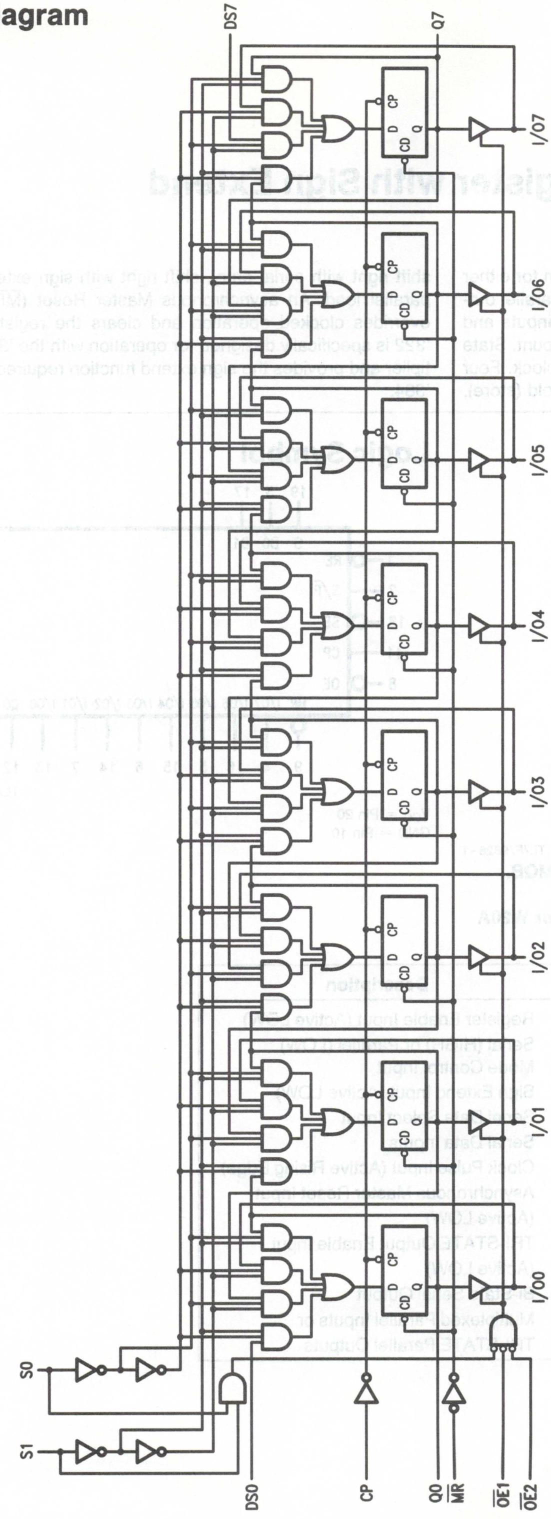
A HIGH signal on either $\overline{OE}1$ or $\overline{OE}2$ disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S0 and S1 in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
$\overline{MR}$	S1	S0	CP	
L	X	X	X	Asynchronous Reset; Q0–Q7 = LOW
H	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↑	Shift Right; $D_{S0} \rightarrow Q0$, $Q0 \rightarrow Q1$, etc.
H	H	L	↑	Shift Left; $D_{S7} \rightarrow Q7$, $Q7 \rightarrow Q6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram


DS7
Q7
I/O7
I/O6
I/O5
I/O4
I/O3
I/O2
I/O1
I/O0
D
Q
CP
CD
S0
S1
DS0
CP
Q0
MR
OE1
OE2

TL/F/9827-3

National Semiconductor

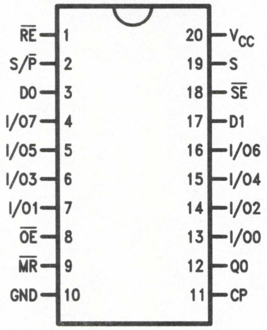
54LS322/DM74LS322
8-Bit Serial/Parallel Register with Sign Extend

General Description

The 'LS322 is an 8-bit shift register with provision for either serial or parallel loading and with TRI-STATE® parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register. The '322 is specifically designed for operation with the '384 Multiplier and provides the sign extend function required for the '384.

Connection Diagram

Dual-In-Line Package

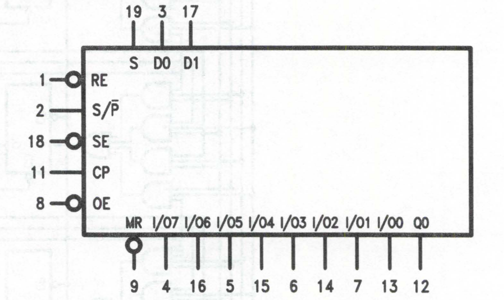


RE
S/P
D0
I/O7
I/O5
I/O3
I/O1
OE
MR
GND
1
2
3
4
5
6
7
8
9
10
20
19
18
17
16
15
14
13
12
11
VCC
S
SE
D1
I/O6
I/O4
I/O2
I/O0
Q0
CP

TL/F/9828-1

Order Number 54LS322DMQB, 54LS322FMQB, DM74LS322WM or DM74LS322N
See NS Package Number J20A, M20B, N20A or W20A

Logic Symbol



19
3
17
S
D0
D1
1
RE
2
S/P
18
SE
11
CP
8
OE
MR
I/O7
I/O6
I/O5
I/O4
I/O3
I/O2
I/O1
I/O0
Q0
9
4
16
5
15
6
14
7
13
12

TL/F/9828-2

V_{CC} = Pin 20
GND = Pin 10

Pin Names	Description
$\overline{RE}$	Register Enable Input (Active LOW)
S/$\overline{P}$	Serial (HIGH) or Parallel (LOW) Mode Control Input
$\overline{SE}$	Sign Extend Input (Active LOW)
S	Serial Data Select Input
D0, D1	Serial Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
Q0	Bi-State Serial Output
I/O0–I/O7	Multiplexed Parallel Inputs or TRI-STATE Parallel Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS322			DM74LS322			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{RE}$ to CP	24 24			24 24			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{RE}$ to CP	5 5			0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW D0, D1 or I/O_n to CP	15 15			10 10			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D0, D1 or I/O_n to CP	5 5			0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{SE}$ to CP	15 15			15 15			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{SE}$ to CP	0 0			0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW S$\overline{P}$ to CP	24 24			24 24			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW S to CP	15 15			15 15			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW S or S$\overline{P}$ to CP	0 0			0 0			ns
t_w (H)	CP Pulse Width HIGH	15			15			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	15			15			ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	15			15			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	54LS		2.5			V
			DM74		2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS				0.4	V
			DM74			0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V					0.1	mA
			S Input				0.2	
			SE Input				0.3	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	µA
			S Input				40	
			SE Input				60	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.4	mA
		V_{CC} = Max, V_I = 0.4V	S Input				−0.8	
		V_{CC} = Max, V_I = 0.4V	SE Input				−1.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	I/On	−30		−130	mA
				Qn	−20		−100	
			DM74		−20		−100	
I_{CC}	Supply Current	V_{CC} = Max					60	mA
I_{OZH}	TRI-STATE Output Off Current HIGH	V_{CC} = V_{CCH} V_{OZH} = 2.7V					40	µA
I_{OZL}	TRI-STATE Output Off Current LOW	V_{CC} = V_{CCH} V_{OZL} = 0.4V					−0.4	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF				Units
		54LS		DM74LS		
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	35		35		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n**		25 35		25 34	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q0		26 28		26 29	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n**		35		34.1	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q0		28		28	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n**		18 25		21.5 23.9	ns

**C_L = 50 pF

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF				Units
		54LS		DM74LS		
		Min	Max	Min	Max	
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O$_n$*		15 20		15 15	ns
t_{PZH} t_{PZL}	Output Enable Time S/$\overline{P}$ to I/O$_n$**		22 30		25.2 25.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time S$\overline{P}$ to I/O$_n$*		23 23		40.2 26.8	ns

*C_L = 5 pF

**C_L = 50 pF

Functional Description

The LS322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on $\overline{RE}$ enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on S/$\overline{P}$ enables shift right, while a LOW signal disables the TRI-STATE output buffers and enables parallel loading. In the shift right mode a HIGH signal on $\overline{SE}$ enables serial entry from either D0 or D1, as determined by the S input. A LOW signal on $\overline{SE}$ enables shift right but Q7 reloads its contents, thus performing the sign extend function required for the '384 Twos Complement Multiplier. A HIGH signal on $\overline{OE}$ disables the TRI-STATE output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

Mode Table

Mode	Inputs							Outputs								
	$\overline{MR}$	$\overline{RE}$	S/$\overline{P}$	$\overline{SE}$	S	$\overline{OE}$*	CP	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Q0
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	↑	I7	I6	I5	I4	I3	I2	I1	I0	I0
Shift Right	H	L	H	H	L	L	↑	D0	O7	O6	O5	O4	O3	O2	O1	O1
	H	L	H	H	H	L	↑	D1	O7	O6	O5	O4	O3	O2	O1	O1
Sign Extend	H	L	H	L	X	L	↑	O7	O7	O6	O5	O4	O3	O2	O1	O1
Hold	H	H	X	X	X	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC

*When the $\overline{OE}$ input is HIGH, all I/O$_n$ terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

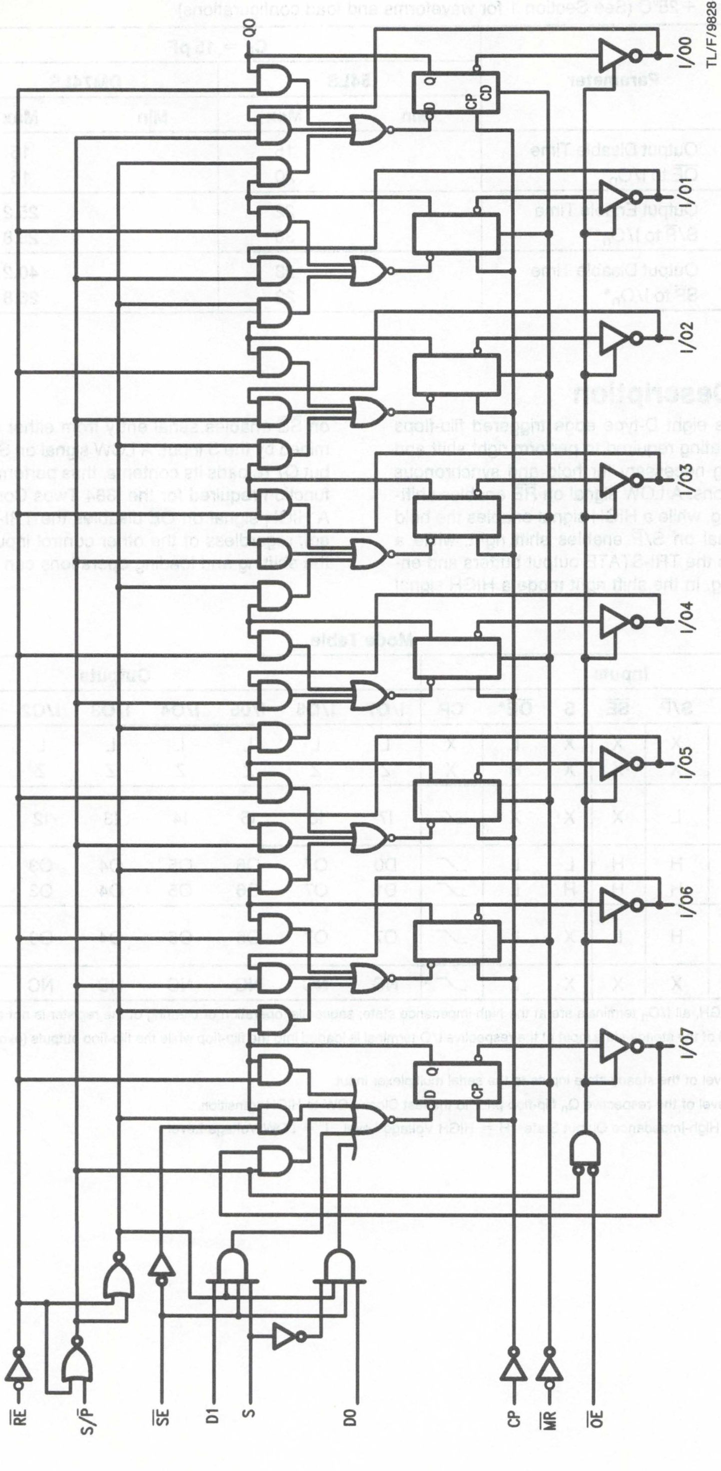
Note 1: I7–I0 = The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q0) are isolated from the I/O terminal.

Note 2: D0, D1 = The level of the steady-state inputs to the serial multiplexer input.

Note 3: O7–O0 = The level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

NC = No Change Z = High-Impedance Output State H = HIGH Voltage Level L = LOW Voltage Level

Logic Diagram


Q0
I/00
I/01
I/02
I/03
I/04
I/05
I/06
I/07
D
Q
CP
CD
RE
S/P
SE
D1
S
D0
CP
MR
OE

TL/F/9828-3

National Semiconductor

54LS323/DM74LS323
8-Bit Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

General Description

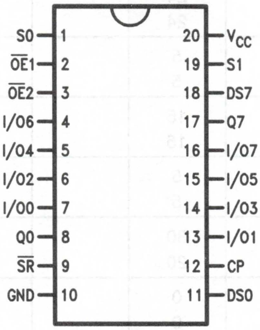
The 'LS323 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Its function is similar to the 'LS299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate inputs and outputs are provided for flip-flops Q0 and Q7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right, and parallel load. All modes are activated on the LOW-to-HIGH transition of the Clock.

Features

- Common I/O for reduced pin count
- Four operation modes: shift left, shift right, parallel load and store
- Separate continuous inputs and outputs from Q0 and Q7 allow easy cascading
- Fully synchronous reset
- TRI-STATE outputs for bus oriented applications

Connection Diagram

Dual-In-Line Package



TL/F/9829–1

Order Number 54LS323DMQB, 54LS323FMQB, DM74LS323WM or DM74LS323N
See NS Package Number J20A, M20B, N20A or W20A

Pin Names	Description
CP	Clock Pulse Input (Active Rising Edge)
D_S0	Serial Data Input for Right Shift
D_S7	Serial Data Input for Left Shift
S0, S1	Mode Select Inputs
$\overline{SR}$	Synchronous Reset Input (Active LOW)
$\overline{OE}1$, $\overline{OE}2$	TRI-STATE Output Enable Inputs (Active LOW)
I/O0–I/O7	Parallel Data Inputs or TRI-STATE Parallel Outputs
Q0, Q7	Serial Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS323			DM74LS323			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW S0 or S1 to CP	24 24			24 24			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW S0 or S1 to CP	5 5			0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW I/O_n, D_S0, D_S7 to CP	15 15			10 10			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW I/O_n, D_S0, D_S7 to CP	5 5			0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{SR}$ to CP	30 20			15 15			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{SR}$ to CP	0 0			0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	15 15			15 15			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
			S_n Inputs			0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
			S_n Inputs			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
			S_n Inputs			−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				60	mA
I_{OZH}	TRI-STATE Output Off Current HIGH	V_{CC} = V_{CCH} V_{OZH} = 2.7V				40	μA
I_{OZL}	TRI-STATE Output Off Current LOW	V_{CC} = V_{CCH} V_{OZL} = 0.4V				−400	μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	54LS323		DM74LS323		Units
		C_L = 15 pF		R_L = 2 kΩ, C_L = 15 pF		
		Min	Max	Min	Max	
f_{max}	Maximum Input Frequency	35		35		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q0 or Q7		26 28		23 25	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		25 35		25 29	ns
t_{PZH} t_{PZL}	Output Enable Time C_L = 50 pF		18 25		18 23	ns
t_{PHZ} t_{PLZ}	Output Disable Time C_L = 5 pF		15 20		15 15	ns

Functional Description

The 'LS323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S0 and S1 as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q0 and Q7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

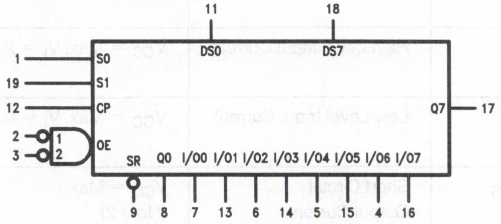
A HIGH signal on either $\overline{OE}1$ or $\overline{OE}2$ disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S0 and S1 in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
$\overline{SR}$	S1	S0	CP	
L	X	X	↑	Synchronous Reset; Q0–Q7 = LOW
H	H	H	↑	Parallel Load; I/O$_n$ → Q$_n$
H	L	H	↑	Shift Right; DS0 → Q0, Q0 → Q1, etc.
H	H	L	↑	Shift Left; DS7 → Q7, Q7 → Q6, etc.
H	H	H	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

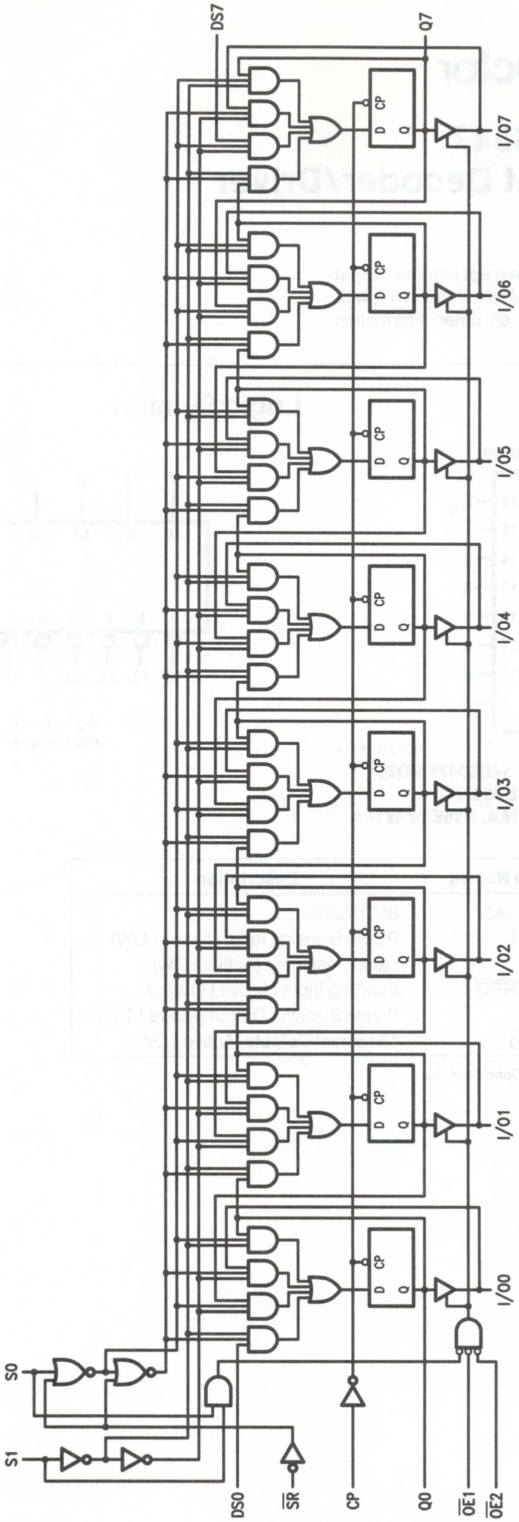
Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

TL/F/9829-2

Logic Diagram


DS7
Q7
CP
D
Q
I/O7
I/O6
I/O5
I/O4
I/O3
I/O2
I/O1
I/O0
S0
S1
DS0
$\overline{SR}$
CP
Q0
$\overline{OE1}$
$\overline{OE2}$

TL/F/9829-3

National Semiconductor

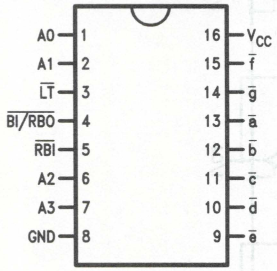
54LS347/DM74LS347
BCD to 7-Segment Decoder/Driver

General Description

The 'LS347 is the same as the 'LS47 except that the Output OFF Voltage, V_{OH}, is specified as 7.0V rather than 15V, with the same I_{OH} limit of 250 μA. For all other information please refer to the 'LS47 data sheet.

Connection Diagram

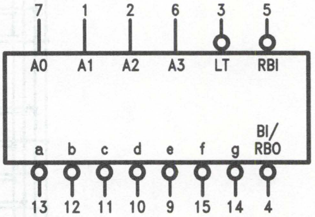
Dual-In-Line Package


A0 1
A1 2
LT 3
BI/RBO 4
RBI 5
A2 6
A3 7
GND 8
16 VCC
15 f
14 g
13 a
12 b
11 c
10 d
9 e

TL/F/10184-1

Order Number 54LS347DMQB, 54LS347FMQB, DM74LS347M or DM74LS347N
See NS Package Number J16A, M16A, N16E or W16A

Logic Symbol


7
1
2
6
3
5
A0
A1
A2
A3
LT
RBI
BI/RBO
a
b
c
d
e
f
g
13
12
11
10
9
15
14
4

TL/F/10184-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI}/\overline{RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
$\overline{a}$–$\overline{g}$	*Segment Outputs (Active LOW)

*OC—Open Collector

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS347			DM74LS347			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Voltage			−50			−50	μA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V		−0.03		−0.4	mA
		BI/$\overline{RBO}$ Input		−0.09		−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−0.3		−2.0	mA
			DM74	−0.3		−2.0	
I_{CC}	Supply Current	V_{CC} = Max				13	mA
I_{OFF}		Segment Outputs, V_O = 7V				250	μA

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Loading)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay		100	ns
t_{PHL}	A_n to $\overline{a}-\overline{g}$		100	ns
t_{PLH}	Propagation Delay		100	ns
t_{PHL}	$\overline{RBI}$ to $\overline{a}-\overline{g}$		100	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

54LS352/DM74LS352 Dual 4-Line to 1-Line Data Selectors/Multiplexers

General Description

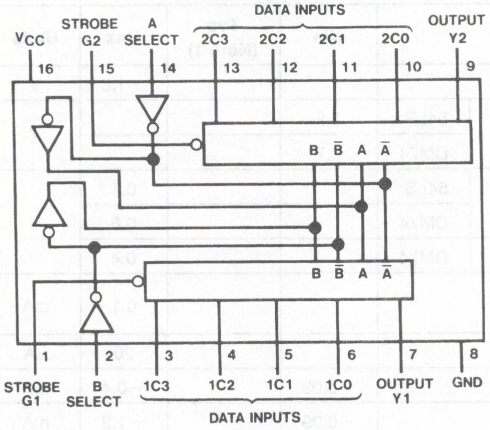
Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

- Inverting version of DM54/74LS153
- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low-impedance, totem-pole outputs
- Typical average propagation delay times
  - From data 15 ns
  - From strobe 19 ns
  - From select 22 ns
- Typical power dissipation 31 mW

Connection Diagram

Dual-In-Line Package


DATA INPUTS
VCC
STROBE G2
A SELECT
2C3
2C2
2C1
2C0
OUTPUT Y2
16
15
14
13
12
11
10
9
B
B̄
A
Ā
B
B̄
A
Ā
1
2
3
4
5
6
7
8
STROBE G1
B SELECT
1C3
1C2
1C1
1C0
OUTPUT Y1
GND
DATA INPUTS

TL/F/6425-1

Order Number 54LS352DMQB, 54LS352FMQB, DM74LS352M or DM74LS352N
See NS Package Number J16A, M16A, N16E or W16A

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55° C to +125°C
DM74LS	0° C to +70°C
Storage Temperature Range	−65° C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS352			DM74LS352			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			12			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V	54LS			0.1	mA
		V_{CC} = Max, V_I = 7V	DM74				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.2	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

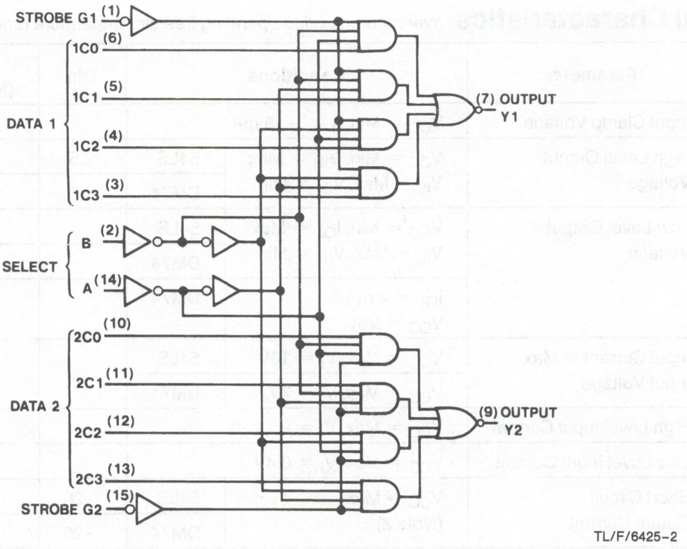
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all other inputs at ground.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	54LS C_L = 15 pF		DM74LS C_L = 50 pF R_L = 2 kΩ		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		12		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		12		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		22		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		38		47	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		15		29	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		20		41	ns

Logic Diagram


STROBE G1 (1)
DATA 1
1C0 (6)
1C1 (5)
1C2 (4)
1C3 (3)
(7) OUTPUT Y1
SELECT
B (2)
A (14)
DATA 2
2C0 (10)
2C1 (11)
2C2 (12)
2C3 (13)
(9) OUTPUT Y2
STROBE G2 (15)

TL/F/6425-2

National Semiconductor

54LS353/DM74LS353
Dual 4-Input Multiplexer with TRI-STATE® Outputs

General Description

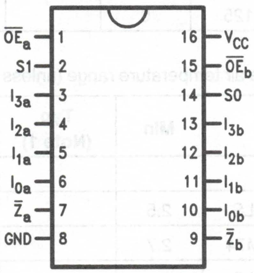
The '353 is a dual 4-input multiplexer with TRI-STATE outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all National TTL families.

Features

- Inverted version of 'LS253
- Schottky process for high speed
- Multifunction capability

Connection Diagram

Dual-In-Line Package

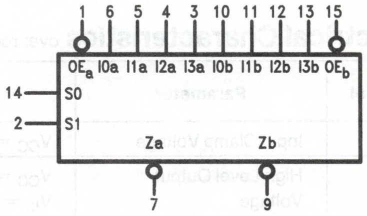


$\overline{OE}_a$ 1
S1 2
I_{3a} 3
I_{2a} 4
I_{1a} 5
I_{0a} 6
$\overline{Z}_a$ 7
GND 8
16 V_{CC}
15 $\overline{OE}_b$
14 S0
13 I_{3b}
12 I_{2b}
11 I_{1b}
10 I_{0b}
9 $\overline{Z}_b$

TL/F/10185-1

Order Number 54LS353DMQB, 54LS353FMQB, DM74LS353M or DM74LS353N
See NS Package Number J16A, M16A, N16E or W16A

Logic Symbol



1 6 5 4 3 10 11 12 13 15
OE_a I0a I1a I2a I3a I0b I1b I2b I3b OE_b
14 S0
2 S1
Za Zb
7 9

TL/F/10185-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
I0a–I3a	Side A Data Inputs
I0b–I3b	Side B Data Inputs
S0, S1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input (Active Low)
$\overline{OE}_b$	Side B Output Enable Input (Active Low)
$\overline{Z}_a$, $\overline{Z}_b$	TRI-STATE Outputs (Inverted)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS353			DM74LS353			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1.0			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−30		−130	mA
			DM74	−30		−130	
I_{CCL}	Supply Current Outputs HIGH	V_{CC} = Max, In, Sn, $\overline{OE}$n = GND				12	mA
I_{CCZ}	Supply Current Outputs OFF	V_{CC} = Max, $\overline{OE}$n = 4.5V In, Sn = GND				14	mA
I_{OZH}	TRI-STATE Output OFF Current HIGH	V_{CC} = V_{CCH} V_{OZH} = 2.7V				20	μA
I_{OZL}	TRI-STATE Output OFF Current LOW	V_{CC} = V_{CCH} V_{OZL} = 0.4V				−20	μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output loads)

Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 50\ pF$		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Sn to $\overline{Z}$n		24 32	ns
t_{PLH} t_{PHL}	Propagation Delay In to $\overline{Z}$n		15 15	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Zn		18 18	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Zn		18 18	ns

Functional Description

The 'LS353 contains two identical 4-input multiplexers with TRI-STATE outputs. They select two bits from four sources selected by common Select inputs (S0, S1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$), $\overline{OE}_b$) inputs which when HIGH, force the outputs to a high impedance (high Z) state. The logic equations for the outputs are shown below:

If the outputs of TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so that there is no overlap.

$$\overline{\overline{Z}_a = \overline{OEa} \bullet (I0a \bullet \overline{S1} \bullet \overline{S0} + I1a \bullet \overline{S1} \bullet S0 + I2a \bullet S1 \bullet \overline{S0} + I3a \bullet S1 \bullet S0)}$$

$$\overline{\overline{Z}_b = \overline{OE_b} \bullet (I0b \bullet \overline{S1} \bullet \overline{S0} + I1b \bullet \overline{S1} \bullet S0 + I2b \bullet S1 \bullet \overline{S0} + I3b \bullet S1 \bullet S0)}$$

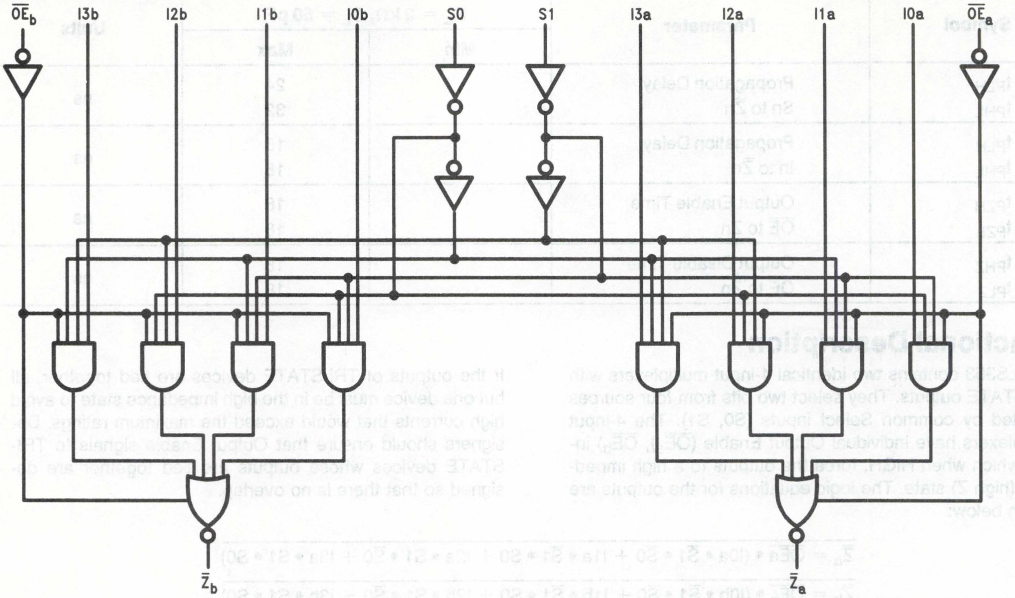
Truth Table

Select Inputs		Data Inputs				Output Enable	Output
S0	S1	I0	I1	I2	I3	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs S0 and S1 are common to both sections.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance

Logic Diagram


$\overline{OE}_b$
I3b
I2b
I1b
I0b
S0
S1
I3a
I2a
I1a
I0a
$\overline{OE}_a$
$\overline{Z}_b$
$\overline{Z}_a$

TL/F/10185–3

National Semiconductor

54LS365A/DM54LS365A/DM74LS365A Hex TRI-STATE® Buffers

General Description

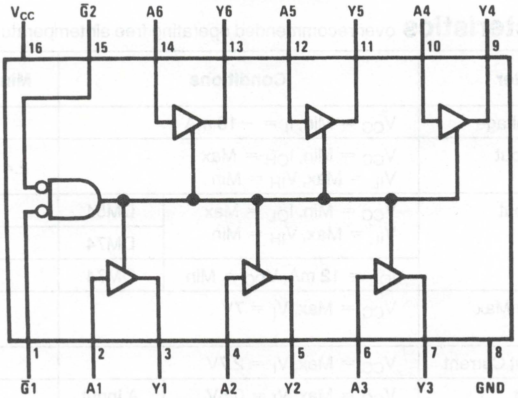
This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Features

- Alternate Military/Aerospace device (54LS365A) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6427–1

Order Number 54LS365ADMQB, 54LS365AFMQB, 54LS365ALMQB, DM54LS365AJ, DM54LS365AW, DM74LS265AM or DM74LS365AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Y = A

Input			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	H	H
L	L	L	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS365A			DM74LS365A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 4)	A Input			−20	µA
		V_{CC} = Max, V_I = 0.4V (Note 5)	A Input			−0.4	mA
		V_{CC} = Max, V_I = 0.4V	$\overline{G}$ Input			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			14	24	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs at 0.4V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 667\Omega$				Units
		$C_L = 50$ pF		$C_L = 150$ pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		16		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		16		25	ns
t_{PZH}	Output Enable Time to High Level Output		30		40	ns
t_{PZL}	Output Enable Time to Low Level Output		30		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 6)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 6)		20			ns

Note 6: $C_L = 5$ pF.

National Semiconductor

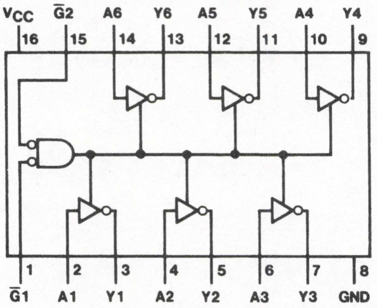
54LS366A/DM74LS366A
Hex TRI-STATE® Inverting Buffers

General Description

This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6428-1

Order Number 54LS366ADMQB, 54LS366AFMQB, 54LS366ALMQB, DM74LS366AM or DM74LS366AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

$Y = \overline{A}$

Inputs			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	L	H
L	L	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS366A			DM74LS366A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	54LS		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_{CC} = Max, V_I = 10.0V	54LS				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 4)	A Input			−20	µA
		V_{CC} = Max, V_I = 0.4V (Note 5)	A Input			−0.4	mA
		V_{CC} = Max, V_I = 0.4V	$\overline{G}$ Input			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−30		−130	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			12	21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs at 0.4V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	54LS C_L = 50 pF		DM74LS C_L = 150 pF R_L = 667Ω		Units
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		12		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		22		25	ns
t_{PZH}	Output Enable Time to High Level Output		24		35	ns
t_{PZL}	Output Enable Time to Low Level Output		30		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 6)		25			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 6)		20			ns

Note 6: C_L = 5 pF.

National Semiconductor

54LS367A/DM54LS367A/DM74LS367A Hex TRI-STATE® Buffers

General Description

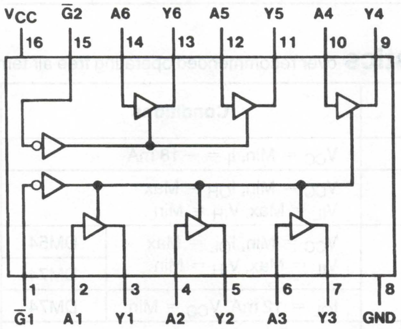
This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Features

- Alternate military/aerospace device (54LS367A) is available. Contact a National Semiconductor sales office/distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6429–1

Order Number 54LS367ADMQB, 54LS367AFMQB, 54LS367ALMQB, DM54LS367AJ, DM54LS367AW, DM74LS367AM or DM74LS367AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Y = A

Inputs		Output
A	$\overline{G}$	Y
L	L	L
H	L	H
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS367A			DM74LS367A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 4)	A Input			−20	μA
		V_{CC} = Max, V_I = 0.4V (Note 5)	A Input			−0.4	mA
		V_{CC} = Max, V_I = 0.4V	$\overline{G}$ Input			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			14	24	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs at 0.4V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 667\Omega$				Units
		$C_L = 50$ pF		$C_L = 150$ pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		16		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		16		25	ns
t_{PZH}	Output Enable Time to High Level Output		30		40	ns
t_{PZL}	Output Enable Time to Low Level Output		30		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 6)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 6)		20			ns

Note 6: $C_L = 5$ pF.

National Semiconductor

54LS368A/DM54LS368A/DM74LS368A Hex TRI-STATE® Inverting Buffers

General Description

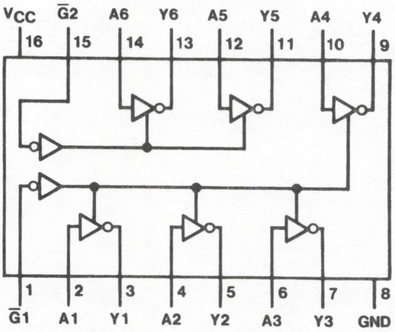
This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Features

- Alternate Military/Aerospace device (54LS368) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6430–1

Order Number 54LS368ADMQB, 54LS368AFMQB, 54LS368ALMQB, DM54LS368AJ, DM54LS368AW, DM74LS368AM or DM74LS368AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

$Y = \overline{A}$

Inputs		Output
A	$\overline{G}$	Y
L	L	H
H	L	L
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS368A			DM74LS368A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 4)	A Input			−20	μA
		V_{CC} = Max, V_I = 0.4V (Note 5)	A Input			−0.4	mA
		V_{CC} = Max, V_I = 0.4V	$\overline{G}$ Input			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			12	21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs at 0.4V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 667\Omega$				Units
		$C_L = 50$ pF		$C_L = 150$ pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		15		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		18		25	ns
t_{PZH}	Output Enable Time to High Level Output		30		35	ns
t_{PZL}	Output Enable Time to Low Level Output		30		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 6)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 6)		20			ns

Note 6: $C_L = 5$ pF.

National Semiconductor

DM54LS373/DM74LS373, 54LS374/DM54LS374/DM74LS374 TRI-STATE® Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. (Continued)

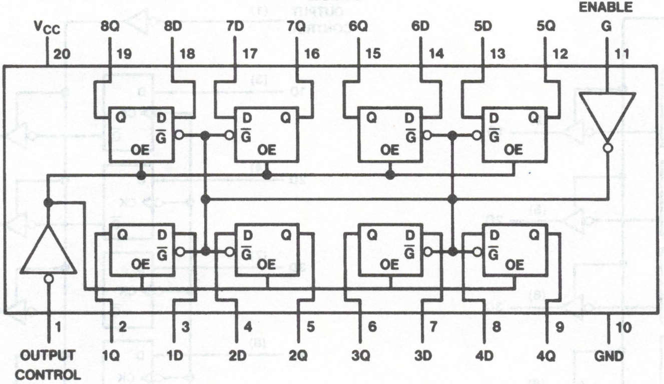
Features

- Choice of 8 latches or 8 D-type flip-flops in a single package
- TRI-STATE bus-driving outputs
- Full parallel-access for loading
- Buffered control inputs
- P-N-P inputs reduce D-C loading on data lines
- Alternate military/aerospace device (54LS374) is available. Contact a National Semiconductor sales office/distributor for specifications.

Connection Diagrams

Dual-In-Line Packages

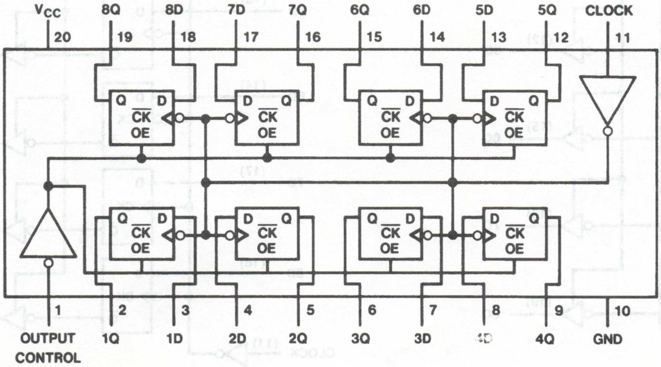
'LS373


V_{CC} 20
8Q 19
8D 18
7D 17
7Q 16
6Q 15
6D 14
5D 13
5Q 12
ENABLE G 11
Q D G OE
1 OUTPUT CONTROL
2 1Q
3 1D
4 2D
5 2Q
6 3Q
7 3D
8 4D
9 4Q
10 GND

Order Number DM54LS373J, DM54LS373W, DM74LS373N or DM74LS373WM
See NS Package Number J20A, M20B, N20A or W20A

TL/F/6431-1

'LS374


V_{CC} 20
8Q 19
8D 18
7D 17
7Q 16
6Q 15
6D 14
5D 13
5Q 12
CLOCK 11
Q D CK OE
1 OUTPUT CONTROL
2 1Q
3 1D
4 2D
5 2Q
6 3Q
7 3D
8 4D
9 4Q
10 GND

Order Number 54LS374DMQB, 54LS374FMQB, 54LS374LMQB, DM54LS374J, DM54LS374W, DM74LS374WM or DM74LS374N
See NS Package Number E20A, J20A, M20B, N20A or W20A

TL/F/6431-2

General Description (Continued)

The eight latches of the DM54/74LS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

The eight flip-flops of the DM54/74LS374 are edge-triggered D-type flip flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Function Tables

DM54/74LS373

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

DM54/74LS374

Output Control	Clock	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care

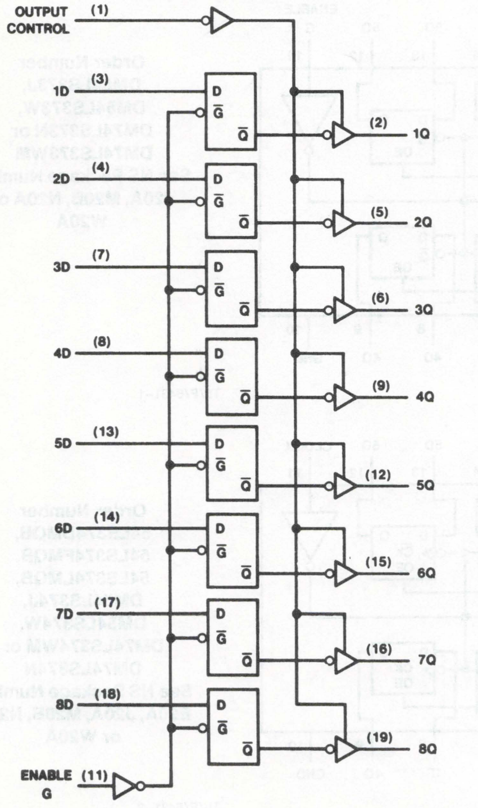
↑ = Transition from low-to-high level, Z = High Impedance State

Q_0 = The level of the output before steady-state input conditions were established.

Logic Diagrams

DM54/74LS373

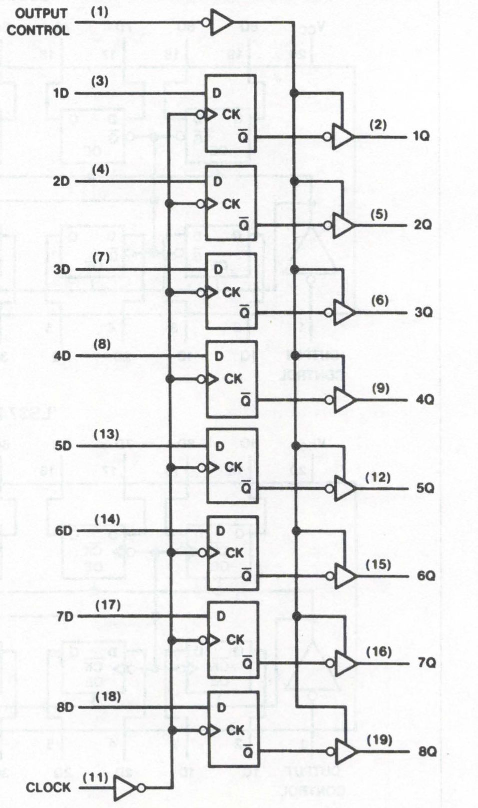
Transparent Latches


OUTPUT CONTROL (1)
1D (3)
2D (4)
3D (7)
4D (8)
5D (13)
6D (14)
7D (17)
8D (18)
ENABLE G (11)
D
G
Q
(2) 1Q
(5) 2Q
(6) 3Q
(9) 4Q
(12) 5Q
(15) 6Q
(16) 7Q
(19) 8Q

TL/F/6431-3

DM54/74LS374

Positive-Edge-Triggered Flip-Flops


OUTPUT CONTROL (1)
1D (3)
2D (4)
3D (7)
4D (8)
5D (13)
6D (14)
7D (17)
8D (18)
CLOCK (11)
D
CK
Q
(2) 1Q
(5) 2Q
(6) 3Q
(9) 4Q
(12) 5Q
(15) 6Q
(16) 7Q
(19) 8Q

TL/F/6431-4

Absolute Maximum Ratings (See Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS373			DM74LS373			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Votage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
t_W	Pulse Width (Note 2)	Enable High	15			15			ns
		Enable Low	15			15			
t_{SU}	Data Setup Time (Notes 1 & 2)		5↓			5↓			ns
t_H	Data Hold Time (Notes 1 & 2)		20↓			20↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 2: T_A = 25°C and V_{CC} = 5V.

'LS373 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min I_{OH} = Max V_{IL} = Max V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−50		−225	mA
			DM74	−50		−225	
I_{CC}	Supply Current	V_{CC} = Max			24	40	mA

'LS373 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω C_L = 45 pF Min	 Max	 C_L = 150 pF Min	 Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Q		18		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Q		18		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Q		30		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Q		30		36	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Any Q		28		36	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Any Q		36		50	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 3)	Output Control to Any Q		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 3)	Output Control to Any Q		25			ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: C_L = 5 pF.

Recommended Operating Conditions

Symbol	Parameter		DM54LS374 Min	 Nom	 Max	DM74LS374 Min	 Nom	 Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLK}	Clock Frequency (Note 2)		0		35	0		35	MHz
f_{CLK}	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width (Note 4)	Clock High	15			15			ns
		Clock Low	15			15			
t_{SU}	Data Setup Time (Notes 1 & 4)		20 ↑			20 ↑			ns
t_H	Data Hold Time (Notes 1 & 4)		1 ↑			1 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: C_L = 45 pF, R_L = 667Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 150 pF, R_L = 667Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

’LS374 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min I_{OH} = Max V_{IL} = Max V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−50		−225	mA
			DM74	−50		−225	
I_{CC}	Supply Current	V_{CC} = Max			27	45	mA

’LS374 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 45 pF		C_L = 150 pF		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	35		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		28		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		28		38	ns
t_{PZH}	Output Enable Time to High Level Output		28		44	ns
t_{PZL}	Output Enable Time to Low Level Output		28		44	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 3)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 3)		25			ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: C_L = 5 pF.

National Semiconductor

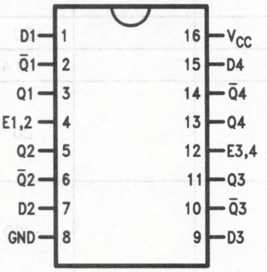
54LS375/DM74LS375
4-Bit Latch

General Description

The 'LS375 is a 4-bit D-type latch for use as temporary storage for binary information between processing units and input/output or indicator units. When its Enable (E) input is HIGH, a latch is transparent, i.e., the Q output will follow the D input each time it changes. When E is LOW a latch stores the last valid data present on the D input preceding the HIGH-to-LOW transition of E. The 'LS375 is functionally identical to the 'LS75 except for the corner power pins.

Connection Diagram

Dual-In-Line Package

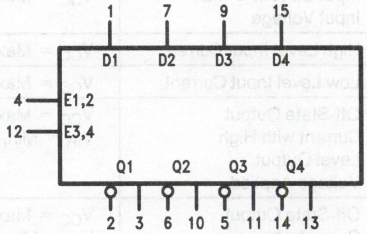


D1 1
$\overline{Q}$1 2
Q1 3
E1,2 4
Q2 5
$\overline{Q}$2 6
D2 7
GND 8
16 V_{CC}
15 D4
14 $\overline{Q}$4
13 Q4
12 E3,4
11 Q3
10 $\overline{Q}$3
9 D3

TL/F/9830-1

Order Number 54LS375DMQB, 54LS375FMQB, DM74LS375M or DM74LS375N
See NS Package Number J16A, M16A, N16E or W16A

Logic Symbol



1
7
9
15
D1
D2
D3
D4
4
E1,2
12
E3,4
Q1
Q2
Q3
Q4
2
3
6
10
5
11
14
13

TL/F/9830-2

V_{CC} = Pin 16
GND = Pin 8

Pin Name	Description
D1–D4	Data Inputs
E1, 2	Latches 1, 2 Enable Inputs
E3, 4	Latches 3, 4 Enable Inputs
Q1–Q4	Latch Outputs
$\overline{Q}$1–Q4	Complementary Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS375			DM74LS375			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to E_n	20			20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to E_n	0			0			ns
t_w (H)	E_n Pulse Width HIGH	20			15			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
			Enable Input			0.4	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
			Enable Input			80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
			Enable Input			−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				12	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	54LS/DM74LS C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		27 23	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{Q}_n$		20 15	ns
t_{PLH} t_{PHL}	Propagation Delay E_n to Q_n		27 25	ns
t_{PLH} t_{PHL}	Propagation Delay E_n to $\overline{Q}_n$		30 18	ns

Truth Table (Each Latch)

t_n	$t_n + 1$
D	Q
H	H
L	L

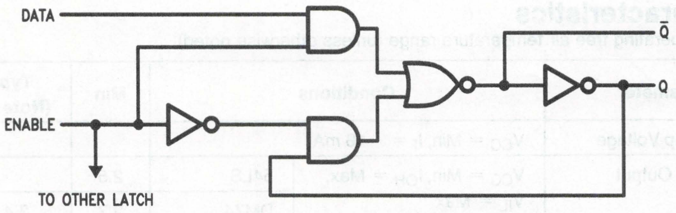
t_n = Bit time before Enable negative going transition.

t_{n+1} = Bit time after Enable negative going transition.

H = HIGH Voltage Level

L = LOW Voltage Level

Logic Diagram (1/4 of diagram shown)



TL/F/9830-3

National Semiconductor

54LS377/DM74LS377
Octal D Flip-Flop with Common Enable and Clock

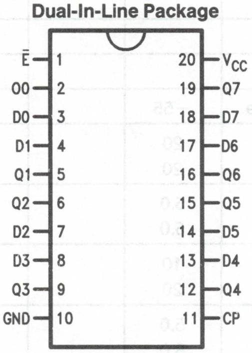
General Description

The 'LS377 is an 8-bit register built using advanced low power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common input enable. The device is packaged in the space-saving (0.3 inch row spacing) 20-pin package.

Features

- 8-bit high speed parallel registers
- Positive edge-triggered D-type flip-flops
- Fully buffered common clock and enable inputs

Connection Diagram


Dual-In-Line Package
Ē 1
Q0 2
D0 3
D1 4
Q1 5
Q2 6
D2 7
D3 8
Q3 9
GND 10
20 V_CC
19 Q7
18 D7
17 D6
16 Q6
15 Q5
14 D5
13 D4
12 Q4
11 CP

TL/F/9831-1

Order Number 54LS377DMQB, 54LS377FMQB, 54LS377LMQB, DM74LS377WM or DM74LS377N
See NS Package Number
E20A, J20A, M20B, N20A or W20A

Pin Names	Description
Ē	Enable Input (Active LOW)
D0–D7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
Q0–Q7	Flip-Flop Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS377			DM74LS377			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	20 20			10 10			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	5.0 5.0			5.0 5.0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{E}$ to CP	10 20			10 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{E}$ to CP	5.0 5.0			5.0 5.0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 20			20 20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20.0	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				28	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 15\ pF$		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		25 25	ns

Functional Description

The 'LS377 consists of eight edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable input ($\overline{E}$) are common to all flip-flops.

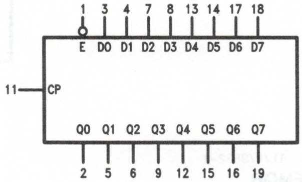
When $\overline{E}$ is LOW, new data is entered into the register on the next LOW-to-HIGH transition of CP. When $\overline{E}$ is HIGH, the register will retain the present data independent of the CP.

Truth Table

Inputs			Output
$\overline{E}$	CP	D_n	Q_n
H	X	X	No Change
L	↑	H	H
L	↑	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

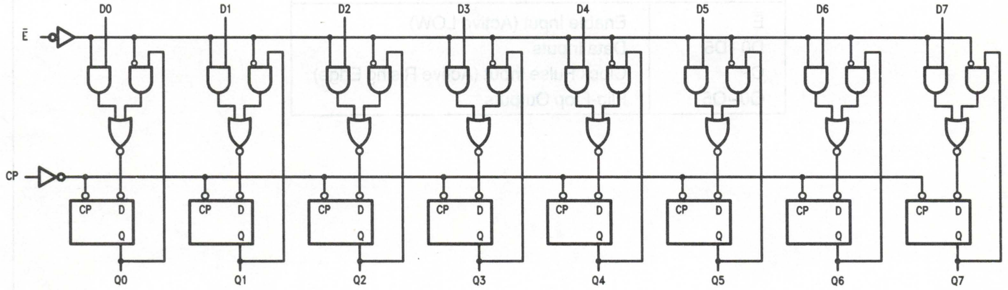
Logic Symbol


1
3
4
7
8
13
14
17
18
E
D0
D1
D2
D3
D4
D5
D6
D7
11
CP
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
2
5
6
9
12
15
16
19

TL/F/9831-2

V_{CC} = Pin 20
GND = Pin 10

Logic Diagram


D0
D1
D2
D3
D4
D5
D6
D7
Ē
CP
CP
D
Q
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7

TL/F/9831-3

National Semiconductor

54LS378/DM74LS378 Parallel D Register with Enable

General Description

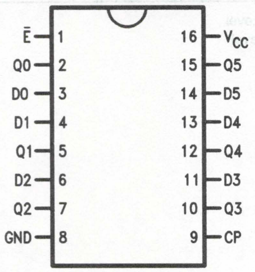
The 'LS378 is a 6-bit register with a buffered common enable. This device is similar to the 'LS174, but with common Enable rather than common Master Reset.

Features

- 6-bit high speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common clock and enable inputs
- Input clamp diodes limit high speed termination effects
- Full TTL and CMOS compatible

Connection Diagram

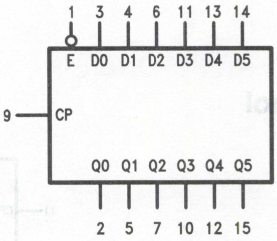
Dual-In-Line Package


Ē 1
Q0 2
D0 3
D1 4
Q1 5
D2 6
Q2 7
GND 8
16 V_{CC}
15 Q5
14 D5
13 D4
12 Q4
11 D3
10 Q3
9 CP

TL/F/9832-1

Order Number 54LS378DMQB, 54LS378FMQB, DM74LS378M or DM74LS378N
See NS Package Number J16A, M16A, N16E or W16A

Logic Symbol


1
3
4
6
11
13
14
E
D0
D1
D2
D3
D4
D5
9
CP
Q0
Q1
Q2
Q3
Q4
Q5
2
5
7
10
12
15

TL/F/9832-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
Ē	Enable Input (Active LOW)
D0–D5	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
Q0–Q5	Flip-Flop Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
54LS	−54°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS378			DM74LS378			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H)	Setup Time HIGH, D_n to CP	20			20			ns
t_h (H)	Hold Time HIGH, D_n to CP	5.0			5.0			ns
t_s (L)	Setup Time LOW, D_n to CP	20			20			ns
t_h (L)	Hold Time LOW, D_n to CP	5.0			5.0			ns
t_s (H)	Setup Time HIGH, $\overline{E}$ to CP	30			30			ns
t_h (H)	Hold Time HIGH, $\overline{E}$ to CP	5.0			5.0			ns
t_s (L)	Setup Time LOW, $\overline{E}$ to CP	30			30			ns
t_h (L)	Hold Time LOW, $\overline{E}$ to CP	5.0			5.0			ns
t_w (H)	CP Pulse Width HIGH	20			20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20.0	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max D_n; $\overline{E}$ = GND, CP = _/‾				22	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	2 kΩ, C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		27 27	ns

Functional Description

The 'LS378 consists of eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

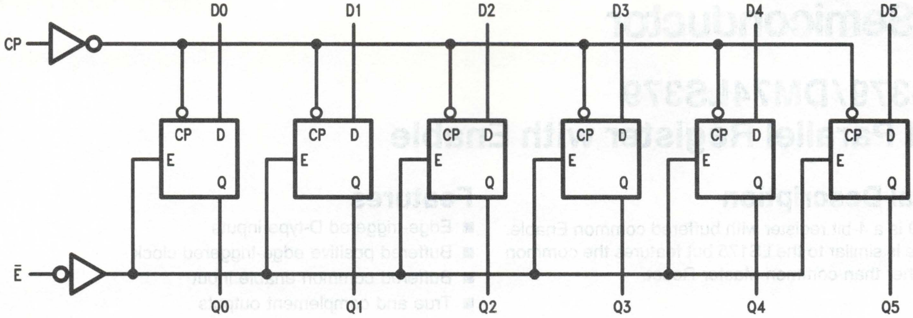
When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH the register will retain the present data independent of the CP input.

Truth Table

Inputs			Output
$\overline{E}$	CP	D_n	Q_n
H	↑	X	No change
L	↑	H	H
L	↑	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram


D0
D1
D2
D3
D4
D5
CP
Ē
CP
D
E
Q
Q0
Q1
Q2
Q3
Q4
Q5

TL/F/9832-3

National Semiconductor

54LS379/DM74LS379
Quad Parallel Register with Enable

General Description

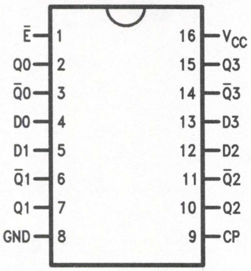
The LS379 is a 4-bit register with buffered common Enable. This device is similar to the LS175 but features the common Enable rather than common Master Reset.

Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Buffered common enable input
- True and complement outputs

Connection Diagram

Dual-In-Line Package

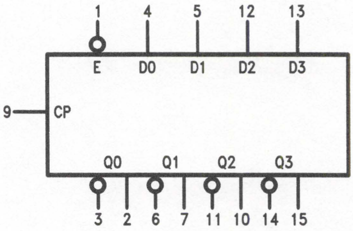


$\overline{E}$ 1
Q0 2
$\overline{Q}0$ 3
D0 4
D1 5
$\overline{Q}1$ 6
Q1 7
GND 8
16 V_{CC}
15 Q3
14 $\overline{Q}3$
13 D3
12 D2
11 $\overline{Q}2$
10 Q2
9 CP

TL/F/10186-1

Order Number 54LS379DMQB, 54LS379FMQB, 54LS379LMQB, DM74LS379M or DM74LS379N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Logic Symbol



1
4
5
12
13
E
D0
D1
D2
D3
9
CP
Q0
Q1
Q2
Q3
3
2
6
7
11
10
14
15

TL/F/10186-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{E}$	Enable Input (Active LOW)
D0–D3	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
Q0–Q3	Flip-Flop Outputs
$\overline{Q}0$–$\overline{Q}3$	Complement Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS379			DM74LS379			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW Dn to CP	20			20			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW Dn to CP	5			5			ns
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW $\overline{E}$ to CP	25			25			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW $\overline{E}$ to CP	5			5			ns
$t_w(L)$	CP Pulse Width LOW	17			17			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				18	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Note more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 15\ pF$		Units
		Min	Max	
t_{max}	Maximum Clock Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Qn		27 27	ns

Functional Description

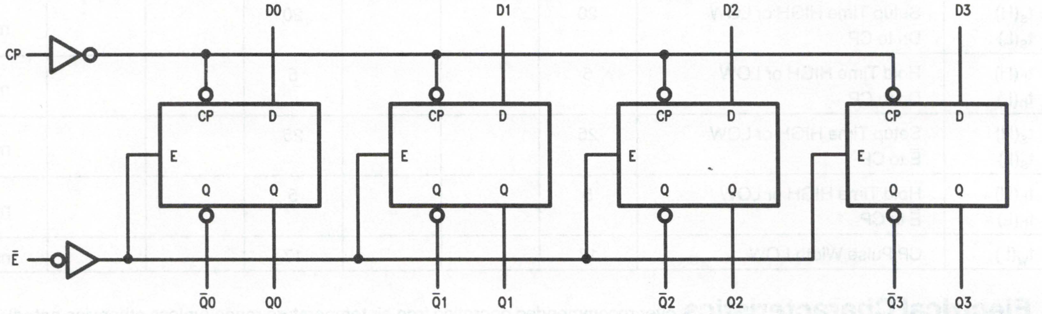
The LS379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input. The Dn and $\overline{E}$ inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

Truth Table

Inputs			Outputs	
$\overline{E}$	CP	Dn	Qn	$\overline{Q}n$
H	↑	X	No Change	No Change
L	↑	H	H	L
L	↑	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/10186–3

National Semiconductor

DM54LS380/74LS380 Multifunction Octal Register

General Description

The 'LS380 is an 8-bit synchronous register with parallel load, load complement, preset, clear, and hold capacity. Four control inputs ($\overline{LD}$, POL, $\overline{CLR}$, $\overline{PR}$) provide one of four operations which occur synchronously on the rising edge of the clock (CK). The LS380 combines the features of the LS374, LS377, LS273 and LS534 into a single 300 mil wide package.

The LOAD operation loads the inputs (D_7–D_0) into the output register (Q_7–Q_0), when POL is HIGH, or loads the compliment of the inputs when POL is LOW. The CLEAR operation resets the output register to all LOWs. The PRESET operation presets the output register to all HIGHs. The HOLD operation holds the previous value regardless of clock transitions. CLEAR overrides PRESET, PRESET overrides LOAD, and LOAD overrides HOLD.

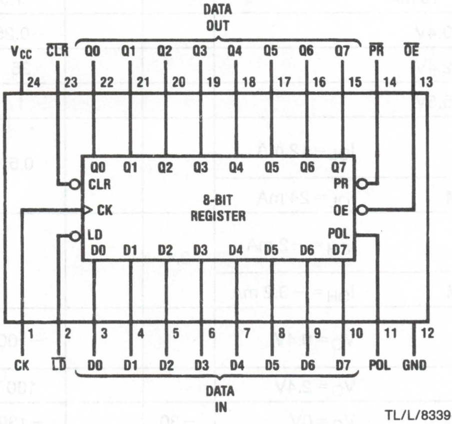
The output register (Q_7–Q_0) is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Features/Benefits

- Octal Register for general purposes interfacing applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP saves space
- TRI-STATE® outputs
- Low current PNP inputs reduce loading

Connection Diagram

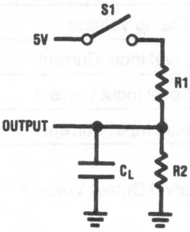
Top View


DATA OUT
VCC
CLR
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
PR
OE
24
23
22
21
20
19
18
17
16
15
14
13
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
CLR
PR
CK
8-BIT REGISTER
OE
LD
POL
D0 D1 D2 D3 D4 D5 D6 D7
1
2
3
4
5
6
7
8
9
10
11
12
CK
LD
D0
D1
D2
D3
D4
D5
D6
D7
POL
GND
DATA IN

TL/L/8339-1

Order Number DM54LS380J, DM74LS380J or DM74LS380N
See NS Package Number J24F or N24C

Standard Test Load


S1
5V
R1
OUTPUT
CL
R2

TL/L/8339-2

Function Table

$\overline{OC}$	CLK	$\overline{CLR}$	$\overline{PR}$	$\overline{LD}$	POL	D7–D0	Q7–Q0	Operation
H	X	X	X	X	X	X	Z	HI-Z
L	↑	L	X	X	X	X	L	CLEAR
L	↑	H	L	X	X	X	H	PRESET
L	↑	H	H	H	X	X	Q	HOLD
L	↑	H	H	L	H	D	D	LOAD true
L	↑	H	H	L	L	D	$\overline{D}$	LOAD comp

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65° to +150°C

Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		−55		125*	0		75	°C
t_w	Width of Clock	High	40			40			ns
		Low	35			35			
t_{SU}	Set-Up Time		60			50			ns
t_h	Hold Time		0	−15		0	−15		

*Case temperature

Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ†	Max	Units
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IH}	High-Level Input Voltage				2			V
V_{IC}	Input Clamp Voltage	$V_{CC}=MIN$	$I_I=-18$ mA				−1.5	V
I_{IL}	Low-Level Input Current	$V_{CC}=MAX$	$V_I=0.4V$				−0.25	mA
I_{IH}	High-Level Input Current	$V_{CC}=MAX$	$V_I=2.4V$				25	μA
I_I	Maximum Input Current	$V_{CC}=MAX$	$V_I=5.5V$				1	mA
V_{OL}	Low-Level Output Voltage	$V_{CC}=MIN$ $V_{IL}=0.8V$ $V_{IH}=2V$	MIL	$I_{OL}=12$ mA			0.5	V
			COM	$I_{OL}=24$ mA				
V_{OH}	High-Level Output Voltage	$V_{CC}=MIN$ $V_{IL}=0.8V$ $V_{IH}=2V$	MIL	$I_{OH}=-2$ mA	2.4			V
			COM	$I_{OH}=-3.2$ mA				
I_{OZL}	Off-State Output Current	$V_{CC}=MAX$ $V_{IL}=0.8V$ $V_{IH}=2V$		$V_O=0.4V$			−100	μA
I_{OZH}				$V_O=2.4V$			100	μA
I_{OS}	Output Short-Circuit Current*	$V_{CC}=5.0V$		$V_O=0V$	−30		−130	mA
I_{CC}	Supply Current	$V_{CC}=MAX$				120	180	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

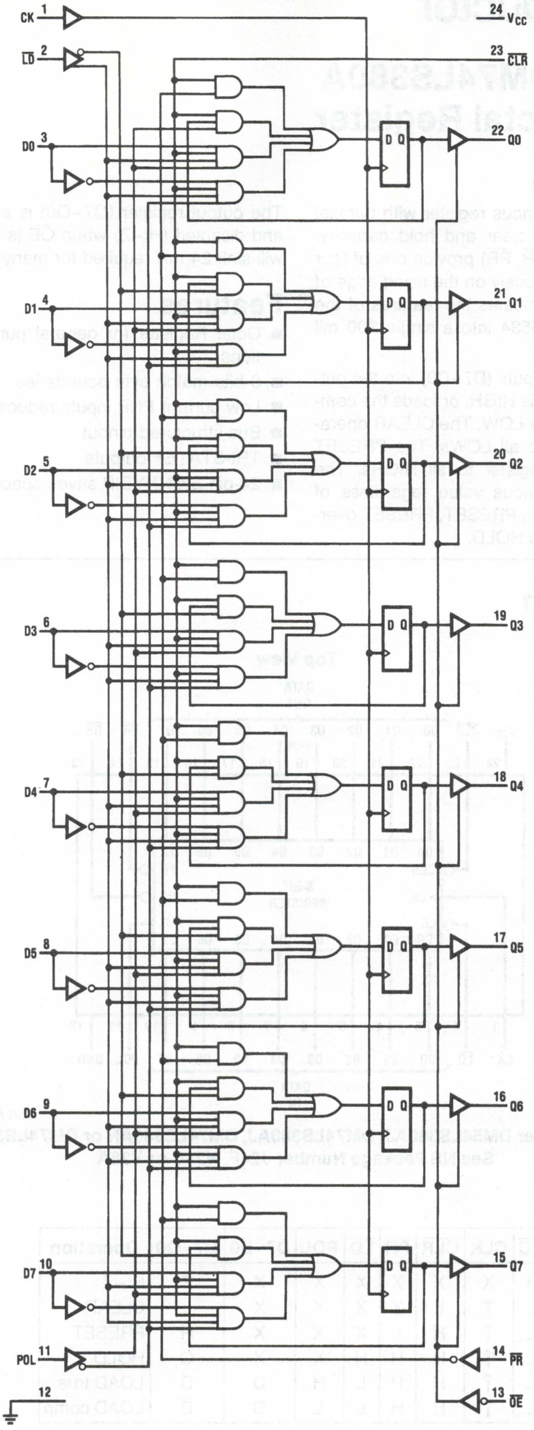
† All typical values are at $V_{CC}=5V$. $T_A=25°C$

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions (See Test Load)	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Clock Frequency	$C_L=50$ pF $R_1=200\Omega$ $R_2=390\Omega$	10.5			12.5			MHz
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PZX}	Output Enable Delay			35	55		35	45	ns
t_{PXZ}	Output Disable Delay			35	55		35	45	ns

Logic Diagram

Octal Register


CK
1
$\overline{\text{LD}}$
2
24
V_{CC}
23
$\overline{\text{CLR}}$
D0
3
22
Q0
D Q
D1
4
21
Q1
D2
5
20
Q2
D3
6
19
Q3
D4
7
18
Q4
D5
8
17
Q5
D6
9
16
Q6
D7
10
15
Q7
POL
11
14
$\overline{\text{PR}}$
12
13
$\overline{\text{OE}}$

TL/L/8339-4

National Semiconductor

DM54LS380A/DM74LS380A Multifunction Octal Register

General Description

The 'LS380A is an 8-bit synchronous register with parallel load, load complement, preset, clear and hold capacity. Four control inputs ($\overline{LD}$, POL, $\overline{CLR}$, $\overline{PR}$) provide one of four operations which occur synchronously on the rising edge of the clock (CK). The 'LS380A combines the features of the 'LS374, 'LS377, 'LS273 and 'LS534 into a single 300 mil wide package.

The LOAD operation loads the inputs (D7–D0) into the output register (Q7–Q0), when POL is HIGH, or loads the compliment of the inputs when POL is LOW. The CLEAR operation resets the output register to all LOWs. The PRESET operation presets the output register to all HIGHs. The HOLD operation holds the previous value regardless of clock transitions. CLEAR overrides PRESET, PRESET overrides LOAD, and LOAD overrides HOLD.

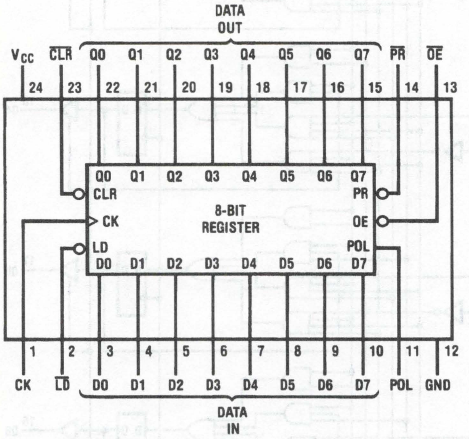
The output register (Q7–Q0) is enabled when $\overline{OE}$ is LOW and disabled (HI–Z) when $\overline{OE}$ is HIGH. The output drivers will sink 24 mA required for many bus interface standards.

Features

- Octal Register for general purpose interfacing applications
- 8 bits match byte boundaries
- Low current PNP inputs reduce loading
- Bus-structured pinout
- TRI-STATE® outputs
- 24-pin SKINNYDIP saves space

Connection Diagram

Top View


DATA OUT
VCC 24
CLR 23
Q0 22
Q1 21
Q2 20
Q3 19
Q4 18
Q5 17
Q6 16
Q7 15
PR 14
OE 13
8-BIT REGISTER
CLR
CK
LD
PR
OE
POL
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
D0 D1 D2 D3 D4 D5 D6 D7
1 CK
2 LD
3 D0
4 D1
5 D2
6 D3
7 D4
8 D5
9 D6
10 D7
11 POL
12 GND
DATA IN

TL/L/10229–1

Order Number DM54LS380AJ, DM74LS380AJ, DM74LS380AN or DM74LS380AV
See NS Package Number J24F, N24C or V28A

Function Table

$\overline{OC}$	CLK	$\overline{CLR}$	$\overline{PR}$	$\overline{LD}$	POL	D7–D0	Q7–Q0	Operation
H	X	X	X	X	X	X	Z	HI–Z
L	↑	L	X	X	X	X	L	CLEAR
L	↑	H	L	X	X	X	H	PRESET
L	↑	H	H	H	X	X	Q	HOLD
L	↑	H	H	L	H	D	D	LOAD true
L	↑	H	H	L	L	D	$\overline{D}$	LOAD comp

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} Supply Voltage	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
ESD Tolerance	>1000V

Czap = 100 pF
Rzap = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP 5-028

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55	25		0	25	75	°C
T_C	Operating Case Temperature			125				°C

Electrical Characteristics Series 24A Over Recommended Operating Temperature Range

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	(Note 2)			2			V
V_{IL}	Low Level Input Voltage	(Note 2)					0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, II = −18 mA				−0.8	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = −2 mA	MIL	2.4	2.9		V
			I_{OH} = −3.2 mA	COM				
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 12 mA	MIL		0.3	0.5	V
			I_{OL} = 24 mA	COM				
I_{OZH}	Off-State Output Current (Note 3)	V_{CC} = Max V_{IL} = 0.8V V_{IH} = 2V	V_O = 2.4V				100	μA
I_{OZL}			V_O = 0.4V				−100	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V					1	mA
I_{IH}	High Level Input Current (Note 3)	V_{CC} = Max, V_I = 2.4V					25	μA
I_{IL}	Low Level Input Current (Note 3)	V_{CC} = Max, V_I = 0.4V				−0.04	−0.25	mA
I_{OS}	Output Short-Circuit Current	V_{CC} = 5V	V_O = 0V (Note 4)		−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max				135	180	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

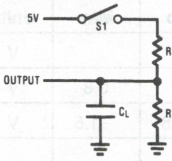
Note 3: I/O leakage as the worst case of IOZX or IIX, e.g., I_{IL} and IOZL.

Note 4: During I_{OS} measurment, only one output at a time should be grounded. Permanent damage otherwise may result.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter		Test Conditions	Military			Commercial			Units
				Min	Typ	Max	Min	Typ	Max	
t_S	Set-Up Time from Input			40	20		30	20		ns
t_W	Width of Clock	High		20	7		15	7		ns
		Low		35	15		25	15		ns
t_H	Hold Time			0	−15		0	−15		ns
T_{clk}	Clock to Output		$C_L = 50$ pF		10	25		10	15	ns
T_{pzx}	Output Enable Delay		$C_L = 50$ pF		19	35		19	30	ns
T_{pxz}	Output Disable Delay		$C_L = 5$ pF		15	35		15	30	ns
f_{max}	Maximum Frequency			15.3	32		22.2	32		MHz

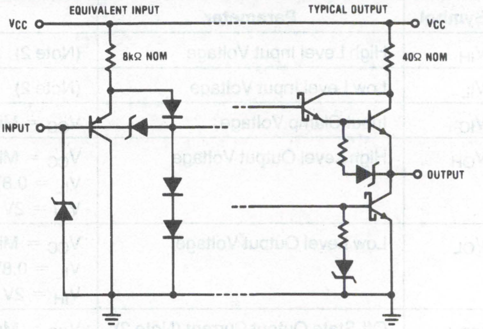
Test Load


5V
S1
R1
OUTPUT
CL
R2

MIL	COM'L
R1 = 390	R1 = 200
R2 = 750	R2 = 390

TL/L/10229-2

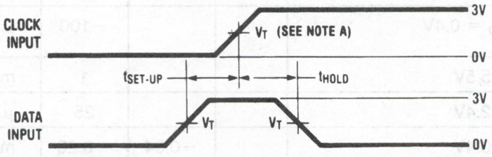
Schematic of Inputs and Outputs


EQUIVALENT INPUT
TYPICAL OUTPUT
VCC
VCC
8kΩ NOM
40Ω NOM
INPUT
OUTPUT

TL/L/10229-3

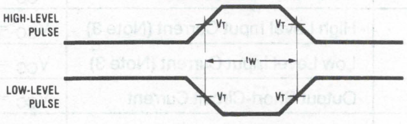
Test Waveforms

Set-Up and Hold


CLOCK INPUT
3V
VT (SEE NOTE A)
0V
tSET-UP
tHOLD
DATA INPUT
3V
VT
VT
0V

TL/L/10229-4

Pulse Width


HIGH-LEVEL PULSE
VT
VT
tW
LOW-LEVEL PULSE
VT
VT

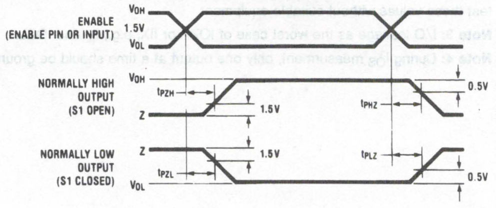
TL/L/10229-5

Note A: $V_T = 1.5V$.

Note B: C_L includes probe and jig capacitance.

Note C: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

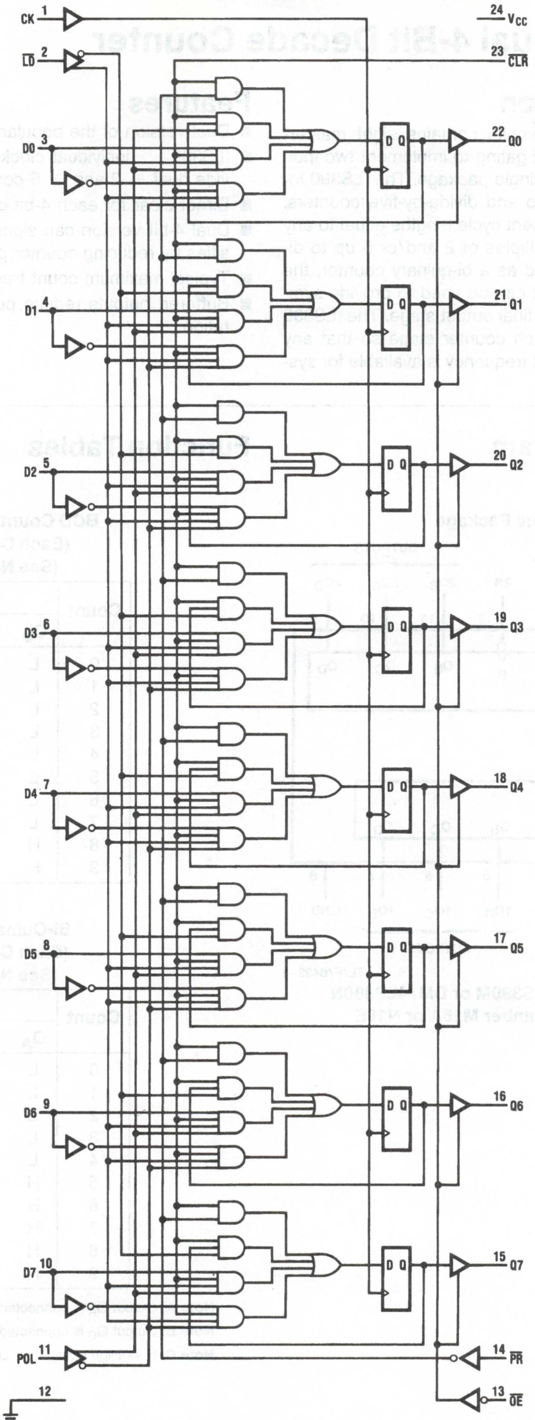
Enable and Disable


ENABLE (ENABLE PIN OR INPUT)
VOH
1.5V
VOL
NORMALLY HIGH OUTPUT (S1 OPEN)
VOH
tPZH
1.5V
tPHZ
0.5V
Z
NORMALLY LOW OUTPUT (S1 CLOSED)
Z
1.5V
tPLZ
tPZL
0.5V
VOL

TL/L/10229-6

Logic Diagram

Octal Register


CK 1
LD 2
D0 3
D1 4
D2 5
D3 6
D4 7
D5 8
D6 9
D7 10
POL 11
12
24 VCC
23 CLR
22 Q0
21 Q1
20 Q2
19 Q3
18 Q4
17 Q5
16 Q6
15 Q7
14 PR
13 OE
D Q

TL/L/10229-7

National Semiconductor

DM74LS390 Dual 4-Bit Decade Counter

General Description

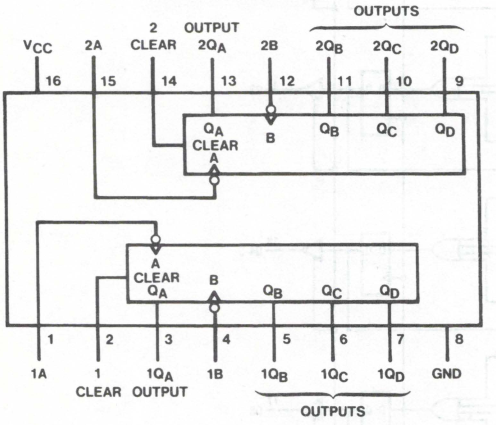
Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'LS390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The 'LS390 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Features

- Dual version of the popular 'LS90
- 'LS390 . . . individual clocks for A and B flip-flops provide dual ÷ 2 and ÷ 5 counters
- Direct clear for each 4-bit counter
- Dual 4-bit version can significantly improve system densities by reducing counter package count by 50%
- Typical maximum count frequency . . . 35 MHz
- Buffered outputs reduce possibility of collector commutation

Connection Diagram

Dual-In-Line Package



TL/F/6433–1

Order Number DM74LS390M or DM74LS390N
See NS Package Number M16A or N16E

Function Tables

BCD Count Sequence
(Each Counter)
(See Note A)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Bi-Quinary (5-2)
(Each Counter)
(See Note B)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Note A: Output Q_A is connected to input B for BCD count.

Note B: Output Q_D is connected to input A for Bi-quinary count.

Note C: H = High Level, L = Low Level.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Clear	7V
A or B	5.5V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74LS390			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 1)	A to Q_A	0		25	MHz
		B to Q_B	0		20	
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		20	MHz
		B to Q_B	0		15	
t_W	Pulse Width (Note 1)	A	20			ns
		B	25			
		Clear High	20			
t_{REL}	Clear Release Time (Notes 3 & 4)		25↓			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: The symbol (↓) indicates the falling edge of the clear pulse is used for reference.

Note 4: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Clear			0.1	mA
		V_{CC} = Max V_I = 5.5V	A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Clear			20	μA
			A			40	
			B			80	

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clear			−0.4	mA
			A			−1.6	
			B			−2.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM74	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			15	26	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

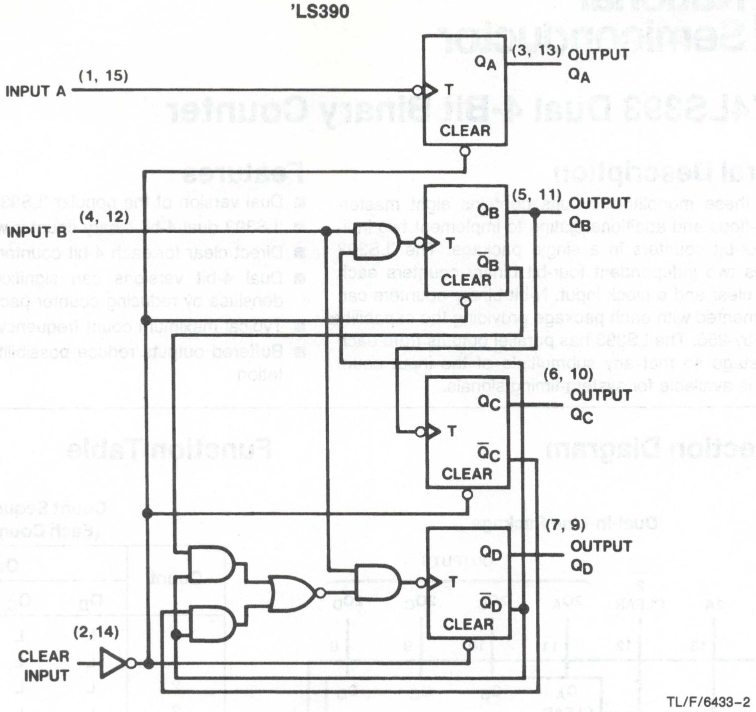
Note 3: I_{CC} is measured with all outputs open, both CLEAR inputs grounded following momentary connection to 4.5 and all other inputs grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	25		20		MHz
		B to Q_B	20		15		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		20		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_C		60		81	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_C		60		81	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		21		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		39		51	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		39		54	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		21		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		21		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		39		45	ns

Logic Diagram


'LS390
INPUT A
(1, 15)
T
CLEAR
QA
(3, 13)
OUTPUT QA
INPUT B
(4, 12)
QB
(5, 11)
OUTPUT QB
Q̄B
(6, 10)
OUTPUT QC
QC
Q̄C
(7, 9)
OUTPUT QD
QD
Q̄D
(2,14)
CLEAR INPUT
TL/F/6433-2

National Semiconductor

DM74LS393 Dual 4-Bit Binary Counter

General Description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'LS393 comprises two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The LS393 has parallel outputs from each counter stage so that any submultiple of the input count freqency is available for system-timing signals.

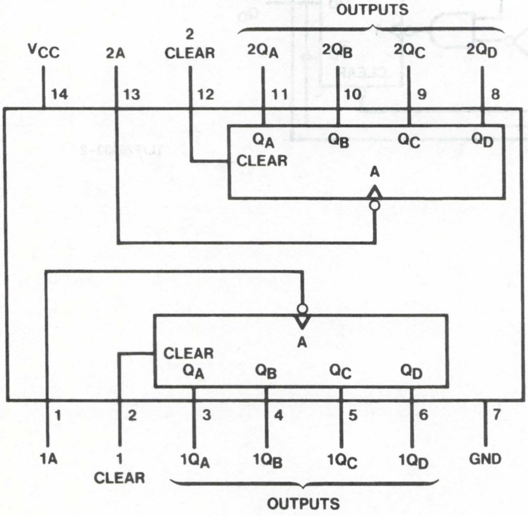
Features

- Dual version of the popular 'LS93
- 'LS393 dual 4-bit binary counter with individual clocks
- Direct clear for each 4-bit counter
- Dual 4-bit versions can significantly improve system densities by reducing counter package count by 50%
- Typical maximum count frequency 35 MHz
- Buffered outputs reduce possibility of collector commutation

---

Connection Diagram

Dual-In-Line Package



TL/F/6434-1

Order Number DM74LS393M or DM74LS393N
See NS Package Number M14A or N14A

Function Table

Count Sequence
(Each Counter)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 7V

Input Voltage

Clear 7V

A 5.5V

Operating Free Air Temperature Range

DM74LS 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74LS393 Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	MHz
f_{CLK}	Clock Frequency (Note 2)		0		20	MHz
t_W	Pulse Width (Note 7)	A	20			ns
		Clear High	20			
t_{REL}	Clear Release Time (Notes 3 & 7)		25↓			ns
T_A	Free Air Operating Temperature		0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Clear			0.1	mA
		V_{CC} = Max, V_I = 5.5V	A			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Clear			20	μA
			A			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clear			−0.4	mA
			A			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			15	26	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: The symbol (↓) indicates that the falling edge of the clear pulse is used for reference.

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

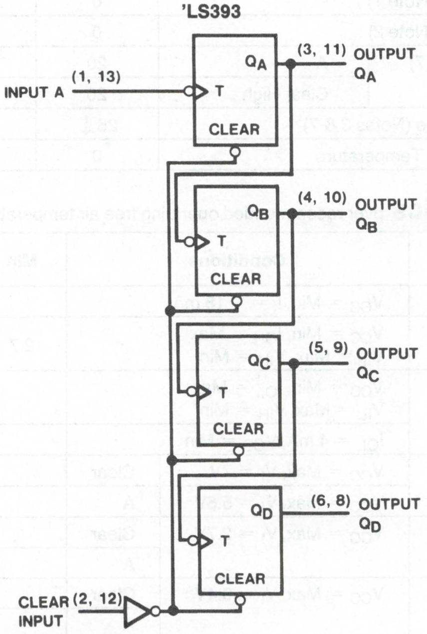
Note 6: I_{CC} is measured with all outputs open, both CLEAR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

Note 7: T_A = 25°C, and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ C_L = 15 pF Min	 Max	 C_L = 50 pF Min	 Max	Units
f_{MAX}	Maximum Clock Frequency	A to Q_A	25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		20		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		60		87	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		60		87	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		39		45	ns

Logic Diagram


'LS393
Q_A
(3, 11) OUTPUT Q_A
(1, 13)
INPUT A
T
CLEAR
Q_B
(4, 10) OUTPUT Q_B
T
CLEAR
Q_C
(5, 9) OUTPUT Q_C
T
CLEAR
Q_D
(6, 8) OUTPUT Q_D
T
CLEAR
CLEAR INPUT (2, 12)

TL/F/6434-2

National Semiconductor

54LS395/DM74LS395
4-Bit Shift Register with TRI-STATE® Outputs

General Description

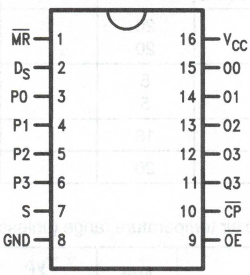
The LS395 is a 4-bit shift register with TRI-STATE outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset ($\overline{MR}$) input overrides the synchronous operations and clears the register. An active LOW Output Enable ($\overline{OE}$) input controls the TRI-STATE output buffers, but does not interfere with the other operations. The fourth stage also has a conventional output for linking purposes in multi-stage serial operations.

Features

- Shift right or parallel 4-bit register
- TRI-STATE outputs
- Input clamp diodes limit high speed termination effects
- Fully CMOS and TTL compatible

Connection Diagram

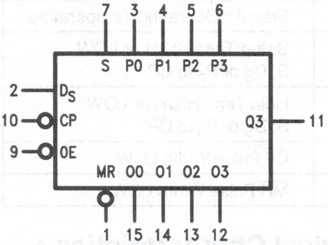
Dual-In-Line Package



TL/F/9833-1

Order Number 54LS395DMQB, 54LS395FMQB, 54LS395LMQB, DM74LS395WM or DM74LS395N
See NS Package Number E20A, J16A, M16B, N16E or W16A

Logic Symbol



TL/F/9833-2

V_{CC} = Pin 16
GND = Pin 8

Mode Select Table

Operating Mode	Inputs @ t_n					Outputs @ t_{n+1}			
	$\overline{MR}$	$\overline{CP}$	S	D_S	P_n	O0	O1	O2	O3
Asynchronous Reset	L	X	X	X	X	L	L	L	L
Shift, SET First Stage	H	‾_	L	H	X	H	$O0_n$	$O1_n$	$O2_n$
Shift, RESET First Stage	H	‾_	L	L	X	L	$O0_n$	$O1_n$	$O2_n$
Parallel Load	H	‾_	H	X	Pn	P0	P1	P2	P3

t_n, t_{n+1} = Time before and after CP HIGH-to-LOW transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS395			DM74LS395			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW S, D_S or P_n to CP	20 20			20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW S, D_S or P_n to $\overline{CP}$	5 5			5 5			ns
t_w (L)	$\overline{CP}$ Pulse Width LOW	18			18			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	20			20			ns

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current with Outputs OFF	V_{CC} = Max, $\overline{OE}$, D_S, S = 4.5V $\overline{CP}$ = ⎺╲⎽, P_n = GND				29	mA
	Supply Current with Outputs ON	V_{CC} = Max, D_S, S = 4.5V $\overline{OE}$, $\overline{CP}$, P_n = GND				25	mA
I_{OZH}	TRI-STATE Output Off Current HIGH	V_{CC} = V_{CCH} V_{OZH} = 2.7V				20	µA
I_{OZL}	TRI-STATE Output Off Current LOW	V_{CC} = V_{CCH} V_{OZL} = 0.4V				−20	µA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	54LS/DM74LS R_L = 2 kΩ, C_L = 15 pF Min	 Max	Units
f_{max}	Maximum Shift Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to O_n		35 25	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to O_n		35	ns
t_{PZH} t_{PZL}	Output Enable Time		20 20	ns
t_{PHZ} t_{PLZ}	Output Disable Time		17 23	ns

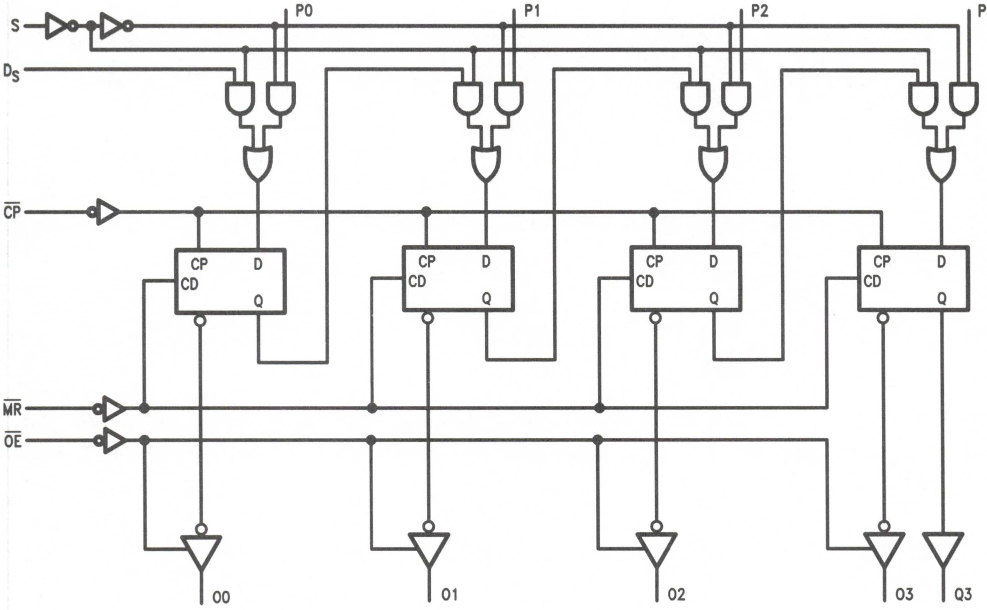
Functional Description

The LS395 contains four D-type edge-triggered flip-flops and auxiliary gating to select a D input either from a Parallel (P_n) input or from the preceding stage. When the Select input is HIGH, the P_n inputs are enabled. A LOW signal in the S input enables the serial inputs for shift-right operations, as indicated in the Truth Table.

State changes are initiated by HIGH-to-LOW transitions on the Clock Pulse ($\overline{CP}$) input. Signals on the P_n, D_S and S inputs can change when the Clock is in either state, provided that the recommended setup and hold times are observed. When the S input is LOW, a $\overline{CP}$ HIGH-LOW transition transfers data in O0 to O1, O1 to O2, and O2 to O3. A left-shift is accomplished by connecting the outputs back to the P_n inputs, but offset one place to the left, i.e., O3 to P2, O2 to P1, and O1 to P0, with P3 acting as the linking input from another package.

When the $\overline{OE}$ input is HIGH, the output buffers are disabled and the O0–O3 outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

Logic Diagram



TL/F/9833-3

National Semiconductor

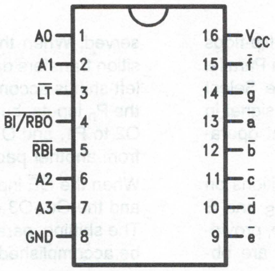
54LS447/DM74LS447 BCD to 7-Segment Decoder/Driver

General Description

The 'LS447 is the same as the 'LS247 except that the Output OFF Voltage, V_{OH} is specified as 7.0V rather than 15V, with the same I_{OH} limit of 250 μA. For all other information please refer to the 'LS247 data sheet.

Connection Diagram

Dual-In-Line Package


A0 1
A1 2
$\overline{LT}$ 3
$\overline{BI}/\overline{RBO}$ 4
$\overline{RBI}$ 5
A2 6
A3 7
GND 8
16 V_{CC}
15 $\overline{f}$
14 $\overline{g}$
13 $\overline{a}$
12 $\overline{b}$
11 $\overline{c}$
10 $\overline{d}$
9 $\overline{e}$

TL/F/10187-1

Order Number 54LS447FMQB, 54LS447FMQB, DM74LS447M or DM74LS447N
See NS Package Number J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS447			DM74LS447			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−50			−50	μA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.4			V
			DM74	2.4	3.4		
I_{OFF}	High Level Output Current	Segment Outputs, V_M = 7.0V				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V		−0.03		−0.4	mA
		BI/$\overline{\text{RBO}}$ Inputs		−0.09		−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−0.3		−2.0	mA
			DM74	−0.3		−2.0	
I_{CC}	Supply Current	V_{CC} = Max				13	mA

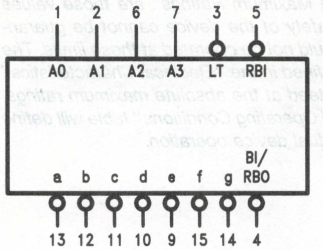
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load).

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay		100 100	ns

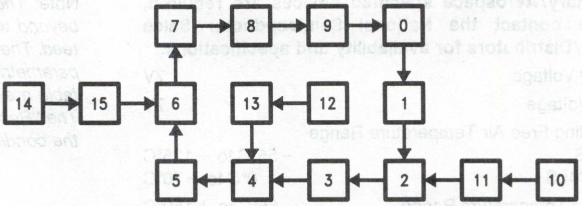
Logic Symbol


1
2
6
7
3
5
A0
A1
A2
A3
LT
RBI
BI/
RBO
a
b
c
d
e
f
g
13
12
11
10
9
15
14
4

TL/F/10187-2

V$_{CC}$ = Pin 16
GND = Pin 8

State Diagram


7
8
9
0
14
15
6
13
12
1
5
4
3
2
11
10

TL/F/10187-3

National Semiconductor

PRELIMINARY

DM54LS450/DM74LS450 16:1 Multiplexer

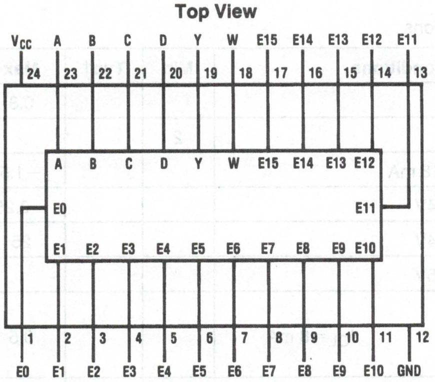
General Description

The 16:1 Mux selects one of sixteen inputs, E0 through E15, specified by four binary select inputs, A, B, C, and D. The true data is output on Y and the inverted data on W. Propagation delays are the same for both inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

Features/Benefits

- 24-pin SKINNYDIP saves space
- Similar to 74150 (Fat DIP)
- Low current PNP inputs reduce loading

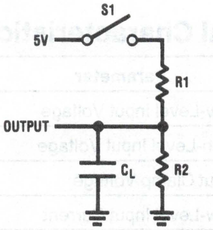
Connection Diagram


Top View
V_{CC}
A
B
C
D
Y
W
E15
E14
E13
E12
E11
24
23
22
21
20
19
18
17
16
15
14
13
A
B
C
D
Y
W
E15
E14
E13
E12
E0
E11
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
1
2
3
4
5
6
7
8
9
10
11
12
E0
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
GND

TL/L/8338-1

Order Number DM54LS450J, DM74LS450J, DM74LS450N or DM74LS450V
See NS Package Number J24F, N24C or V28A

Standard Test Load


S1
5V
R1
OUTPUT
C_L
R2

TL/L/8338-2

Function Table

Input Select				Output	
D	C	B	A	W	Y
L	L	L	L	$\overline{E0}$	E0
L	L	L	H	$\overline{E1}$	E1
L	L	H	L	$\overline{E2}$	E2
L	L	H	H	$\overline{E3}$	E3
L	H	L	L	$\overline{E4}$	E4
L	H	L	H	$\overline{E5}$	E5
L	H	H	L	$\overline{E6}$	E6
L	H	H	H	$\overline{E7}$	E7
H	L	L	L	$\overline{E8}$	E8
H	L	L	H	$\overline{E9}$	E9
H	L	H	L	$\overline{E10}$	E10
H	L	H	H	$\overline{E11}$	E11
H	H	L	L	$\overline{E12}$	E12
H	H	L	H	$\overline{E13}$	E13
H	H	H	L	$\overline{E14}$	E14
H	H	H	H	$\overline{E15}$	E15

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65° to +150°C

Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55		125*	0		75	°C

*Case temperature

Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions		Min	Typ†	Max	Units
V_{IL}	Low-Level Input Voltage					0.8	V
V_{IH}	High-Level Input Voltage			2			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN	I_I = −18 mA			−1.5	V
I_{IL}	Low-Level Input Current	V_{CC} = MAX	V_I = 0.4V			−0.25	mA
I_{IH}	High-Level Input Current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum Input Current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 8 mA			0.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = −2 mA COM I_{OH} = −3.2 mA	2.4			V
I_{OS}	Output Short-Circuit Current*	V_{CC} = 5.0V	V_O = 0V	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = MAX			60	100	mA

*No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

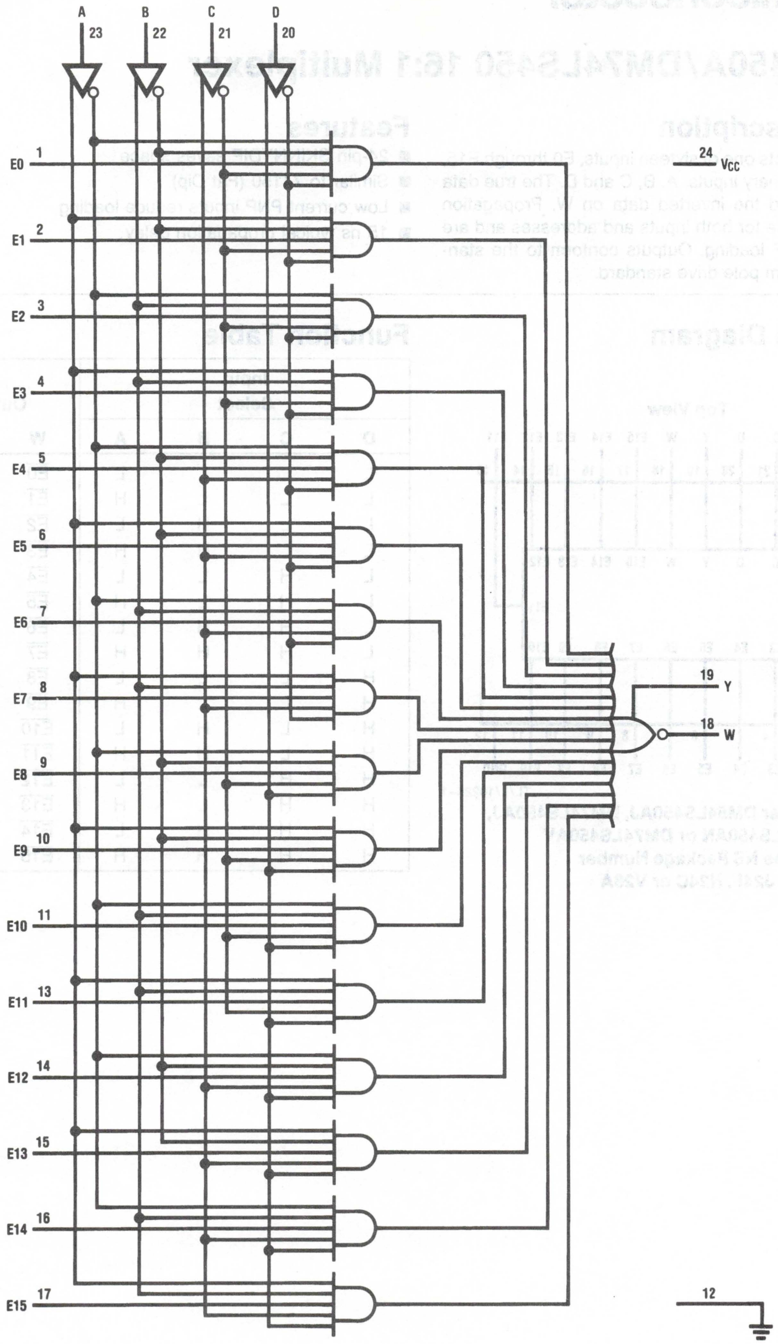
†All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions (See Test Load)	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PD}	Any Input to Y or W	C_L = 50 pF R_1 = 560Ω R_2 = 1.1kΩ		25	45		25	40	ns

Logic Diagram

16:1 Mux


A
23
B
22
C
21
D
20
E0
1
E1
2
E2
3
E3
4
E4
5
E5
6
E6
7
E7
8
E8
9
E9
10
E10
11
E11
13
E12
14
E13
15
E14
16
E15
17
24
V_{CC}
19
Y
18
W
12

TL/L/8338-3

National Semiconductor

DM54LS450A/DM74LS450 16:1 Multiplexer

General Description

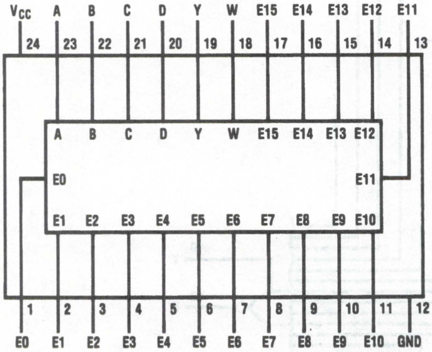
The 16:1 Mux selects one of sixteen inputs, E0 through E15, specified by four binary inputs, A, B, C and D. The true data is output on Y and the inverted data on W. Propagation delays are the same for both inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

Features

- 24-pin SKINNYDIP saves space
- Similar to 74150 (Fat Dip)
- Low current PNP inputs reduce loading
- 15 ns typical propagation delay

Connection Diagram

Top View



V_{CC}
A
B
C
D
Y
W
E15
E14
E13
E12
E11
24
23
22
21
20
19
18
17
16
15
14
13
A
B
C
D
Y
W
E15
E14
E13
E12
E0
E11
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
1
2
3
4
5
6
7
8
9
10
11
12
E0
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
GND

TL/L/10228-1

Order Number DM54LS450AJ, DM74LS450AJ, DM74LS450AN or DM74LS450AV
See NS Package Number J24F, N24C or V28A

Function Table

Input Select				Output	
D	C	B	A	W	Y
L	L	L	L	$\overline{E0}$	E0
L	L	L	H	$\overline{E1}$	E1
L	L	H	L	$\overline{E2}$	E2
L	L	H	H	$\overline{E3}$	E3
L	H	L	L	$\overline{E4}$	E4
L	H	L	H	$\overline{E5}$	E5
L	H	H	L	$\overline{E6}$	E6
L	H	H	H	$\overline{E7}$	E7
H	L	L	L	$\overline{E8}$	E8
H	L	L	H	$\overline{E9}$	E9
H	L	H	L	$\overline{E10}$	E10
H	L	H	H	$\overline{E11}$	E11
H	H	L	L	$\overline{E12}$	E12
H	H	L	H	$\overline{E13}$	E13
H	H	H	L	$\overline{E14}$	E14
H	H	H	H	$\overline{E15}$	E15

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	−0.5V to +7V (Note 2)
Input Voltage	−1.5V to +5.5V (Note 2)
Off-State Output Voltage	−1.5V to +5.5V (Note 2)
Input Current	−30.0 mA to +5.0 mA (Note 2)
Output Current (I_{OL})	+100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature with Power Applied	−65°C to +150°C
ESD Tolerance	2000V

$C_{ZAP} = 100$ pF
$R_{ZAP} = 1500\Omega$
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

Recommended Operating Conditons

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55		125	0		75	°C

Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (Note 3)						0.8	V
V_{IH}	High Level Input Voltage (Note 3)				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I = −18 mA					−1.5	V
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.25	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V					25	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V					1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 8 mA				0.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2 mA	MIL	2.4			V
			I_{OH} = −3.2 mA	COM				
I_{OS}	Output Short-Circuit Current (Note 4)	V_{CC} = 5V, V_O = 0V			−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open				60	100	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming operations according to the applicable specification.

Note 3: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

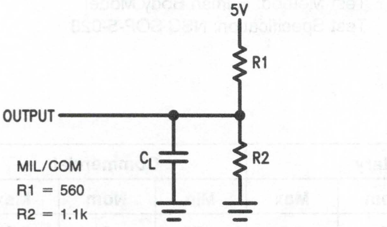
Note 4: To avoid invalid readings in other parameter tests, it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

2

Switching Characteristics Over Operating Conditions

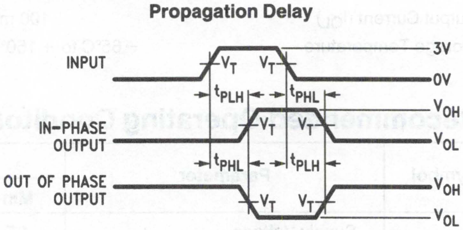
Symbol	Parameter	Test Conditions	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
T_{pd}	Input to Output	$C_L = 50$ pF			35			30	ns

Test Load


5V
R1
OUTPUT
C_L
R2
MIL/COM
R1 = 560
R2 = 1.1k

TL/L/10228-2

Test Waveform


Propagation Delay
INPUT
V_T
V_T
3V
0V
t_{PLH}
t_{PHL}
IN-PHASE OUTPUT
V_T
V_T
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
OUT OF PHASE OUTPUT
V_T
V_T
V_{OH}
V_{OL}

TL/L/10228-3

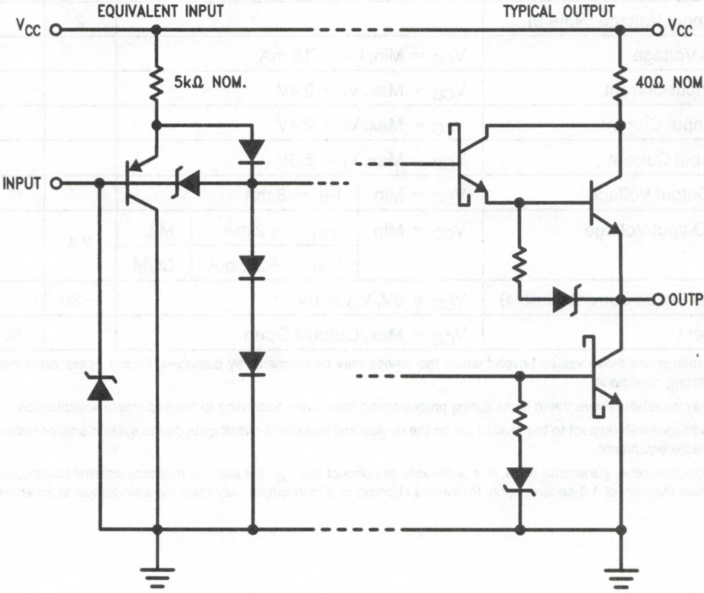
Notes:

$V_T = 1.5V$

C_L includes probe and jig capacitance.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

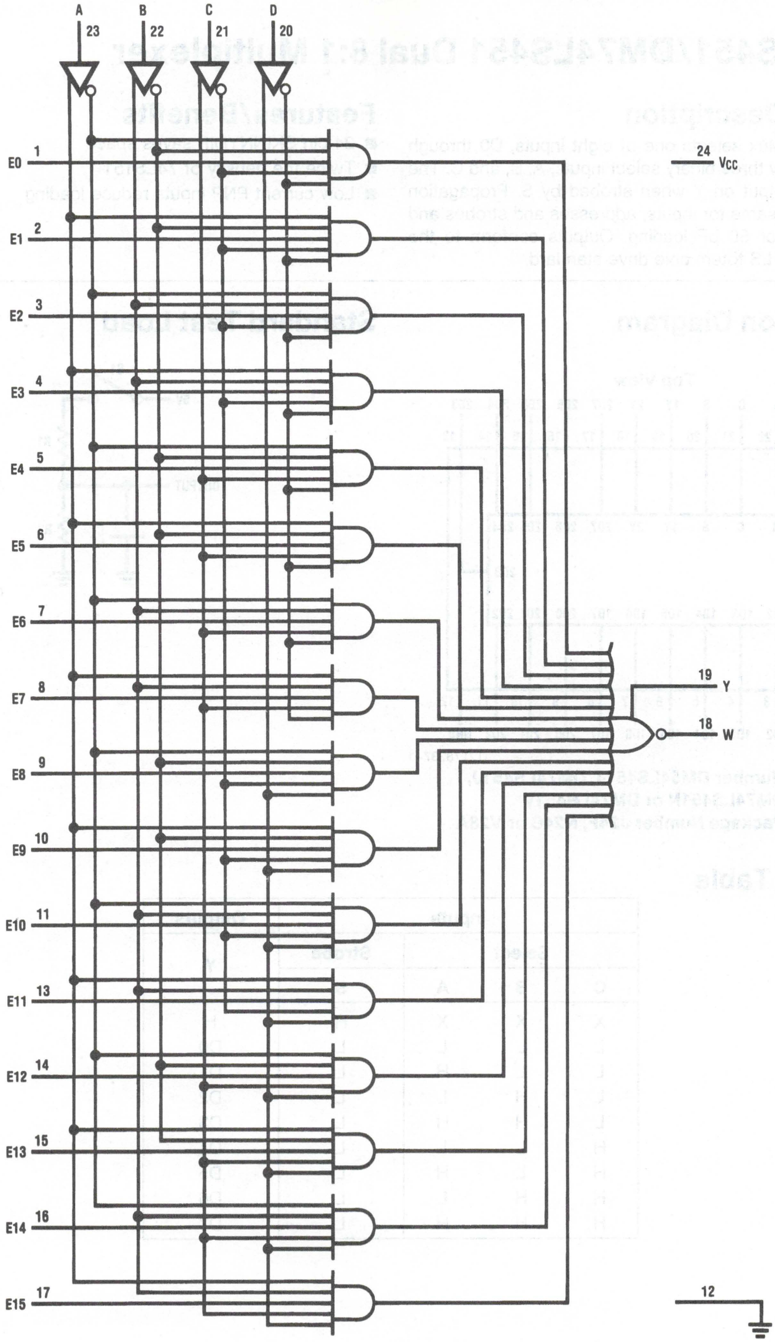
Schematic of Inputs and Outputs


EQUIVALENT INPUT
TYPICAL OUTPUT
V_{CC}
V_{CC}
5kΩ NOM.
40Ω NOM.
INPUT
OUTPUT

TL/L/10228-4

Logic Diagram

LS450A


A
23
B
22
C
21
D
20
E0
1
E1
2
E2
3
E3
4
E4
5
E5
6
E6
7
E7
8
E8
9
E9
10
E10
11
E11
13
E12
14
E13
15
E14
16
E15
17
24
V_{CC}
19
Y
18
W
12

TL/L/10228-5

National Semiconductor

DM54LS451/DM74LS451 Dual 8:1 Multiplexer

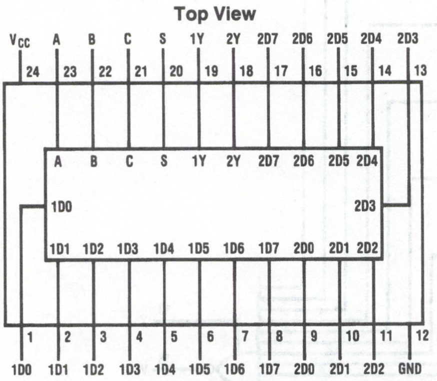
General Description

The Dual 8:1 Mux selects one of eight inputs, D0 through D7, specified by three binary select inputs, A, B, and C. The true data is output on Y when strobed by S. Propagation delays are the same for inputs, addresses and strobes and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

Features/Benefits

- 24-pin SKINNYDIP saves space
- Twice the density of 74LS151
- Low current PNP inputs reduce loading

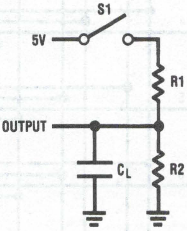
Connection Diagram


Top View
V_{CC} 24
A 23
B 22
C 21
S 20
1Y 19
2Y 18
2D7 17
2D6 16
2D5 15
2D4 14
2D3 13
A B C S 1Y 2Y 2D7 2D6 2D5 2D4
1D0
2D3
1D1 1D2 1D3 1D4 1D5 1D6 1D7 2D0 2D1 2D2
1 1D0
2 1D1
3 1D2
4 1D3
5 1D4
6 1D5
7 1D6
8 1D7
9 2D0
10 2D1
11 2D2
12 GND

TL/L/8337-1

Order Number DM54LS451J, DM74LS451J, DM74LS451N or DM74LS451V
See NS Package Number J24F, N24C or V28A

Standard Test Load


S1
5V
R1
OUTPUT
C_L
R2

TL/L/8337-2

Function Table

Inputs				Outputs
Select			Strobe	Y
C	B	A	S	
X	X	X	H	H
L	L	L	L	D0
L	L	H	L	D1
L	H	L	L	D2
L	H	H	L	D3
H	L	L	L	D4
H	L	H	L	D5
H	H	L	L	D6
H	H	H	L	D7

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65°C to +150°C

Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55		125*	0		75	°C

*Case Temperature

Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ†	Max	Units
V_{IL}	Low-Level Input Voltage				0.8	V
V_{IH}	High-Level Input Voltage		2			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN I_I = −18 mA			−1.5	V
I_{IL}	Low-Level Input Current	V_{CC} = MAX V_I = 0.4V			−0.25	mA
I_{IH}	High-Level Input Current	V_{CC} = MAX V_I = 2.4V			25	μA
I_I	Maximum Input Current	V_{CC} = MAX V_I = 5.5V			1	mA
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V I_{OL} = 8 mA			0.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V MIL I_{OH} = 2 mA COM I_{OH} = −3.2 mA	2.4			V
I_{OS}	Output Short-Circuit Current*	V_{CC} = 5.0V V_O = 0V	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = MAX		60	100	mA

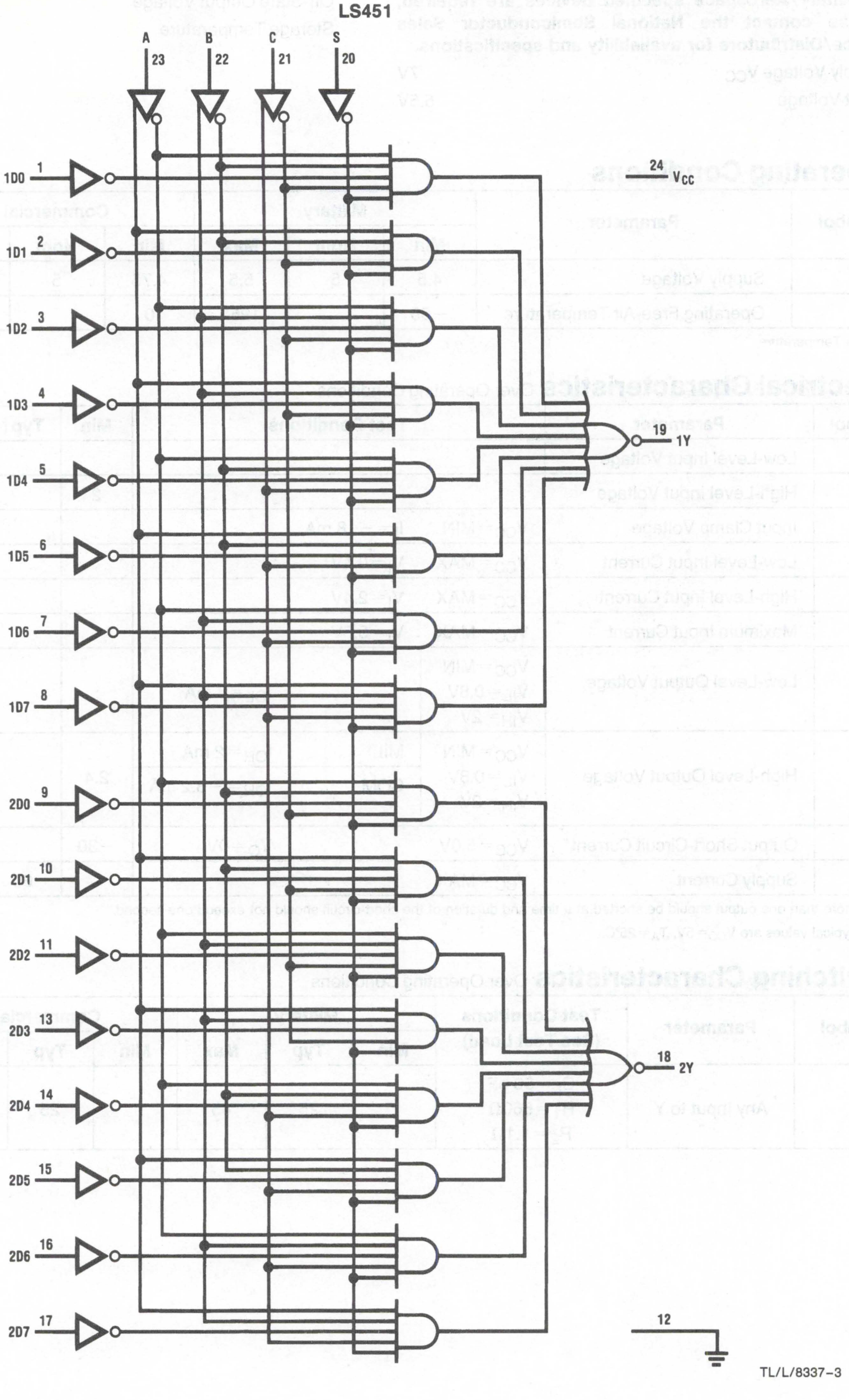
*No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† All typical values are V_{CC} = 5V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions (See Test Load)	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PD}	Any Input to Y	C_L = 50 pF R_1 = 560Ω R_2 = 1.1Ω		25	45		25	40	ns

Logic Diagram


LS451
A
23
B
22
C
21
S
20
1D0
1
1D1
2
1D2
3
1D3
4
1D4
5
1D5
6
1D6
7
1D7
8
2D0
9
2D1
10
2D2
11
2D3
13
2D4
14
2D5
15
2D6
16
2D7
17
24
V_{CC}
19
1Y
18
2Y
12

TL/L/8337-3

National Semiconductor

DM54LS451A/DM74LS451A Dual 8:1 Multiplexer

General Description

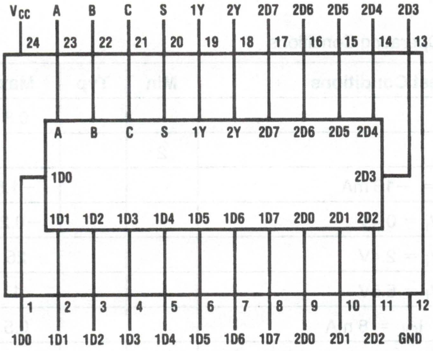
The Dual Mux selects one of eight inputs, D0 through D7, specified by three binary select inputs, A, B and C. The true data is output on Y when strobed by S. Propagation delays are the same for inputs, addresses and strobes and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

Features

- 24-pin SKINNYDIP saves space
- Twice the density of 74LS151
- Low current PNP inputs reduce loading
- 15 ns typical propagation delay

Connection Diagram

Top View


V$_{CC}$
A
B
C
S
1Y
2Y
2D7
2D6
2D5
2D4
2D3
24
23
22
21
20
19
18
17
16
15
14
13
1D0
1D1
1D2
1D3
1D4
1D5
1D6
1D7
2D0
2D1
2D2
GND
1
2
3
4
5
6
7
8
9
10
11
12

TL/L/10227-1

Order Number DM54LS451AJ, DM74LS451AJ, DM74LS451AN or DM74LS451AV
See NS Package Number J24F, N24C or V28A

Function Table

Inputs				Outputs
Select			Strobe	Y
C	B	A	S	
X	X	X	H	H
L	L	L	L	D0
L	L	H	L	D1
L	H	L	L	D2
L	H	H	L	D3
H	L	L	L	D4
H	L	H	L	D5
H	H	L	L	D6
H	H	H	L	D7

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	−0.5V to +7V (Note 2)
Input Voltage	−1.5V to +5.5V (Note 2)
Off-State Output Voltage	−1.5V to +5.5V (Note 2)
Input Current	−30.0 mA to +5.0 mA (Note 2)
Output Current (I_{OL})	+100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature with Power Applied	−65°C to +150°C
ESD Tolerance	2000V

C_{ZAP} = 100 pF
R_{ZAP} = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55		125	0		75	°C

Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (Note 3)						0.8	V
V_{IH}	High Level Input Voltage (Note 3)				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I = −18 mA					−1.5	V
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.25	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V					25	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V					1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 8 mA				0.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2 mA I_{OH} = −3.2 mA	MIL COM	2.4			V
I_{OS}	Output Short-Circuit Current (Note 4)	V_{CC} = 5V, V_O = 0V			−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open				60	100	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming operations according to the applicable specification.

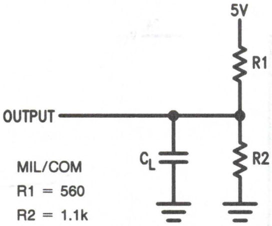
Note 3: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 4: To avoid invalid readings in other parameter tests, it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

Switching Characteristics Over Recommended Operating Conditions

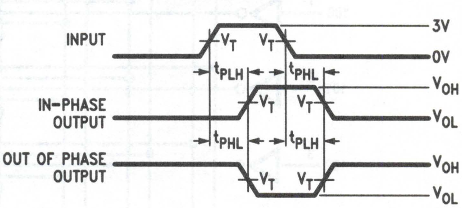
Symbol	Parameter	Test Conditions	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
T_{pd}	Input to Output	$C_L = 50$ pF		15	30		15	25	ns

Test Load


5V
R1
OUTPUT
C_L
R2
MIL/COM
R1 = 560
R2 = 1.1k

TL/L/10227-2

Test Waveform


Propagation Delay
INPUT
V_T
V_T
3V
0V
t_{PLH}
t_{PHL}
V_{OH}
IN-PHASE OUTPUT
V_{OL}
t_{PHL}
t_{PLH}
OUT OF PHASE OUTPUT
V_{OH}
V_{OL}

TL/L/10227-3

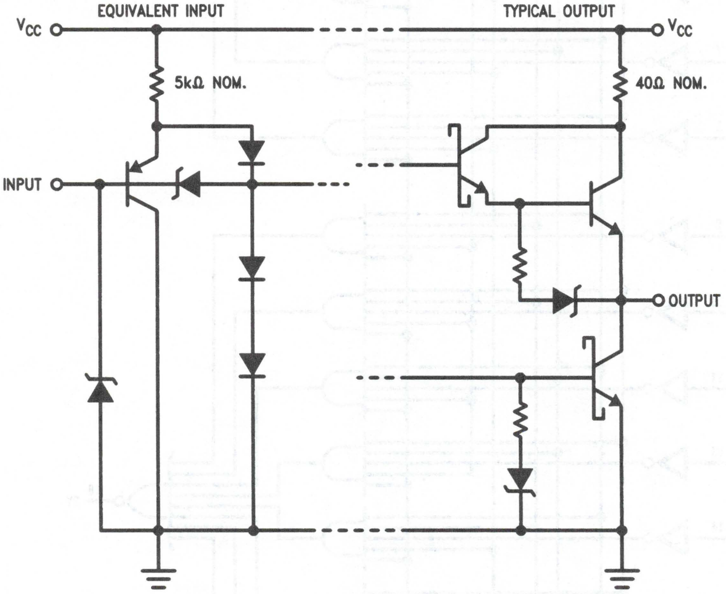
Notes:

$V_T = 1.5V$

C_L includes probe and jig capacitance.

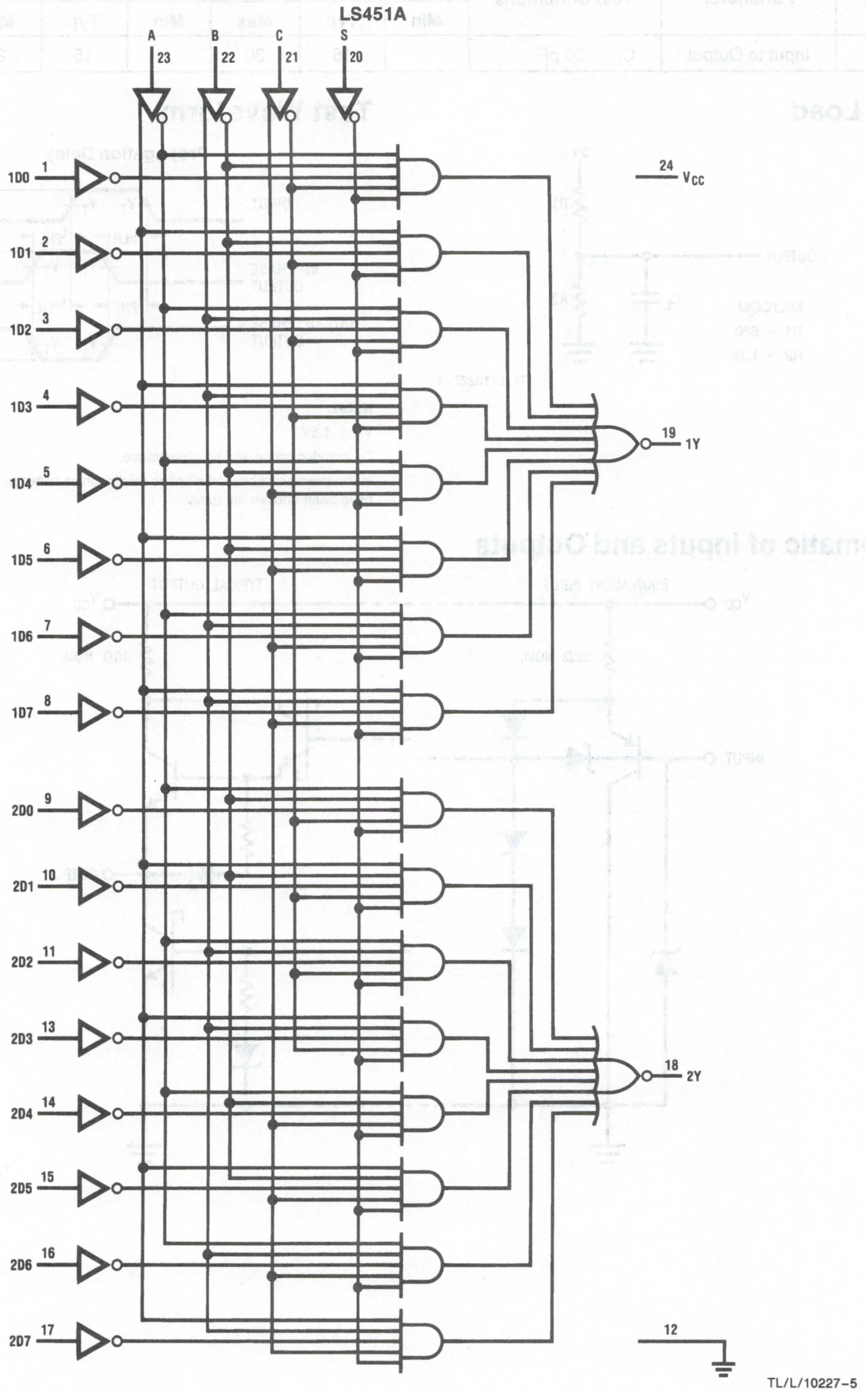
In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Schematic of Inputs and Outputs


EQUIVALENT INPUT
TYPICAL OUTPUT
V_{CC}
V_{CC}
5kΩ NOM.
40Ω NOM.
INPUT
OUTPUT

TL/L/10227-4

Logic Diagram


LS451A
A
23
B
22
C
21
S
20
24
V_{CC}
1D0 1
1D1 2
1D2 3
1D3 4
1D4 5
1D5 6
1D6 7
1D7 8
19
1Y
2D0 9
2D1 10
2D2 11
2D3 13
2D4 14
2D5 15
2D6 16
2D7 17
18
2Y
12

TL/L/10227-5

National Semiconductor

DM54LS453/DM74LS453
Quad 4:1 Multiplexer

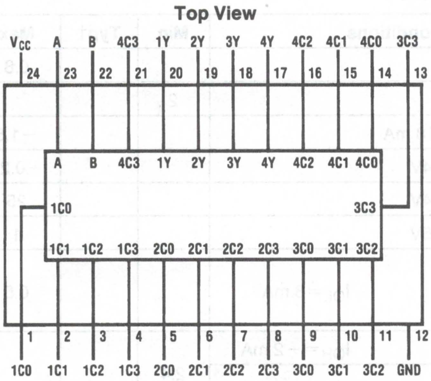
General Description

The quad 4:1 Mux selects one of four inputs, C0 through C3, specified by two binary select inputs, A and B. The true data is output on Y. Propagation delays are the same for inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

Features/Benefits

- 24-pin SKINNYDIP saves space
- Twice the density of 74LS153
- Low current PNP inputs reduce loading

Connection Diagram

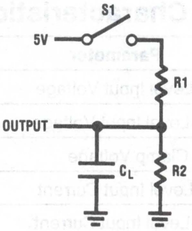


Top View
VCC
A
B
4C3
1Y
2Y
3Y
4Y
4C2
4C1
4C0
3C3
24
23
22
21
20
19
18
17
16
15
14
13
A
B
4C3
1Y
2Y
3Y
4Y
4C2
4C1
4C0
1C0
3C3
1C1
1C2
1C3
2C0
2C1
2C2
2C3
3C0
3C1
3C2
1
2
3
4
5
6
7
8
9
10
11
12
1C0
1C1
1C2
1C3
2C0
2C1
2C2
2C3
3C0
3C1
3C2
GND

TL/L/8336–1

Order Number DM54LS453J, DM74LS453J or DM74LS453N
See NS Package Number J24F or N24C

Standard Test Load



S1
5V
R1
OUTPUT
CL
R2

TL/L/8336–2

Function Table

INPUT SELECT		OUTPUTS Y
B	A	
L	L	C0
L	H	C1
H	L	C2
H	H	C3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−66° to +150°C

Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55		125*	0		75	°C

*Case temperature

Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ†	Max	Units
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IH}	High-Level Input Voltage				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL}	Low-Level Input Current	V_{CC} = MAX	V_I = 0.4V				−0.25	mA
I_{IH}	High-Level Input Current	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum Input Current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V		I_{OL} = 8 mA			0.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL	I_{OH} = −2 mA	2.4			V
			COM	I_{OH} = −3.2 mA				
I_{OS}	Output Short-Circuit Current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = MAX				60	100	mA

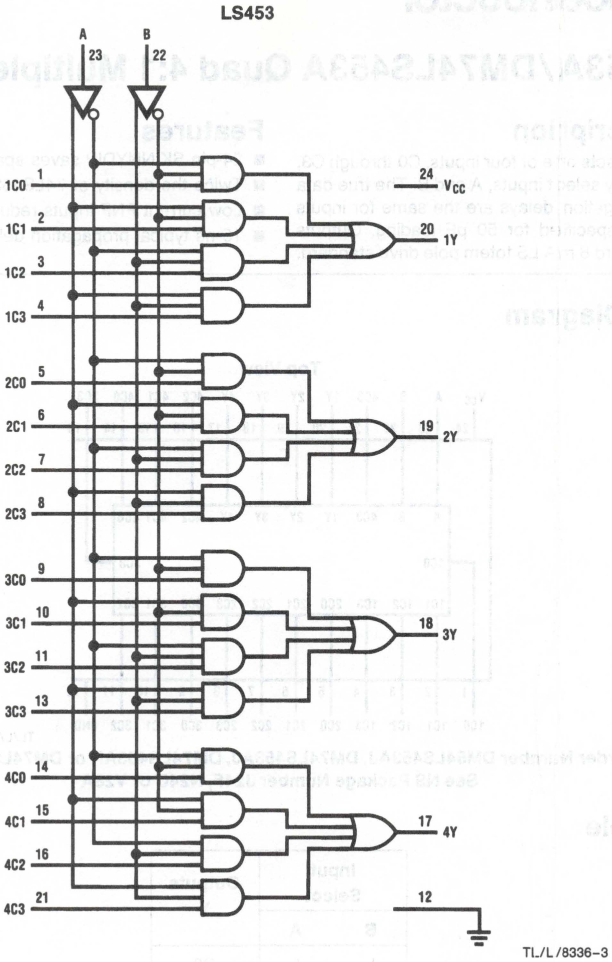
*No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

†All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions (See Test Load)	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PD}	Any Input to Y	C_L = 50 pF R_1 = 560Ω R_2 = 1.1 kΩ		25	45		25	40	ns

Logic Diagram


LS453
A
23
B
22
1
1C0
2
1C1
3
1C2
4
1C3
5
2C0
6
2C1
7
2C2
8
2C3
9
3C0
10
3C1
11
3C2
13
3C3
14
4C0
15
4C1
16
4C2
21
4C3
24
V_CC
20
1Y
19
2Y
18
3Y
17
4Y
12
TL/L/8336-3

National Semiconductor

DM54LS453A/DM74LS453A Quad 4:1 Multiplexer

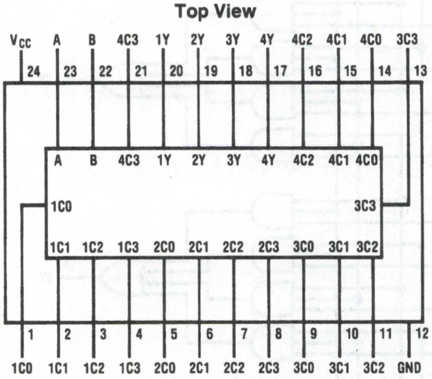
General Description

The quad 4:1 Mux selects one of four inputs, C0 through C3, specified by two binary select inputs, A and B. The true data is output on Y. Propagation delays are the same for inputs and addresses and specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem pole drive standard.

Features

- 24-pin SKINNYDIP saves space
- Twice the density of 74LS153
- Low current PNP inputs reduce loading
- 15 ns typical propagation delay

Connection Diagram


Top View
V_{CC}
A
B
4C3
1Y
2Y
3Y
4Y
4C2
4C1
4C0
3C3
24
23
22
21
20
19
18
17
16
15
14
13
A
B
4C3
1Y
2Y
3Y
4Y
4C2
4C1
4C0
1C0
3C3
1C1
1C2
1C3
2C0
2C1
2C2
2C3
3C0
3C1
3C2
1
2
3
4
5
6
7
8
9
10
11
12
1C0
1C1
1C2
1C3
2C0
2C1
2C2
2C3
3C0
3C1
3C2
GND

TL/L/10226-1

Order Number DM54LS453AJ, DM74LS453AJ, DM74LS453AN or DM74LS453AV
See NS Package Number J24F, N24C or V28A

Function Table

Input Select		Outputs Y
B	A	
L	L	C0
L	H	C1
H	L	C2
H	H	C3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	−0.5V to +7V (Note 2)
Input Voltage	−1.5V to +5.5V (Note 2)
Off-State Output Voltage	−1.5V to +5.5V (Note 2)
Input Current	−30.0 mA to +5.0 mA (Note 2)
Output Current (I_{OL})	+100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature with Power Applied	−65°C to +150°C
ESD Tolerance	2000V

C_{ZAP} = 100 pF
R_{ZAP} = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP5-028

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55		125	0		75	°C

Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (Note 3)						0.8	V
V_{IH}	High Level Input Voltage (Note 3)				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I = −18 mA					−1.5	V
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.25	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V					25	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V					1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 8 mA				0.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2 mA	MIL	2.4			V
			I_{OH} = −3.2 mA	COM				
I_{OS}	Output Short-Circuit Current (Note 4)	V_{CC} = 5V, V_O = 0V			−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open				60	100	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming operations according to the applicable specification.

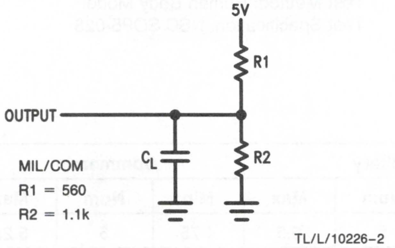
Note 3: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 4: To avoid invalid readings in other parameter tests, it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
T_{pd}	Input to Output	$C_L = 50$ pF		15	30		15	25	ns

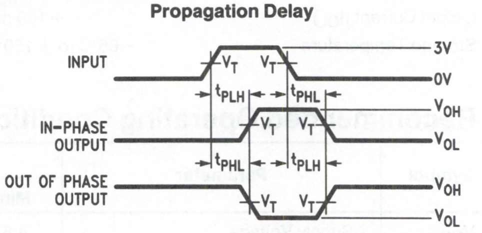
Test Load



5V
R1
OUTPUT
C_L
R2
MIL/COM
R1 = 560
R2 = 1.1k

TL/L/10226-2

Test Waveform



Propagation Delay
INPUT
V_T
V_T
3V
0V
t_{PLH}
t_{PHL}
IN-PHASE OUTPUT
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
OUT OF PHASE OUTPUT
V_{OH}
V_{OL}

TL/L/10226-3

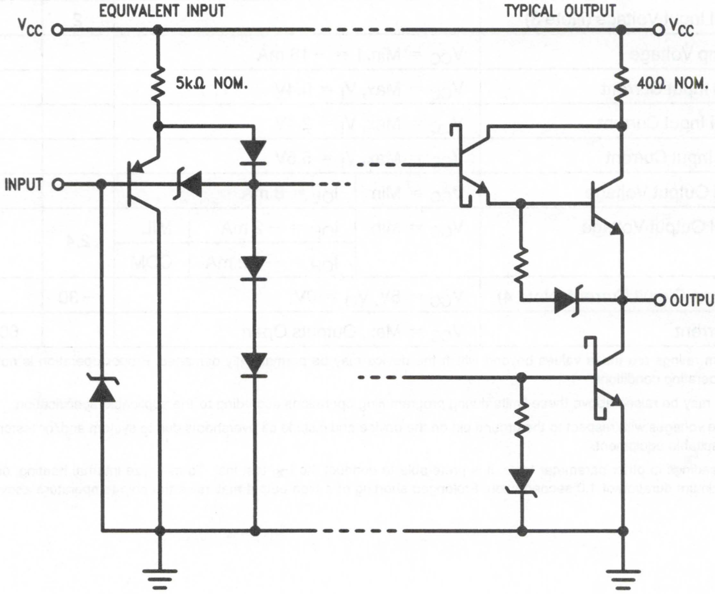
Notes:

$V_T = 1.5V$

C_L includes probe and jig capacitance.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

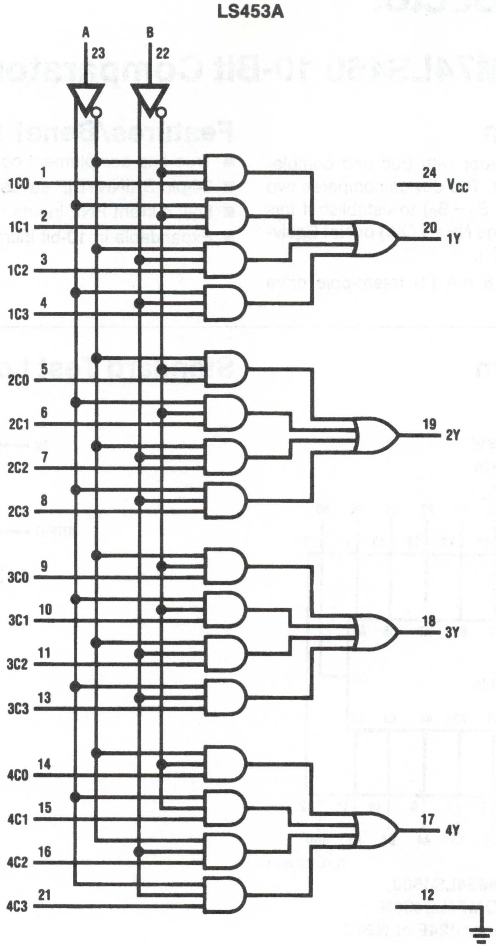
Schematic of Inputs and Outputs



EQUIVALENT INPUT
TYPICAL OUTPUT
V_{CC}
V_{CC}
5kΩ NOM.
40Ω NOM.
INPUT
OUTPUT

TL/L/10226-4

Logic Diagram


LS453A
A
23
B
22
1
1C0
2
1C1
3
1C2
4
1C3
5
2C0
6
2C1
7
2C2
8
2C3
9
3C0
10
3C1
11
3C2
13
3C3
14
4C0
15
4C1
16
4C2
21
4C3
24
V$_{CC}$
20
1Y
19
2Y
18
3Y
17
4Y
12

TL/L/10226-5

National Semiconductor

DM54LS460/DM74LS460 10-Bit Comparator

General Description

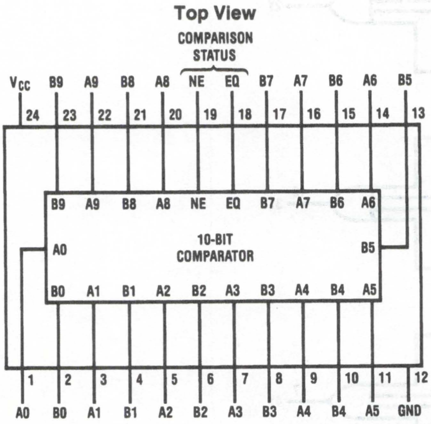
The 'LS460 is a 10-bit comparator with true and complement comparison status outputs. The device compares two 10-bit data strings ($A_g - A_0$ and $B_g - B_0$) to establish if this data is Equivalent (EQ = HIGH and NE = LOW) or Not Equivalent (EQ = LOW and NE = HIGH).

Outputs conform to the usual 8 mA LS totem-pole drive standard.

Features/Benefits

- True and complement comparison status outputs
- 24-pin SKINNYDIP saves space
- Low current PNP inputs reduce loading
- Expandable in 10-bit increments

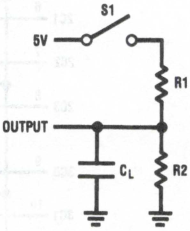
Connection Diagram


Top View
COMPARISON STATUS
V_CC
B9
A9
B8
A8
NE
EQ
B7
A7
B6
A6
B5
24
23
22
21
20
19
18
17
16
15
14
13
10-BIT COMPARATOR
A0
B0
A1
B1
A2
B2
A3
B3
A4
B4
A5
GND
1
2
3
4
5
6
7
8
9
10
11
12

TL/L/8335-1

Order Number DM54LS460J, DM74LS460J, or DM74LS460N
See NS Package Number J24F or N24C

Standard Test Load


S1
5V
R1
OUTPUT
C_L
R2

TL/L/8335-3

Function Table

A9 – A0	B9 – B0	EQ	NE	Operation
A	A	H	L	Equivalent (A = B)
B	B	H	L	
A	B	L	H	Not Equivalent (A ≠ B)

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65° to +150°C

Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55		125*	0		75	°C

*Case Temperature

Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ†	Max	Units
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IH}	High-Level Input Voltage				2			V
V_{IC}	Input Clamp Voltage	V_{CC}=MIN	I_I=−18 mA				−1.5	V
I_{IL}	Low-Level Input Current	V_{CC}=MAX	V_I=0.4V				−0.25	mA
I_{IH}	High-Level Input Current	V_{CC}=MAX	V_I=2.4V				25	μA
I_I	Maximum Input Current	V_{CC}=MAX	V_I=5.5V				1	mA
V_{OL}	Low-Level Output Voltage	V_{CC}=MIN V_{IL}=0.8V V_{IH}=2V		I_{OL}=8 mA			0.5	V
V_{OH}	High-Level Output Voltage	V_{CC}=MIN V_{IL}=0.8V V_{IH}=2V	MIL	I_{OH}=−2 mA	2.4			V
			COM	I_{OH}=−3.2 mA				
I_{OS}	Output Short-Circuit Current*	V_{CC}=5.0V		V_O=0V	−30		−130	mA
I_{CC}	Supply Current	V_{CC}=MAX				60	100	mA

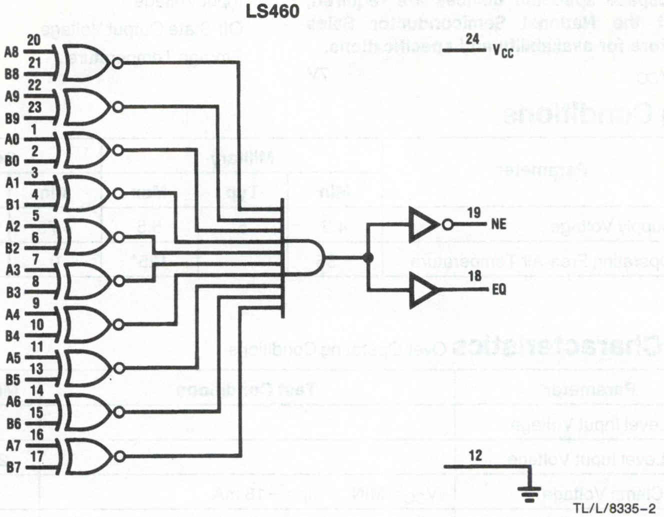
*No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

†All typical values are at V_{CC}=5V, T_A=25°C

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions (See Test Load)	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PD}	Any Input to EQ or NE	C_L=50 pF R_1=560Ω R_2=1.1 kΩ		25	45		25	40	ns

Logic Diagram


LS460
A8
20
B8
21
A9
22
B9
23
A0
1
B0
2
A1
3
B1
4
A2
5
B2
6
A3
7
B3
8
A4
9
B4
10
A5
11
B5
13
A6
14
B6
15
A7
16
B7
17
24
V_{CC}
19
NE
18
EQ
12

TL/L/8335-2

National Semiconductor

DM54LS460A/DM74LS460A 10-Bit Comparator

General Description

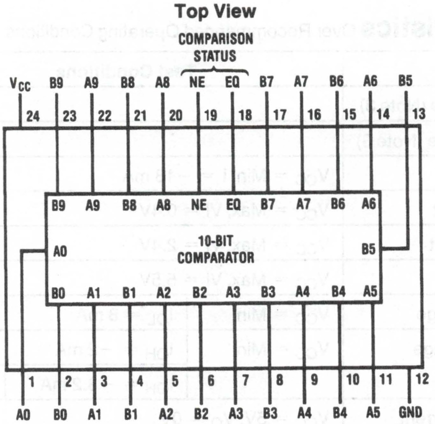
The 'LS460A is a 10-bit comparator with true complement comparison status outputs. The device compares two 10-bit data strings (Ag−A0 and Bg−B0) to establish if this data is Equivalent (EQ=HIGH and NE=LOW) or Not Equivalent (EQ=LOW and NE=HIGH).

Outputs conform to the usual 8 mA LS totem-pole drive standard.

Features

- True and complement comparison status outputs
- 24-pin SKINNYDIP saves space
- Low current PNP inputs reduce loading
- Expandable in 10-bit increments
- 15 ns typical propagation delay

Connection Diagram


Top View
COMPARISON STATUS
VCC
B9
A9
B8
A8
NE
EQ
B7
A7
B6
A6
B5
24
23
22
21
20
19
18
17
16
15
14
13
B9
A9
B8
A8
NE
EQ
B7
A7
B6
A6
A0
10-BIT COMPARATOR
B5
B0
A1
B1
A2
B2
A3
B3
A4
B4
A5
1
2
3
4
5
6
7
8
9
10
11
12
A0
B0
A1
B1
A2
B2
A3
B3
A4
B4
A5
GND

TL/L/10225-1

Order Number DM54LS460AJ, DM74LS460AJ, DM74LS460AN or DM74LS460AV
See NS Package Number J24F, N24C or V28A

Function Table

A9−A0	B9−B0	EQ	NE	Operation
A	A	H	L	} Equivalent (A=B)
B	B	H	L	
A	B	L	H	Not Equivalent (A≠B)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7V (Note 2)
Input Voltage	−1.5 to +5.5V (Note 2)
Off-State Output Voltage	−1.5 to +5.5V (Note 2)
Input Current	−30.0 mA to +5.0 mA (Note 2)
Output Current (I_{OL})	+100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature with Power Applied	−65°C to +150°C
ESD Tolerance	2000V

CZAP = 100 pF
RZAP = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55		125	0		75	°C

Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (Note 3)						0.8	V
V_{IH}	High Level Input Voltage (Note 3)				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I = −18 mA					−1.5	V
I_{IL}	Low Level Input Current	V_{CC} = Max, VI = 0.4V					−0.25	mA
I_{IH}	High Level Input Current	V_{CC} = Max, VI = 2.4V					25	μA
I_I	Maximum Input Current	V_{CC} = Max, VI = 5.5V					1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 8 mA				0.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2 mA	MIL	2.4			V
			I_{OH} = −3.2 mA	COM				
I_{OS}	Output Short-Circuit Current (Note 4)	V_{CC} = 5V, V_O = 0V			−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open				60	100	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming operations according to the applicable specification.

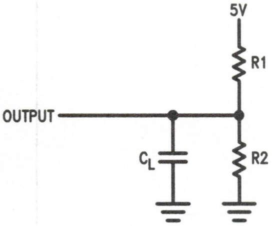
Note 3: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 4: To avoid invalid readings in other parameter tests, it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
T_{pd}	Input to Output	$C_L = 50$ pF			35			30	ns

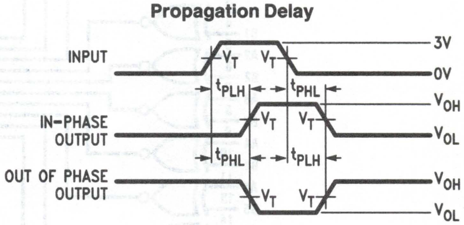
Test Load


5V
R1
OUTPUT
C_L
R2

MIL/COM
R1 = 560
R2 = 1.1k

TL/L/10225-2

Test Waveform


Propagation Delay
INPUT
IN-PHASE OUTPUT
OUT OF PHASE OUTPUT
V_T
t_{PLH}
t_{PHL}
3V
0V
V_{OH}
V_{OL}

TL/L/10225-3

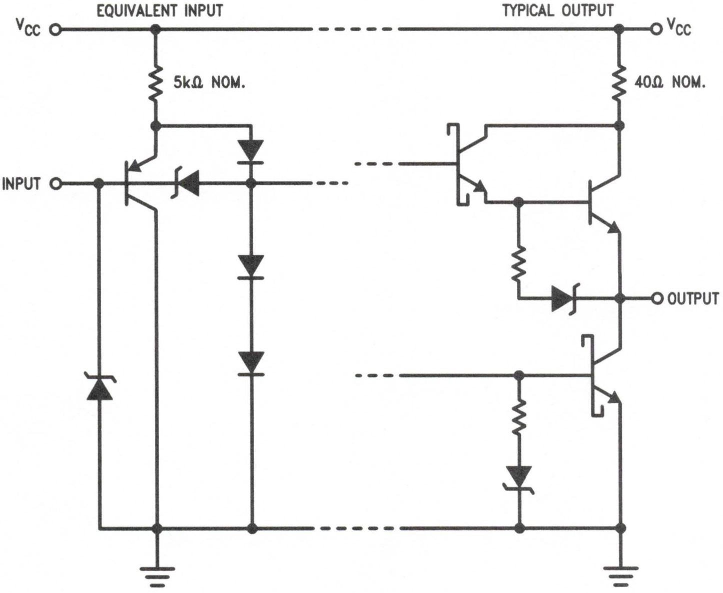
Notes:

$V_T = 1.5V$

C_L includes probe and jig capacitance.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

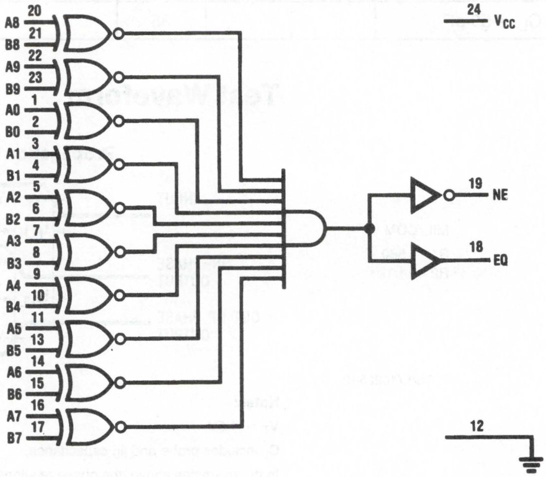
Schematic of Inputs and Outputs


EQUIVALENT INPUT
TYPICAL OUTPUT
V_{CC}
V_{CC}
5kΩ NOM.
40Ω NOM.
INPUT
OUTPUT

TL/L/10225-4

Logic Diagram

10-Bit Comparator


A8
20
B8
21
A9
22
B9
23
A0
1
B0
2
A1
3
B1
4
A2
5
B2
6
A3
7
B3
8
A4
9
B4
10
A5
11
B5
13
A6
14
B6
15
A7
16
B7
17
24
V_{CC}
19
NE
18
EQ
12

TL/L/10225-5

National Semiconductor

DM54LS461/DM74LS461 Octal Counter

General Description

The LS461 is an 8-bit synchronous counter with parallel load, clear, and hold capability. Two function select inputs (I_0, I_1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D_7–D_0) into the output register (Q_7–Q_0). The CLEAR operation resets the output register to all LOWs. The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CI}$ = LOW), otherwise the operation is a HOLD. The carry-out ($\overline{CO}$) is TRUE ($\overline{CO}$ = LOW) when the output register (Q_7–Q_0) is all HIGHs, otherwise FALSE ($\overline{CO}$ = HIGH).

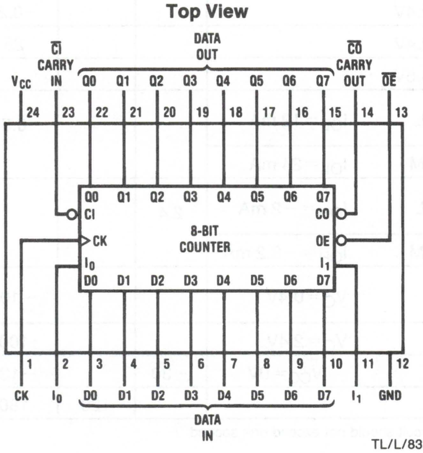
The output register (Q_7–Q_0) is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Two or more LS461 octal counters may be cascaded to provide larger counters. The operation codes were chosen such that when I_1 is HIGH, I_0 may be used to select between LOAD and INCREMENT as in a program counter (JUMP/INCREMENT).

Features/Benefits

- Octal counter for microprogram-counter, DMA controller and general purpose counting applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin Skinny Dip saves space
- TRI-STATE® outputs drive bus lines
- Low current PNP inputs reduce loading
- Expandable in 8-bit increments

Connection Diagram

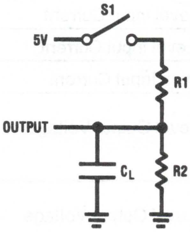


Top View
DATA OUT
$\overline{CI}$ CARRY IN
$\overline{CO}$ CARRY OUT
V_{CC}
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
$\overline{OE}$
24 23 22 21 20 19 18 17 16 15 14 13
CI CK I_0 D0 D1 D2 D3 D4 D5 D6 D7 I_1 OE CO
8-BIT COUNTER
1 2 3 4 5 6 7 8 9 10 11 12
CK I_0 D0 D1 D2 D3 D4 D5 D6 D7 I_1 GND
DATA IN

TL/L/8334-1

Order Number DM54LS461J, DM74LS461J or DM74LS461N
See NS Package Number J24F or N24C

Standard Test Load



S1
5V
R1
OUTPUT
C_L
R2

TL/L/8334-2

Function Table

$\overline{OE}$	CK	I1	I0	$\overline{CI}$	D7–D0	Q7–Q0	Operation
H	X	X	X	X	X	Z	HI-Z
L	↑	L	L	X	X	L	CLEAR
L	↑	L	H	X	X	Q	HOLD
L	↑	H	L	X	D	D	LOAD
L	↑	H	H	H	X	Q	HOLD
L	↑	H	H	L	X	Q plus 1	INCREMENT

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65°C to +150°C

Operating Conditions

Symbol	Parameter		Military Min	Military Typ	Military Max	Commercial Min	Commercial Typ	Commercial Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		−55		125*	0		75	°C
t_W	Width of Clock	Low	40			35			ns
		High	30			25			
t_{SU}	Set Up Time		60			50			ns
t_h	Hold Time		0	−15		0	−15		

*Case Temperature

Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ†	Max	Units
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IH}	High-Level Input Voltage				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN		I_I = −18 mA			−1.5	V
I_{IL}	Low-Level Input Current	V_{CC} = MAX		V_I = 0.4V			−0.25	mA
I_{IH}	High-Level Input Current	V_{CC} = MAX		V_I = 2.4V			25	µA
I_I	Maximum Input Current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL	I_{OL} = 12 mA			0.5	V
			COM	I_{OL} = 24 mA				
V_{OH}	High-Level Output Voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL	I_{OH} = −2 mA	2.4			V
			COM	I_{OH} = −3.2 mA				
I_{OZL}	Off-State Output Current	V_{CC} = MAX V_{IL} = 0.8V V_{IH} = 2V		V_O = 0.4V			−100	µA
I_{OZH}				V_O = 2.4V			100	µA
I_{OS}	Output Short-Circuit Current*	V_{CC} = 5.0V		V_{CC} = 0V	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = MAX				120	180	mA

*No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

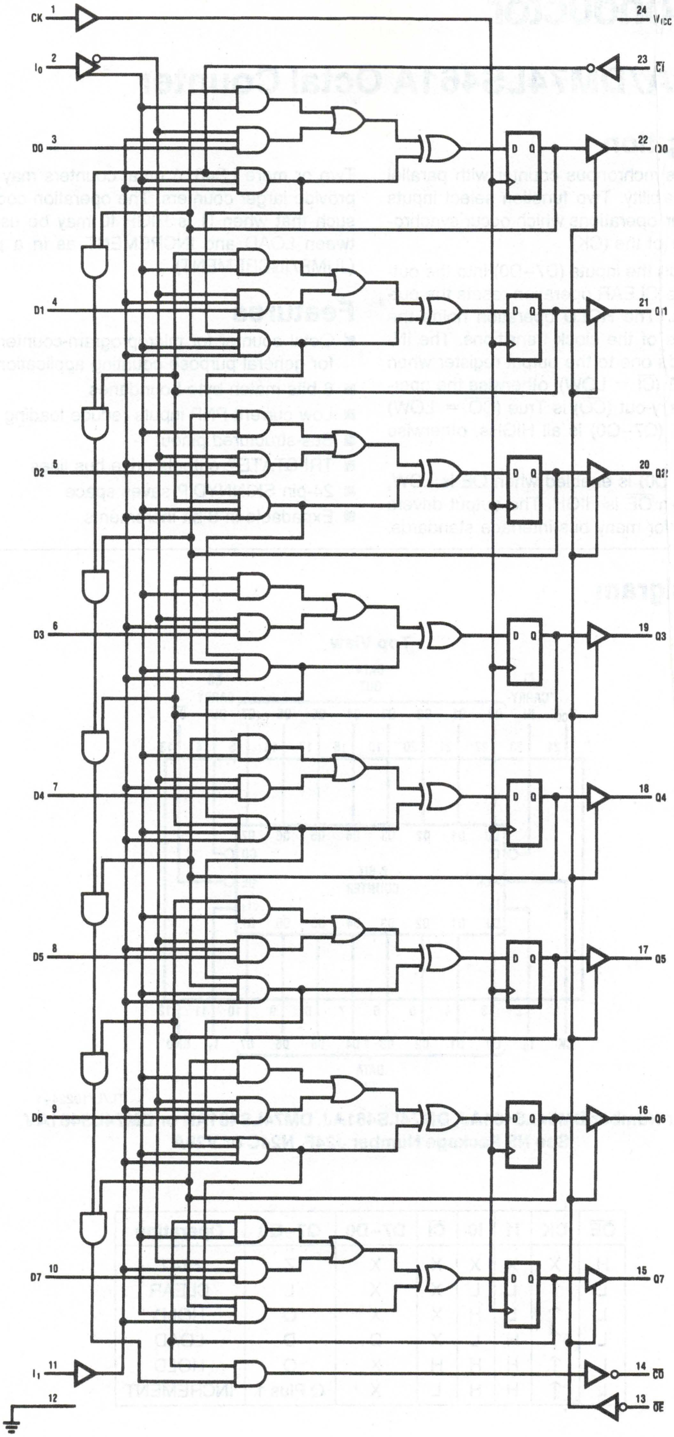
† All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions (See Test Load)	Military Min	Military Typ	Military Max	Commercial Min	Commercial Typ	Commercial Max	Units
f_{MAX}	Maximum Clock Frequency		10.5			12.5			MHz
t_{PD}	$\overline{CBI}$ to $\overline{CBO}$ Delay	C_L = 50 pF R_1 = 200 Ω R_2 = 390 Ω		35	60		35	50	ns
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PD}	Clock to $\overline{CO}$			55	95		55	80	ns
t_{PZX}	Output Enable Delay			35	55		35	45	ns
t_{PXZ}	Output Disable Delay			35	55		35	45	ns

Logic Diagram

LS461


CK 1
I_0 2
D0 3
D1 4
D2 5
D3 6
D4 7
D5 8
D6 9
D7 10
I_1 11
12
24 V_{CC}
23 $\overline{CI}$
22 Q0
21 Q1
20 Q2
19 Q3
18 Q4
17 Q5
16 Q6
15 Q7
14 $\overline{CO}$
13 $\overline{OE}$
D Q

TL/L/8334-3

National Semiconductor

DM54LS461A/DM74LS461A Octal Counter

General Description

The LS461A is an 8-bit synchronous counter with parallel load, clear and hold capability. Two function select inputs (I0, I1) provide one of four operations which occur synchronously on the rising edge of the (CK).

The LOAD operation loads the inputs (D7–D0) into the output register (Q7–Q0). The CLEAR operation resets the output register to all LOWs. The HOLD operation holds the previous value regardless of the clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CI}$ = LOW), otherwise the operation is a HOLD. The carry-out ($\overline{CO}$) is True ($\overline{CO}$ = LOW) when the output register (Q7–Q0) is all HIGHs, otherwise FALSE ($\overline{CO}$ = HIGH).

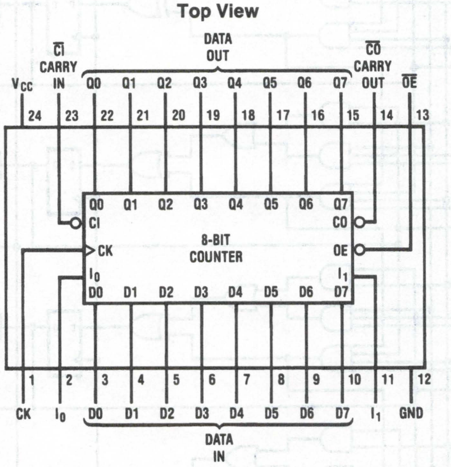
The output register (Q7–Q0) is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink 24 mA required for many bus interface standards.

Two or more LS461A octal counters may be cascaded to provide larger counters. The operation codes were chosen such that when I1 is HIGH I0 may be used to select between LOAD and INCREMENT as in a program counter (JUMP/INCREMENT).

Features

- Octal counter for microprogram-counter, DMA controller for general purpose counting applications
- 8 bits match byte boundaries
- Low current PNP inputs reduce loading
- Bus-structured pinout
- TRI-STATE® outputs drive bus lines
- 24-pin SKINNYDIP saves space
- Expadable in 8-bit increments

Connection Diagram


Top View
DATA OUT
$\overline{CI}$ CARRY IN
$\overline{CO}$ CARRY OUT
V_{CC}
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
$\overline{OE}$
24
23
22
21
20
19
18
17
16
15
14
13
CI
CK
I_0
D0
D1
D2
D3
D4
D5
D6
D7
CO
OE
I_1
8-BIT COUNTER
1
2
3
4
5
6
7
8
9
10
11
12
CK
I_0
I_1
GND
DATA IN

TL/L/10224-1

Order Number DM54LS461AJ, DM74LS461AJ, DM74LS461AN or DM74LS461AV
See NS Package Number J24F, N24C or V28A

Function Table

$\overline{OE}$	CK	I1	I0	$\overline{CI}$	D7–D0	Q7–Q0	Operation
H	X	X	X	X	X	Z	HI-Z
L	↑	L	L	X	X	L	CLEAR
L	↑	L	H	X	X	Q	HOLD
L	↑	H	L	X	D	D	LOAD
L	↑	H	H	H	X	Q	HOLD
L	↑	H	H	L	X	Q Plus 1	INCREMENT

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} Supply Voltage	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
ESD Tolerance	>1000V

Czap = 100 pF
Rzap = 150Ω
Test Method: Human Body Model
Test Specification: NSC SOP 5-028

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55	25		0	25	75	°C
T_C	Operating Case Temperature			125				°C

Electrical Characteristics Series 24A Over Recommended Operating Temperature Range

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	(Note 2)			2			V
V_{IL}	Low Level Input Voltage	(Note 2)					0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, II = −18 mA				−0.8	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = −2 mA	MIL	2.4	2.9		V
			I_{OH} = −3.2 mA	COM				
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 12 mA	MIL		0.3	0.5	V
			I_{OL} = 24 mA	COM				
I_{OZH}	Off-State Output Current (Note 3)	V_{CC} = Max V_{IL} = 0.8V V_{IH} = 2V	V_O = 2.4V				100	µA
I_{OZL}			V_O = 0.4V				−100	µA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V					1	mA
I_{IH}	High Level Input Current (Note 3)	V_{CC} = Max, V_I = 2.4V					25	µA
I_{IL}	Low Level Input Current (Note 3)	V_{CC} = Max, V_I = 0.4V				−0.04	−0.25	mA
I_{OS}	Output Short-Circuit Current	V_{CC} = 5V	V_O = 0V (Note 4)		−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max				135	180	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

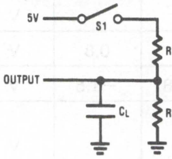
Note 3: I/O leakage as the worst case of IOZX or IIX, e.g., I_{IL} and IOZL.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage otherwise may result.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter		Test Conditions	Military			Commercial			Units
				Min	Typ	Max	Min	Typ	Max	
t_S	Set-Up Time from Input			40	20		30	20		ns
t_W	Width of Clock	High		20	7		15	7		ns
		Low		35	15		25	15		ns
T_{pd}	$\overline{CBI}$ to $\overline{CBO}$ Delay		C_L = 50 pF		23	35		23	30	ns
T_{clk}	Clock to Output		C_L = 50 pF		10	25		10	15	ns
T_{pzx}	Output Enable Delay		C_L = 50 pF		19	35		19	30	ns
T_{pzx}	Output Disable Delay		C_L = 5 pF		15	35		15	30	ns
t_H	Hold Time			0	−15		0	−15		ns
f_{max}	Maximum Frequency			15.3	32		22.2	32		MHz

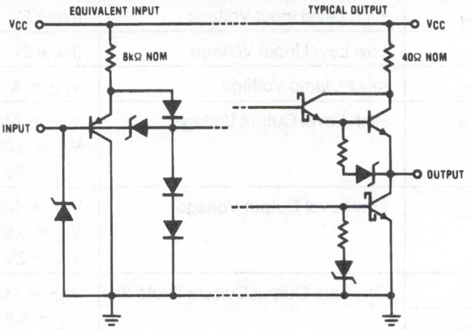
Test Load


5V
S1
R1
OUTPUT
CL
R2

	MIL	COM'L
R1	= 390	= 200
R2	= 750	= 390

TL/L/10224-2

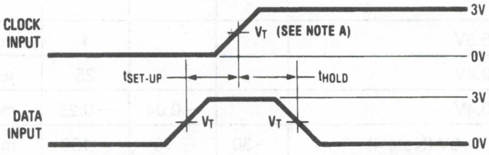
Schematic of Inputs and Outputs


EQUIVALENT INPUT
TYPICAL OUTPUT
VCC
VCC
8kΩ NOM
40Ω NOM
INPUT
OUTPUT

TL/L/10224-3

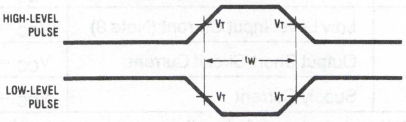
Test Waveforms

Set-Up and Hold


CLOCK INPUT
3V
VT (SEE NOTE A)
0V
tSET-UP
tHOLD
DATA INPUT
VT
VT
3V
0V

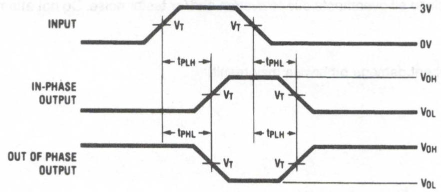
TL/L/10224-4

Pulse Width


HIGH-LEVEL PULSE
VT
VT
tW
LOW-LEVEL PULSE
VT
VT

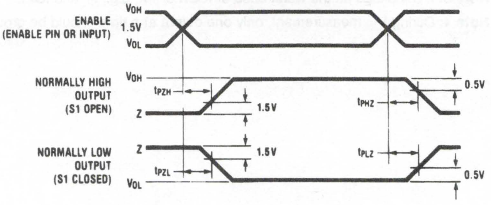
TL/L/10224-6

Propagation Delay


INPUT
VT
VT
3V
0V
tPLH
tPHL
IN-PHASE OUTPUT
VT
VT
VOH
VOL
tPHL
tPLH
OUT OF PHASE OUTPUT
VT
VT
VOH
VOL

TL/L/10224-5

Enable and Disable


ENABLE (ENABLE PIN OR INPUT)
VOH
1.5V
VOL
NORMALLY HIGH OUTPUT (S1 OPEN)
VOH
tPZH
1.5V
Z
tPHZ
0.5V
NORMALLY LOW OUTPUT (S1 CLOSED)
Z
1.5V
tPZL
VOL
tPLZ
0.5V

TL/L/10224-7

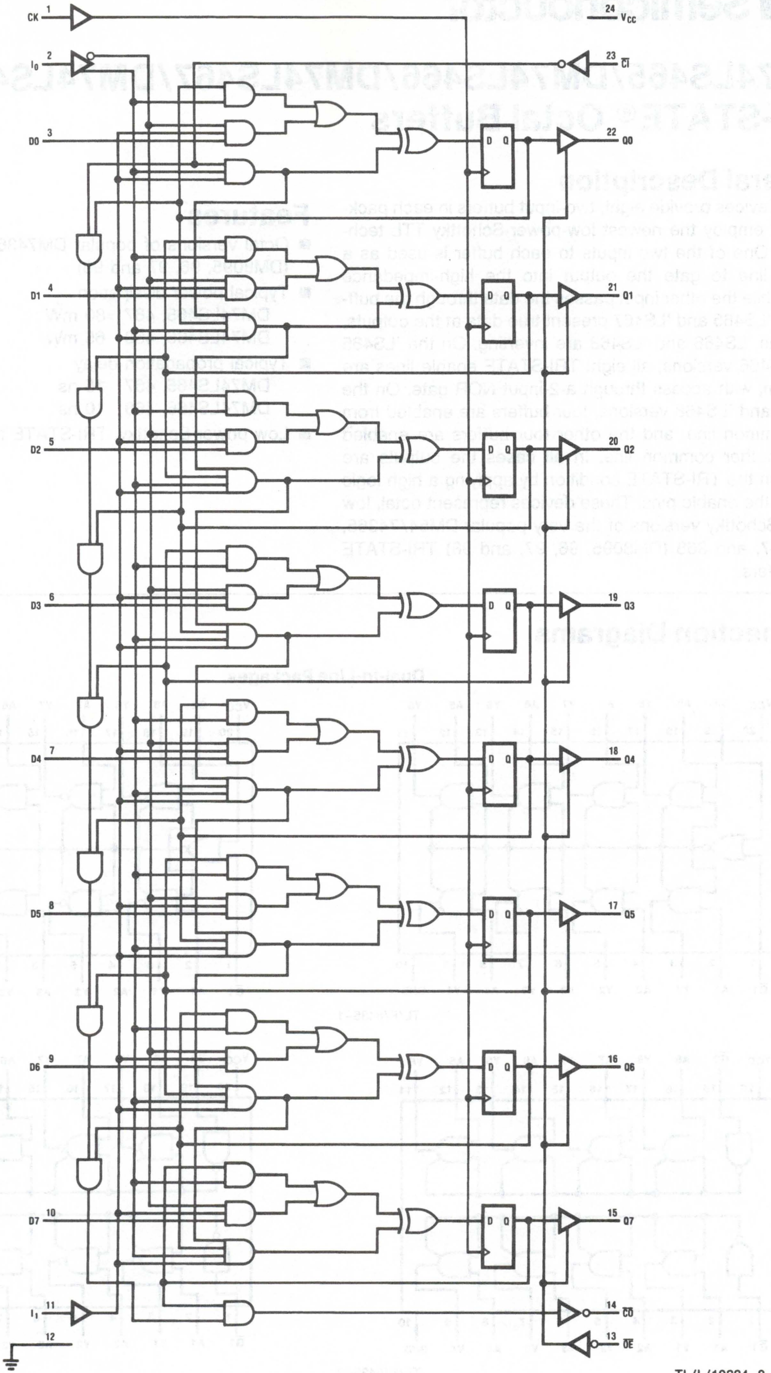
Note A: V_T = 1.5V.

Note B: C_L includes probe and jig capacitance.

Note C: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Logic Diagram

Octal Counter


CK 1
I0 2
D0 3
D1 4
D2 5
D3 6
D4 7
D5 8
D6 9
D7 10
I1 11
12
24 VCC
23 CI
22 Q0
21 Q1
20 Q2
19 Q3
18 Q4
17 Q5
16 Q6
15 Q7
14 CO
13 OE
D Q

TL/L/10224-8

National Semiconductor

DM74LS465/DM74LS466/DM74LS467/DM74LS468 TRI-STATE® Octal Buffers

General Description

These devices provide eight, two-input buffers in each package. All employ the newest low-power-Schottky TTL technology. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state, while the other input passes the data through the buffer. The 'LS465 and 'LS467 present true data at the outputs, while the 'LS466 and 'LS468 are inverting. On the 'LS465 and 'LS466 versions, all eight TRI-STATE enable lines are common, with access through a 2-input NOR gate. On the 'LS467 and 'LS468 versions, four buffers are enabled from one common line, and the other four buffers are enabled from another common line. In all cases the outputs are placed in the TRI-STATE condition by applying a high logic level to the enable pins. These devices represent octal, low power-Schottky versions of the very popular DM54/74365, 366, 367, and 368 (DM8095, 96, 97, and 98) TRI-STATE hex buffers.

Features

- Octal versions of popular DM74365, 366, 367, and 368 (DM8095, 96, 97 and 98)
- Typical power dissipation

DM74LS465, 467	80 mW
DM74LS466, 468	65 mW

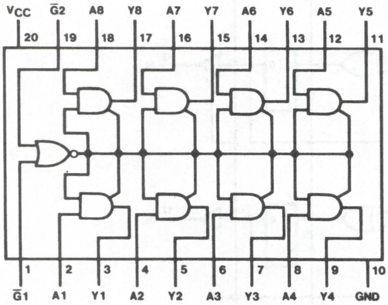
- Typical propagation delay

DM74LS465, 467	15 ns
DM74LS466, 468	10 ns

- Low power-Schottky, TRI-STATE technology

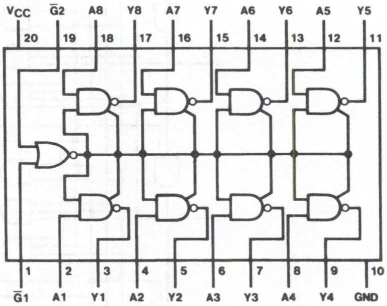
Connection Diagrams

Dual-In-Line Packages



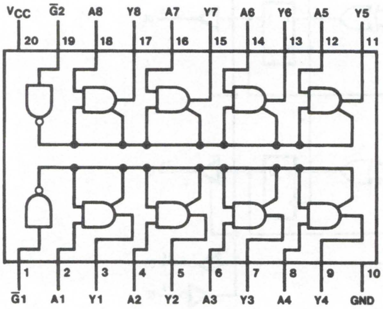
VCC G2 A8 Y8 A7 Y7 A6 Y6 A5 Y5
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10
G1 A1 Y1 A2 Y2 A3 Y3 A4 Y4 GND

TL/F/6435–1



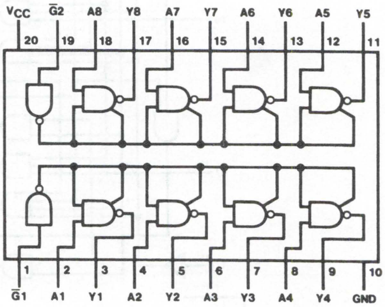
VCC G2 A8 Y8 A7 Y7 A6 Y6 A5 Y5
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10
G1 A1 Y1 A2 Y2 A3 Y3 A4 Y4 GND

TL/F/6435–2



VCC G2 A8 Y8 A7 Y7 A6 Y6 A5 Y5
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10
G1 A1 Y1 A2 Y2 A3 Y3 A4 Y4 GND

TL/F/6435–3



VCC G2 A8 Y8 A7 Y7 A6 Y6 A5 Y5
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10
G1 A1 Y1 A2 Y2 A3 Y3 A4 Y4 GND

TL/F/6435–4

Order Numbers DM74LS465WM, DM74LS465N, DM74LS466WM, DM74LS466N, DM74LS467WM, DM74LS467N, DM74LS468WM or DM74LS468N
See NS Package Number M20B or N20A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. the parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS465, 466, 467, 468			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−5.2	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

'LS465 and 'LS467 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.7			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.5	V
		I_{OL} = 12 mA, V_{CC} = Min			0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V, A (Note 3)			−20	μA
		V_I = 0.4V, A (Note 4)			−50	
		$\overline{G}$			−50	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max			20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)		16	26	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Both $\overline{G}$ inputs are at 2V.

Note 4: Both $\overline{G}$ inputs are at 0.4V.

'LS465 and 'LS467 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω C_L = 50 pF Min	 C_L = 50 pF Max	 C_L = 150 pF Min	 C_L = 150 pF Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output		16		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		28		40	ns
t_{PZH}	Output Enable Time to High Level Output		25		30	ns
t_{PZL}	Output Enable Time to Low Level Output		30		42	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)		27			ns

Note 1: C_L = 5 pF.

'LS466 and 'LS468 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		DM74	2.7			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min					0.5	V
		I_{OL} = 12 mA, V_{CC} = Min					0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V					0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.5V	A (Note 4)			−20	μA
			V_I = 0.4V	A (Note 5)			−50	
				$\overline{G}$			−50	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max					20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max					−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)			−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 5)				13	21	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs are at 0.4V.

'LS466 and 'LS468 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		10		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		17		30	ns
t_{PZH}	Output Enable Time to High Level Output		15		30	ns
t_{PZL}	Output Enable Time to Low Level Output		35		45	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)		27			ns

Note 1: C_L = 5 pF.

Function Tables

LS465

Inputs			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	H	H
L	L	L	L

LS466

Inputs			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	H	L
L	L	L	H

LS467

Inputs		Output
$\overline{G}$	A	Y
H	X	Hi-Z
L	H	H
L	L	L

LS468

Inputs		Output
$\overline{G}$	A	Y
H	X	Hi-Z
L	H	L
L	L	H

H = High Logic Level
L = Low Logic Level
X = Either High or Low Logic Level
Hi-Z = High Impedance (Off) State

National Semiconductor

DM54LS469/DM74LS469 8-Bit Up/Down Counter

General Description

The ‘LS469 is an 8-bit synchronous up/down counter with parallel load and hold capability. Three function-select inputs ($\overline{LD}$, $\overline{UD}$, $\overline{CBI}$) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

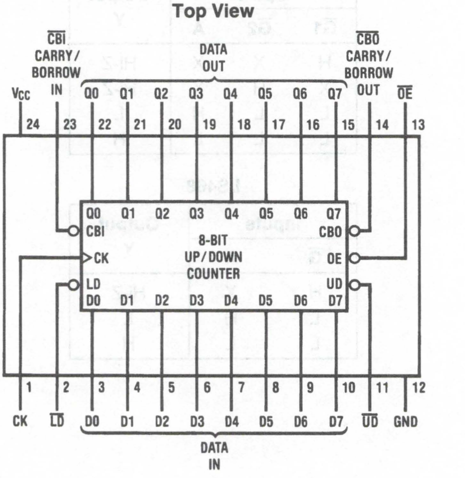
The LOAD operation loads the inputs (D_7–D_0) into the output register (Q_7–Q_0). The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CBI}$ = LOW), otherwise the operation is a HOLD. The carry-out ($\overline{CBO}$) is TRUE ($\overline{CBO}$ = LOW) when the output register (Q_7–Q_0) is all HIGHs, otherwise FALSE ($\overline{CBO}$ = HIGH). The DECREMENT operation subtracts one from the output register when the borrow-in input is TRUE ($\overline{CBI}$ = LOW), otherwise the operation is a HOLD. The borrow-out ($\overline{CBO}$) is TRUE ($\overline{CBO}$ = LOW) when the output register (Q_7–Q_0) is all LOWs, otherwise FALSE ($\overline{CBO}$ = HIGH).

The output register (Q_7–Q_0) is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus-interface standards. Two or more ‘LS469 octal up/down counters may be cascaded to provide larger counters.

Features/Benefits

- 8-bit up/down counter for microprogram-counter, DMA controller and general-purpose counting applications
- 8 bits matches byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP saves space
- TRI-STATE® outputs drive bus lines
- Low current PNP inputs reduce loading
- Expandable in 8-bit increments

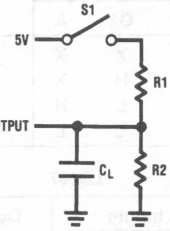
Connection Diagram


Top View
$\overline{CBI}$ CARRY/ BORROW IN
DATA OUT
$\overline{CBO}$ CARRY/ BORROW OUT
V_{CC}
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
$\overline{OE}$
24 23 22 21 20 19 18 17 16 15 14 13
8-BIT UP/DOWN COUNTER
CBI CK LD CBO OE UD
D0 D1 D2 D3 D4 D5 D6 D7
1 2 3 4 5 6 7 8 9 10 11 12
CK $\overline{LD}$ D0 D1 D2 D3 D4 D5 D6 D7 $\overline{UD}$ GND
DATA IN

TL/L/8333-1

Order Number DM54LS469J, DM74LS469J or DM74LS469N
See NS Package Number J24F or N24C

Standard Test Load


S1
5V
R1
OUTPUT
C_L
R2

TL/L/8333-3

Function Table

$\overline{OE}$	CK	$\overline{LD}$	$\overline{UD}$	$\overline{CBI}$	D7–D0	Q7–Q0	Operation
H	X	X	X	X	X	Z	HI-Z
L	↑	L	X	X	D	D	LOAD
L	↑	H	L	H	X	Q	HOLD
L	↑	H	L	L	X	Q plus 1	INCREMENT
L	↑	H	H	H	X	Q	HOLD
L	↑	H	H	L	X	Q minus 1	DECREMENT

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	$-65°C$ to $+150°C$

Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		−55		125*	0		75	°C
t_W	Width of Clock	Low	40			35	10		ns
		High	30			25			
t_{SU}	Set Up Time		60			50			ns
t_h	Hold Time		0	−15		0	−15		

*Case Temperature

Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ†	Max	Units
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IH}	High-Level Input Voltage				2			V
V_{IC}	Input Clamp Voltage	$V_{CC}=MIN$	$I_I=-18$ mA				−1.5	V
I_{IL}	Low-Level Input Current	$V_{CC}=MAX$	$V_I=0.4V$				−0.25	mA
I_{IH}	High-Level Input Current	$V_{CC}=MAX$	$V_I=2.4V$				25	µA
I_I	Maximum Input Current	$V_{CC}=MAX$	$V_I=5.5V$				1	mA
V_{OL}	Low-Level Output Voltage	$V_{CC}=MIN$ $V_{IL}=0.8V$ $V_{IH}=2V$	MIL	$I_{OL}=12$ mA			0.5	V
			COM	$I_{OL}=24$ mA				
V_{OH}	High-Level Output Voltage	$V_{CC}=MIN$ $V_{IL}=0.8V$ $V_{IH}=2V$	MIL	$I_{OH}=-2$ mA	2.4			V
			COM	$I_{OH}=-3.2$ mA				
I_{OZL}	Off-State Output Current	$V_{CC}=MAX$ $V_{IL}=0.8V$ $V_{IH}=2V$		$V_O=0.4V$			−100	µA
I_{OZH}				$V_O=2.4V$			100	µA
I_{OS}	Output Short-Circuit Current*	$V_{CC}=5.0V$		$V_O=0V$	−30		−130	mA
I_{CC}	Supply Current	$V_{CC}=MAX$				120	180	mA

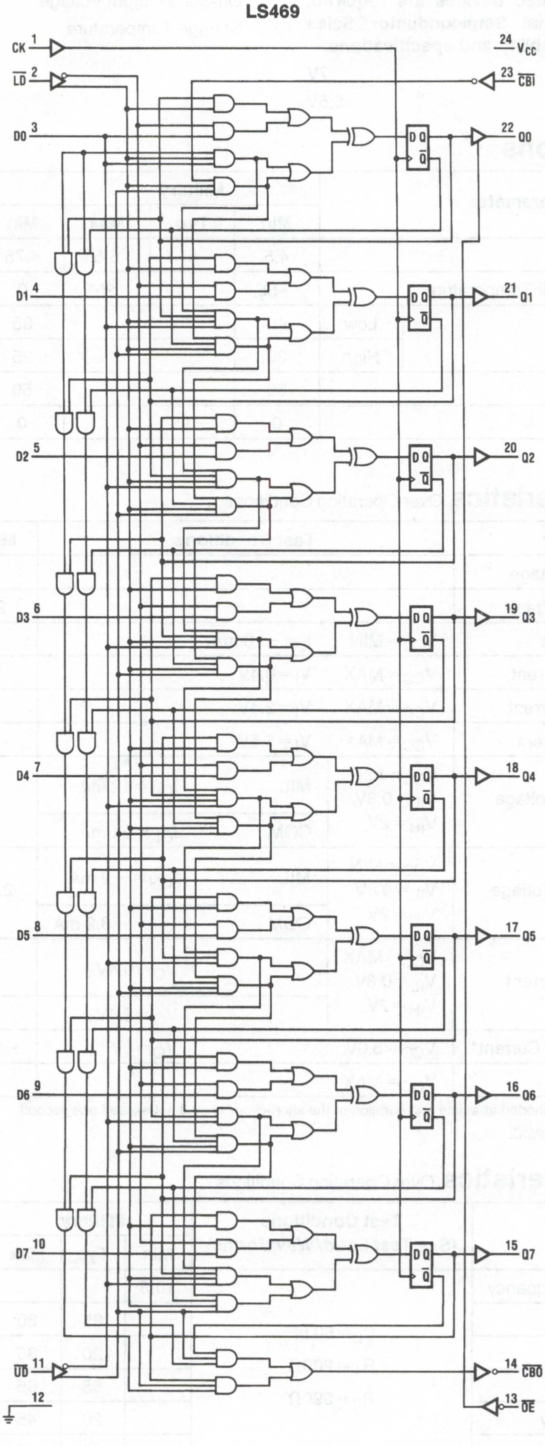
*No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

† All typical values are $V_{CC}=5V$, $T_A=25°C$.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions (See Test Load/Waveforms)	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Clock Frequency		10.5			12.5			MHz
t_{PD}	$\overline{CBI}$ to $\overline{CBO}$ Delay	$C_L=50$ pF $R_1=200\Omega$ $R_2=390\Omega$		35	60		35	50	ns
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PD}	Clock to CBO			55	95		55	80	ns
t_{PZX}	Output Enable Delay			20	45		20	35	ns
t_{PXZ}	Output Disable Delay			20	45		20	35	ns

Logic Diagram



LS469
CK 1
LD 2
D0 3
D1 4
D2 5
D3 6
D4 7
D5 8
D6 9
D7 10
UD 11
12
24 VCC
23 CBI
22 Q0
21 Q1
20 Q2
19 Q3
18 Q4
17 Q5
16 Q6
15 Q7
14 CBO
13 OE
D Q
Q

TL/L/8333-2

National Semiconductor

DM54LS469A/DM74LS469A 8-Bit Up/Down Counter

General Description

The 'LS469A is an 8-bit synchronous up/down counter with parallel load and hold capability. Three function-select inputs ($\overline{LD}$, $\overline{UD}$, $\overline{CBI}$) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

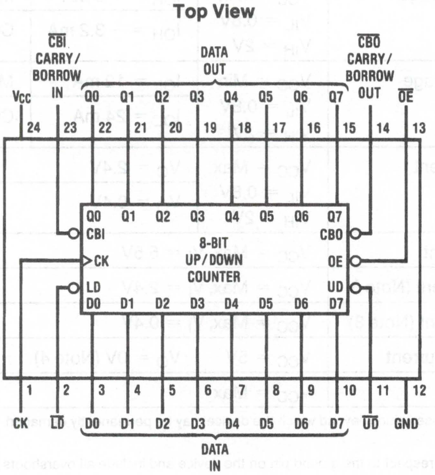
The LOAD operation loads the inputs (D7–D0) into the output register (Q7–Q0). The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CBI}$ = LOW), otherwise the operation is a HOLD. The carry-out ($\overline{CBO}$) is True (CBO = LOW) when the output register (Q7–Q0) is all HIGHs, otherwise FALSE ($\overline{CBO}$ = HIGH). The DECREMENT operation subtracts one from the output register when the borrow-in input is TRUE ($\overline{CBI}$ = LOW), otherwise the operation is a HOLD. The borrow-out ($\overline{CBO}$) is true ($\overline{CBO}$ = LOW) when the output register (Q7–Q0) is all LOWs, otherwise FALSE ($\overline{CBO}$ = HIGH).

The output register (Q7–Q0) is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus-interface standards. Two or more 'LS469A octal up/down counters may be cascaded to provide larger counters.

Features

- Octal Register for general purpose interfacing applications
- 8 bits match byte boundaries
- Low current PNP inputs reduce loading
- Bus-structured pinout
- TRI-STATE® outputs
- 24-pin SKINNYDIP saves space

Connection Diagram


Top View
$\overline{CBI}$ CARRY/ BORROW IN
DATA OUT
$\overline{CBO}$ CARRY/ BORROW OUT
VCC
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
$\overline{OE}$
24
23
22
21
20
19
18
17
16
15
14
13
CBI
CK
LD
8-BIT UP/DOWN COUNTER
CBO
OE
UD
D0
D1
D2
D3
D4
D5
D6
D7
1
2
3
4
5
6
7
8
9
10
11
12
CK
$\overline{LD}$
D0
D1
D2
D3
D4
D5
D6
D7
$\overline{UD}$
GND
DATA IN

TL/L/10223-1

Order Number DM54LS469AJ, DM74LS469AJ, DM74LS469AN or DM74LS469AV
See NS Package Number J24F, N24C or V28A

Function Table

$\overline{OE}$	CK	$\overline{LD}$	$\overline{UD}$	$\overline{CBI}$	D7–D0	Q7–Q0	Operation
H	X	X	X	X	X	Z	HI-Z
L	↑	L	X	X	D	D	LOAD
L	↑	H	L	H	X	Q	HOLD
L	↑	H	L	L	X	Q Plus 1	INCREMENT
L	↑	H	H	H	X	Q	HOLD
L	↑	H	H	L	X	Q Minus 1	DECREMENT

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
ESD Tolerance	>1000V

Czap = 100 pF
Rzap = 150Ω
Test Method: Human Body Model
Test Specification: NSC SOP 5-028

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55	25		0	25	75	°C
T_C	Operating Case Temperature			125				°C

Electrical Characteristics Series 24A Over Recommended Operating Temperature Range

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	(Note 2)			2			V
V_{IL}	Low Level Input Voltage	(Note 2)					0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, II = −18 mA				−0.8	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = −2 mA	MIL	2.4	2.9		V
			I_{OH} = −3.2 mA	COM				
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 12 mA	MIL		0.3	0.5	V
			I_{OL} = 24 mA	COM				
I_{OZH}	Off-State Output Current (Note 3)	V_{CC} = Max V_{IL} = 0.8V V_{IH} = 2V	V_O = 2.4V				100	μA
I_{OZL}			V_O = 0.4V				−100	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V					1	mA
I_{IH}	High Level Input Current (Note 3)	V_{CC} = Max, V_I = 2.4V					25	μA
I_{IL}	Low Level Input Current (Note 3)	V_{CC} = Max, V_I = 0.4V				−0.04	−0.25	mA
I_{OS}	Output Short-Circuit Current	V_{CC} = 5V	V_O = 0V (Note 4)		−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max				135	180	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device maybe operated at these values.

Note 2: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

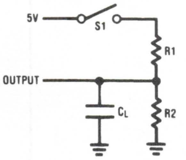
Note 3: I/O leakage as the worst case of IOZX or IIX, e.g., I_{IL} and IOZL.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage otherwise may result.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter		Test Conditions	Military			Commercial			Units
				Min	Typ	Max	Min	Typ	Max	
t_S	Set-Up Time from Input			40	20		30	20		ns
t_W	Width of Clock	High		20	7		15	7		ns
		Low		35	15		25	15		ns
t_{pd}	$\overline{\text{CBI}}$ to $\overline{\text{CBO}}$ Delay		C_L = 50 pF		23	35		23	30	ns
t_{clk}	Clock to Output		C_L = 50 pF		10	25		10	15	ns
t_{pzx}	Output Enable Delay		C_L = 50 pF		19	35		19	30	ns
t_{pzx}	Output Disable Delay		C_L = 5 pF		15	35		15	30	ns
t_H	Hold Time			0	−15		0	−15		ns
f_{max}	Maximum Frequency			15.3	32		22.2	32		MHz

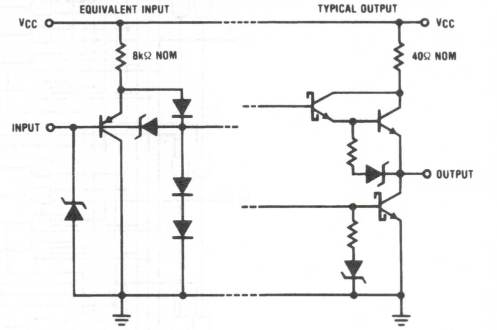
Test Load


5V
S1
R1
OUTPUT
CL
R2

MIL	COM'L
R1 = 390	R1 = 200
R2 = 750	R2 = 390

TL/L/10223-2

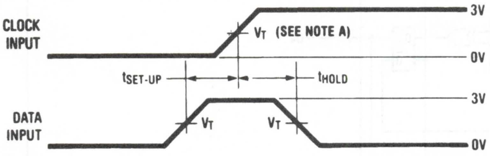
Schematic of Inputs and Outputs


EQUIVALENT INPUT
TYPICAL OUTPUT
VCC
VCC
8kΩ NOM
40Ω NOM
INPUT
OUTPUT

TL/L/10223-3

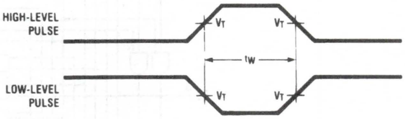
Test Waveforms

Set-Up and Hold


CLOCK INPUT
VT (SEE NOTE A)
3V
0V
tSET-UP
tHOLD
DATA INPUT
VT
VT
3V
0V

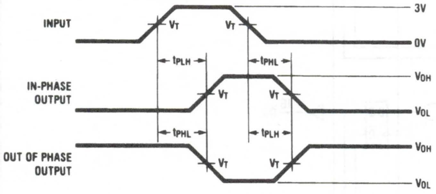
TL/L/10223-4

Pulse Width


HIGH-LEVEL PULSE
VT
VT
tW
LOW-LEVEL PULSE
VT
VT

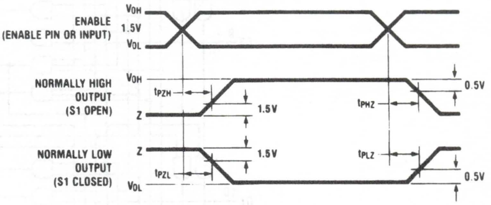
TL/L/10223-6

Propagation Delay


INPUT
VT
VT
3V
0V
tPLH
tPHL
IN-PHASE OUTPUT
VT
VT
VOH
VOL
tPHL
tPLH
OUT OF PHASE OUTPUT
VT
VT
VOH
VOL

TL/L/10223-5

Enable and Disable


ENABLE (ENABLE PIN OR INPUT)
VOH
1.5V
VOL
NORMALLY HIGH OUTPUT (S1 OPEN)
VOH
Z
tPZH
1.5V
tPHZ
0.5V
NORMALLY LOW OUTPUT (S1 CLOSED)
Z
VOL
tPZL
1.5V
tPLZ
0.5V

TL/L/10223-7

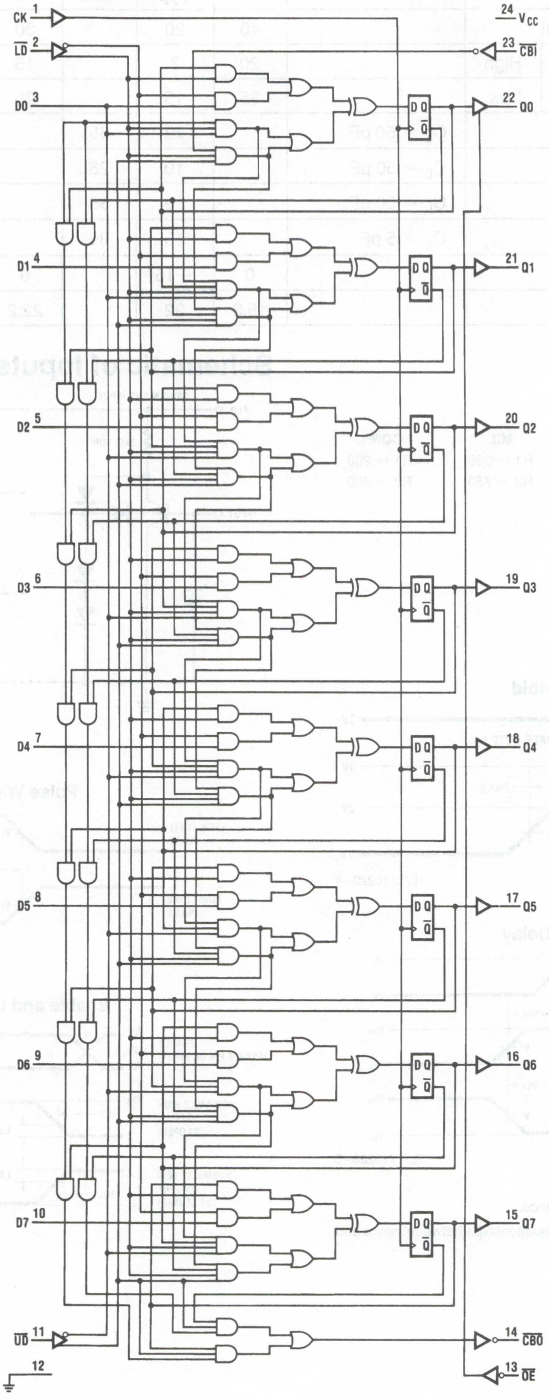
Note A: VT = 1.5V.

Note B: C_L includes probe and jig capacitance.

Note C: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Logic Diagram

8-Bit Up/Down Counter


CK 1
LD 2
D0 3
D1 4
D2 5
D3 6
D4 7
D5 8
D6 9
D7 10
UD 11
12
24 VCC
23 CBI
22 Q0
21 Q1
20 Q2
19 Q3
18 Q4
17 Q5
16 Q6
15 Q7
14 CBO
13 OE
D Q
Q

TL/L/10223-8

National Semiconductor

54LS490/DM74LS490
Dual Decade Counter

General Description

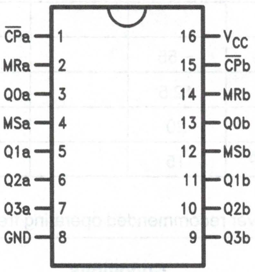
The 'LS490 contains a pair of high speed 4-stage ripple counters. Each half of the 'LS490 has individual Clock, Master Reset and Master Set (Preset 9) inputs. Each section counts in the 8421 BCD code.

Features

- Dual version of 54LS/74LS90
- Individual asynchronous clear and preset to 9 for each counter
- Count frequency—typically 65 MHz
- Input clamp diodes limit high speed termination effects
- TTL and CMOS compatible

Connection Diagram

Dual-In-Line Package


$\overline{CPa}$ 1
MRa 2
Q0a 3
MSa 4
Q1a 5
Q2a 6
Q3a 7
GND 8
16 V_{CC}
15 $\overline{CPb}$
14 MRb
13 Q0b
12 MSb
11 Q1b
10 Q2b
9 Q3b

TL/F/10188-1

Order Number 54LS490DMQB, 54LS490FMQB, DM54LS490M or DM54LS490N
See NS Package Number J16A, M16A, N16E or W16A

Pin Names	Description
MS	Master Set (Set to 9) Input (Active HIGH)
MR	Master Reset Input (Active HIGH)
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)
Q0–Q3	Counter Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS490			DM74LS490			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_w (L)	$\overline{CP}$ Pulse Width LOW	12.5			12.5			ns
t_w (H)	MR, MS Pulse Width HIGH	20			20			ns
t_{rec}	Recovery Time, MR or MS to $\overline{CP}$	15			15			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V	Inputs			100	μA
			$\overline{CP}$			200	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Inputs			20	μA
			$\overline{CP}$			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Inputs	−0.03		−0.4	mA
			$\overline{CP}$	−0.18		−2.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				26	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

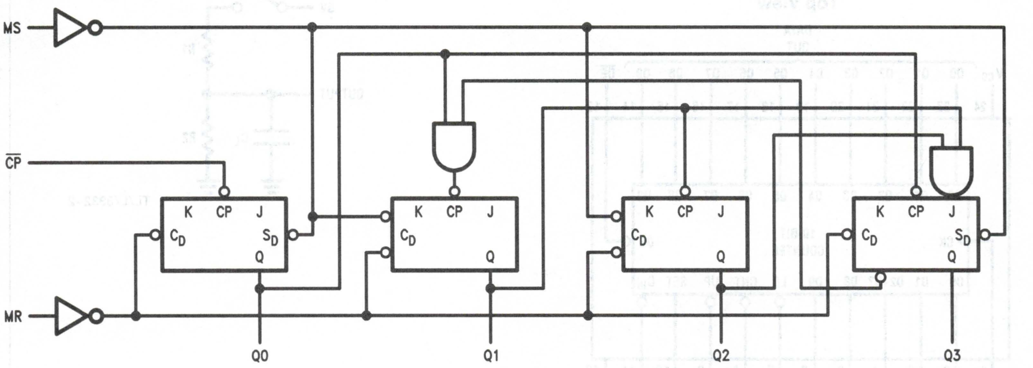
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 15\ pF$		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	40		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q0		15 15	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q1 or Q3		30 30	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q2		45 45	ns
t_{PLH} t_{PHL}	Propagation Delay MS to Qn		35 35	ns
t_{PHL}	Propagation Delay MR to Qn		39	ns

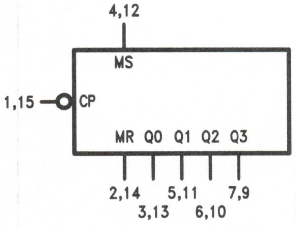
Logic Diagram (one-half shown)



MS
$\overline{CP}$
MR
K
CP
J
C_D
S_D
Q
Q0
Q1
Q2
Q3

TL/F/10188-4

Logic Symbol

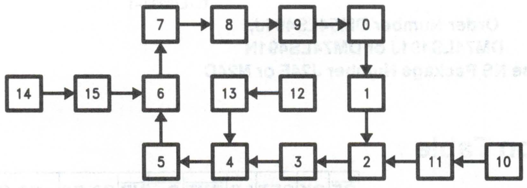


4,12
MS
1,15
CP
MR
Q0
Q1
Q2
Q3
2,14
3,13
5,11
6,10
7,9

TL/F/10188-2

V_{CC} = Pin 16
GND = Pin 8

State Diagram



7
8
9
0
14
15
6
13
12
1
5
4
3
2
11
10

TL/F/10188-3

National Semiconductor

DM54LS491/74LS491 10-Bit Counter

General Description

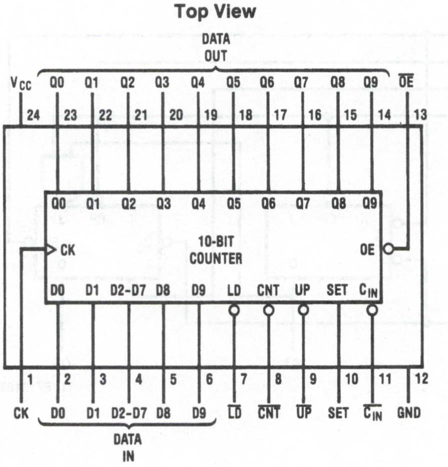
The ten-bit counter can count up, count down, set, and load 2 LSB's, 2 MSB's and 6 middle bits high or low as a group. All operations are synchronous with the clock. SET overrides LOAD, COUNT and HOLD. LOAD overrides COUNT. COUNT is conditional on C_{IN}, otherwise it holds.

All outputs are enabled when $\overline{OE}$ is low, otherwise HIGH-Z. The 24 mA I_{OL} outputs are suitable for driving RAM/PROM address lines in video graphics systems.

Features/Benefits

- CRT vertical and horizontal timing generation
- Bus-structured pinout
- 24-pin SKINNYDIP saves space
- TRI-STATE® outputs drive bus lines
- Low current PNP inputs reduce loading

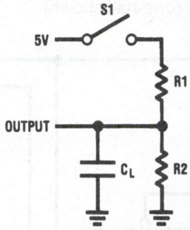
Connection Diagram


Top View
DATA OUT
V_{CC}
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
$\overline{OE}$
24
23
22
21
20
19
18
17
16
15
14
13
10-BIT COUNTER
CK
OE
D0
D1
D2-D7
D8
D9
LD
CNT
UP
SET
C_{IN}
1
2
3
4
5
6
7
8
9
10
11
12
CK
D0
D1
D2-D7
D8
D9
$\overline{LD}$
$\overline{CNT}$
$\overline{UP}$
SET
$\overline{C_{IN}}$
GND
DATA IN

TL/L/8332-1

Order Number DM54LS491J, DM74LS491J or DM74LS491N
See NS Package Number J24F or N24C

Standard Test Load


S1
5V
R1
OUTPUT
C_L
R2

TL/L/8332-2

Function Table

$\overline{OE}$	CK	SET	LD	$\overline{CNT}$	$\overline{C_{IN}}$	$\overline{UP}$	D9-D0	Q9-Q0	Operation
H	X	X	X	X	X	X	X	Z	Hi-Z
L	↑	H	X	X	X	X	X	H	Set all HIGH
L	↑	L	L	X	X	X	D	D	LOAD D
L	↑	L	H	H	X	X	X	Q	HOLD
L	↑	L	H	L	H	X	X	Q	HOLD
L	↑	L	H	L	L	L	X	Q plus 1	Count UP
L	↑	L	H	L	L	H	X	Q minus 1	Count DN

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65° to +150°C

Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		−55		125*	0		75	°C
t_w	Width of Clock	High	40			40			ns
		Low	35			35			
t_{SU}	Set-Up Time		60			50			ns
t_h	Hold Time		0	−15		0	−15		

* Case temperature

Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ†	Max	Units
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IH}	High-Level Input Voltage				2			V
V_{IC}	Input Clamp Voltage	$V_{CC}=MIN$		$I_I=-18$ mA			−1.5	V
I_{IL}	Low-Level Input Current	$V_{CC}=MAX$		$V_I=0.4V$			−0.25	mA
I_{IH}	High-Level Input Current	$V_{CC}=MAX$		$V_I=2.4V$			25	μA
I_I	Maximum Input Current	$V_{CC}=MAX$		$V_I=5.5V$			1	mA
V_{OL}	Low-Level Output Voltage	$V_{CC}=MIN$ $V_{IL}=0.8V$ $V_{IH}=2V$	MIL	$I_{OL}=12$ mA			0.5	V
			COM	$I_{OL}=24$ mA				
V_{OH}	High-Level Output Voltage	$V_{CC}=MIN$ $V_{IL}=0.8V$ $V_{IH}=2V$	MIL	$I_{OH}=-2$ mA	2.4			V
			COM	$I_{OH}=3.2$ mA				
I_{OZL}	Off-State Output Current	$V_{CC}=MAX$ $V_{IL}=0.8V$ $V_{IH}=2V$		$V_O=0.4V$			−100	μA
I_{OZH}				$V_O=2.4V$			100	μA
I_{OS}	Output Short-Circuit Current*	$V_{CC}=5.0V$		$V_O=0V$	−30		−130	mA
I_{CC}	Supply Current	$V_{CC}=MAX$				120	180	mA

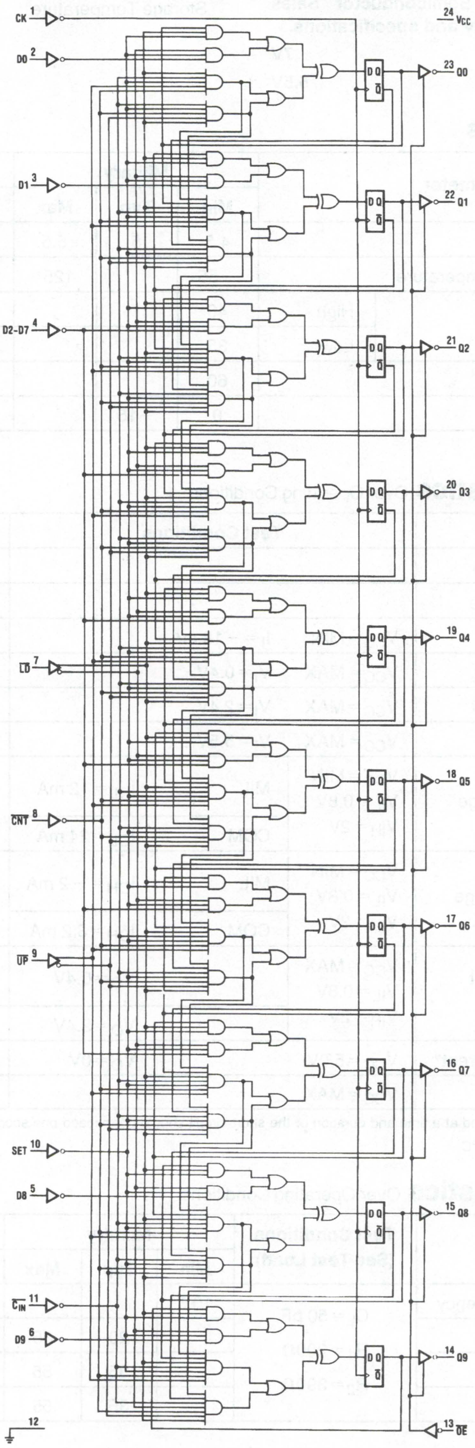
* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† All typical values are at $V_{CC}=5V$, $T_A=25°C$

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions (See Test Load)	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Clock Frequency	$C_L=50$ pF $R_1=200\Omega$ $R_2=390\Omega$	10.5			12.5			MHz
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PZX}	Output Enable Delay			35	55		35	45	ns
t_{PXZ}	Output Disable Delay			35	55		35	45	ns

Logic Diagram



10-Bit Up/Down Counter

CK 1
D0 2
D1 3
D2-D7 4
LD 7
CNT 8
UP 9
SET 10
D8 5
CIN 11
D9 6
12
24 VCC
D Q
Q
23 Q0
22 Q1
21 Q2
20 Q3
19 Q4
18 Q5
17 Q6
16 Q7
15 Q8
14 Q9
13 OE

TL/L/8332-3

National Semiconductor

DM54LS491A/DM74LS491A
10-Bit Counter

General Description

The ten-bit counter can count up, count down, set, and load 2 LSB's, 2 MSB's and 6 middle bits high or low as a group. All operations are synchronous with the clock. SET overrides LOAD, COUNT and HOLD. LOAD overrides COUNT. COUNT is conditional on C_{IN}, otherwise it holds.

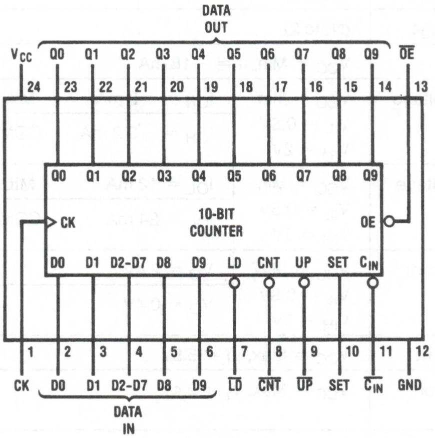
All outputs are enabled when OE is low, otherwise HIGH-Z. The 24 mA I_{OL} outputs are suitable for driving RAM/PROM address lines in video graphics systems.

Features

- CRT vertical and horizontal timing generation
- Bus-structured pinout
- Low current PNP inputs reduce loading
- TRI-STATE® outputs
- 24-pin SKINNYDIP saves space

Connection Diagram

Top View


DATA OUT
V_{CC} 24
Q0 23
Q1 22
Q2 21
Q3 20
Q4 19
Q5 18
Q6 17
Q7 16
Q8 15
Q9 14
$\overline{OE}$ 13
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9
CK
10-BIT COUNTER
OE
D0 D1 D2-D7 D8 D9 LD CNT UP SET C_{IN}
1 CK
2 D0
3 D1
4 D2-D7
5 D8
6 D9
7 $\overline{LD}$
8 $\overline{CNT}$
9 $\overline{UP}$
10 SET
11 $\overline{C_{IN}}$
12 GND
DATA IN

TL/L/10222-1

Order Number DM54LS491AJ, DM74LS491AJ, DM74LS491AN or DM74LS491AV
See NS Package Number J24F, N24C or V28A

Function Table

$\overline{OE}$	CK	SET	LD	$\overline{CNT}$	C_{IN}	$\overline{UP}$	D9–D0	Q9–Q0	Operation
H	X	X	X	X	X	X	X	Z	Hi-Z
L	↑	H	X	X	X	X	X	H	Set all HIGH
L	↑	L	L	X	X	X	D	D	LOAD D
L	↑	L	H	H	X	X	X	Q	HOLD
L	↑	L	H	L	H	X	X	Q	HOLD
L	↑	L	H	L	L	L	X	Q Plus 1	Count Up
L	↑	L	H	L	L	H	X	Q Minus 1	Count Down

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65°C to +150°C

ESD Tolerance >1000V
Czap = 100 pF
Rzap = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP 5-028

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55	25		0	25	75	°C
T_C	Operating Case Temperature			125				°C

Electrical Characteristics Series 24A Over Recommended Operating Temperature Range

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	(Note 2)			2			V
V_{IL}	Low Level Input Voltage	(Note 2)					0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, II = −18 mA				−0.8	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = −2 mA	MIL	2.4	2.9		V
			I_{OH} = −3.2 mA	COM				
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 12 mA	MIL		0.3	0.5	V
			I_{OL} = 24 mA	COM				
I_{OZH}	Off-State Output Current (Note 3)	V_{CC} = Max V_{IL} = 0.8V V_{IH} = 2V	V_O = 2.4V				100	µA
I_{OZL}			V_O = 0.4V				−100	µA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V					1	mA
I_{IH}	High Level Input Current (Note 3)	V_{CC} = Max, V_I = 2.4V					25	µA
I_{IL}	Low Level Input Current (Note 3)	V_{CC} = Max, V_I = 0.4V				−0.04	−0.25	mA
I_{OS}	Outut Short-Circuit Current	V_{CC} = 5V	V_O = 0V (Note 4)		−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max				135	180	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

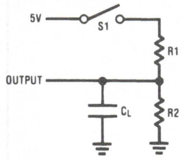
Note 3: I/O leakage as the worst case of IOZX or IIX, e.g., I_{IL} and IOZL.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage otherwise may result.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter		Test Condition	Military			Commercial			Units
				Min	Typ	Max	Min	Typ	Max	
t_S	Setup Time from Input			40	20		30	20		ns
t_W	Width of Clock	High		20	7		15	7		ns
		Low		35	15		25	15		ns
t_H	Hold Time			0	−15		0	−15		ns
tCLK	Clock to Output		$C_L = 50$ pF		10	25		10	15	ns
tpzx	Output Enable Delay		$C_L = 50$ pF		19	35		19	30	ns
tpxz	Output Disable Delay		$C_L = 5$ pF		15	35		15	30	ns
f_{MAX}	Maximum Frequency			15.3	32		22.2	32		MHz

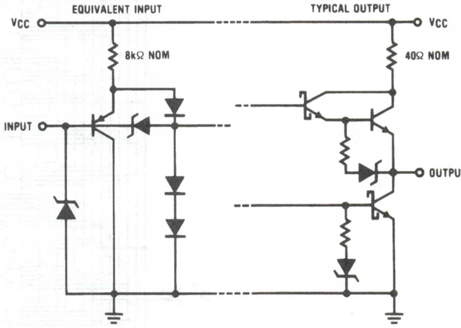
Test Load


5V
S1
R1
OUTPUT
CL
R2

MIL	COM'L
R1 = 390	R1 = 200
R2 = 750	R2 = 390

TL/L/10222-2

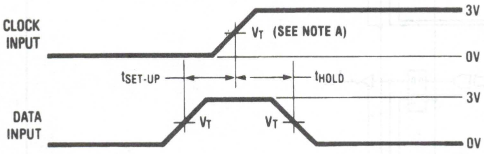
Schematic of Inputs and Outputs


EQUIVALENT INPUT
TYPICAL OUTPUT
VCC
VCC
8kΩ NOM
40Ω NOM
INPUT
OUTPUT

TL/L/10222-3

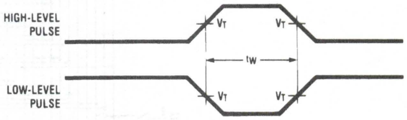
Test Waveforms

Set-up and Hold


CLOCK INPUT
3V
VT (SEE NOTE A)
0V
tSET-UP
tHOLD
3V
DATA INPUT
VT
VT
0V

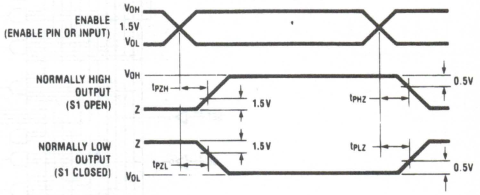
TL/L/10222-4

Pulse Width


HIGH-LEVEL PULSE
VT
VT
tW
LOW-LEVEL PULSE
VT
VT

TL/L/10222-5

Enable and Disable


ENABLE (ENABLE PIN OR INPUT)
VOH
1.5V
VOL
NORMALLY HIGH OUTPUT (S1 OPEN)
VOH
Z
tPZH
1.5V
tPHZ
0.5V
NORMALLY LOW OUTPUT (S1 CLOSED)
Z
VOL
tPZL
1.5V
tPLZ
0.5V

TL/L/10222-6

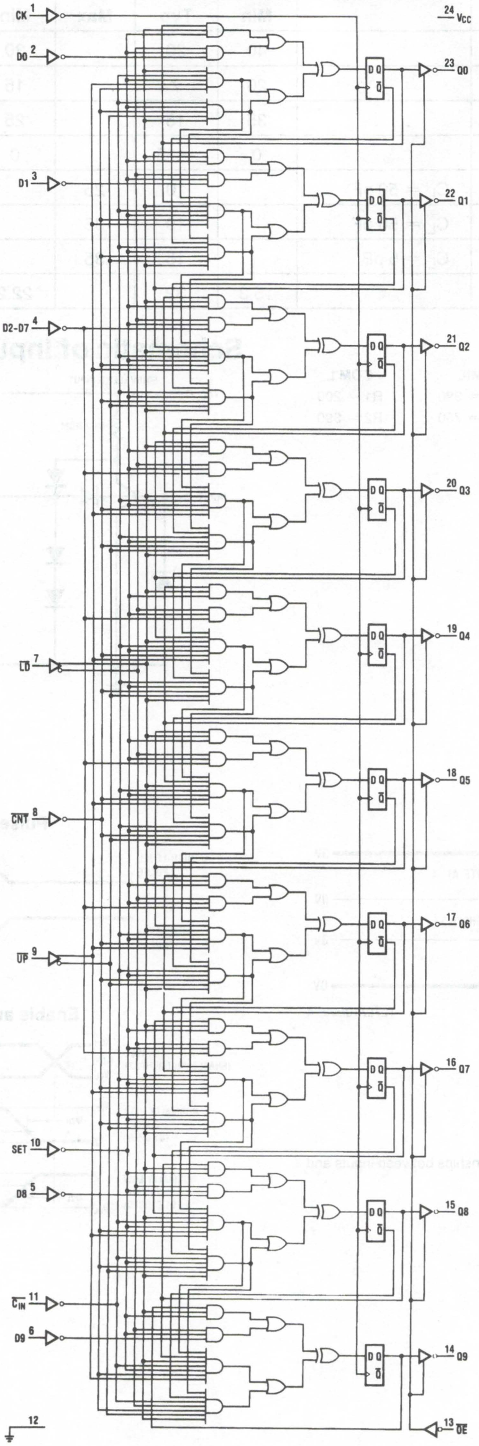
Note A: $V_T = 1.5V$.

Note B: C_L includes probe and jig capacitance.

Note B: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Logic Diagram

10-Bit Up/Down Counter


1 CK
2 D0
3 D1
4 D2-D7
7 LD
8 CNT
9 UP
10 SET
5 D8
11 CIN
6 D9
12
24 VCC
23 Q0
22 Q1
21 Q2
20 Q3
19 Q4
18 Q5
17 Q6
16 Q7
15 Q8
14 Q9
13 OE
D Q
Q̄

TL/L/10222-7

National Semiconductor

DM54LS498/DM74LS498 Octal Shift Register

General Description

The LS498 is an 8-bit synchronous shift register with parallel load and hold capability. Two function select inputs (I_0, I_1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the input ($D_7 - D_0$) into the output register ($Q_7 - Q_0$). The HOLD operation holds the previous value regardless of clock transitions. The SHIFT LEFT operation shifts the output register, Q, one bit to the left; Q_0 is replaced by LIRO. RILO outputs Q_7.

The SHIFT RIGHT operation shifts the output register, Q, one bit to the right; Q_7 is replaced by RILO. LIRO outputs Q_0.

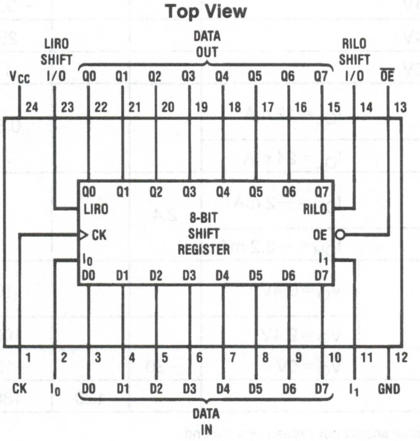
The output register ($Q_7 - Q_0$)—is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Two or more LS498 octal shift registers may be cascaded to provide larger shift registers as shown in the application section.

Features/Benefits

- Octal shift register for serial to parallel and parallel to serial applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP saves space
- TRI-STATE® outputs drive bus lines
- Low current PNP inputs reduce loading
- Expandable in 8-bit increments

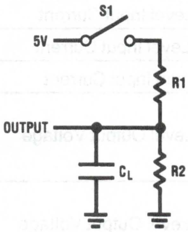
Connection Diagram


Top View
LIRO SHIFT I/O
DATA OUT
RILO SHIFT I/O
VCC
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
OE
24 23 22 21 20 19 18 17 16 15 14 13
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
LIRO
RILO
CK
8-BIT SHIFT REGISTER
OE
I0
I1
D0 D1 D2 D3 D4 D5 D6 D7
1 2 3 4 5 6 7 8 9 10 11 12
CK I0 D0 D1 D2 D3 D4 D5 D6 D7 I1 GND
DATA IN

TL/L/8331-1

Order Number DM54LS498J, DM74LS498J or DM74LS498N
See NS Package Number J24F or N24C

Standard Test Load


S1
5V
R1
OUTPUT
CL
R2

TL/L/8331-2

Function Table

$\overline{OE}$	CK	I_1	I_0	$D_7 - D_0$	$Q_7 - Q_0$	Operation
H	X	X	X	X	Z	HI-Z
L	↑	L	L	X	L	HOLD
L	↑	L	H	X	SR(Q)	SHIFT RIGHT
L	↑	H	L	X	SL(Q)	SHIFT LEFT
L	↑	H	H	D	D	LOAD

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65° to +150°C

Operating Conditions

Symbol	Parameter		Military Min	Military Typ	Military Max	Commercial Min	Commercial Typ	Commercial Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		−55		125*	0		75	°C
t_w	Width of Clock	Low	40			35			ns
		High	30			25			
t_{su}	Set-Up Time		60			50			ns
t_h	Hold Time		0	−15		0	−15		

*Case temperature

Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ†	Max	Units
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IH}	High-Level Input Voltage				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN	$I_I = -18$ mA				−1.5	V
I_{IL}	Low-Level Input Current	V_{CC} = MAX	$V_I = 0.4V$				−0.25	mA
I_{IH}	High-Level Input Current	V_{CC} = MAX	$V_I = 2.4V$				25	µA
I_I	Maximum Input Current	V_{CC} = MAX	$V_I = 5.5V$				1	mA
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN $V_{IL} = 0.8V$ $V_{IH} = 2V$	MIL	$I_{OL} = 12$ mA			0.5	V
			COM	$I_{OL} = 24$ mA				
V_{OH}	High-Level Output Voltage	V_{CC} = MIN $V_{IL} = 0.8V$ $V_{IH} = 2V$	MIL	$I_{OH} = -2$ mA	2.4			V
			COM	$I_{OH} = -3.2$ mA				
I_{OZL}	Off-State Output Current	V_{CC} = MAX $V_{IL} = 0.8V$ $V_{IH} = 2V$		$V_O = 0.4V$			−100	µA
I_{OZH}				$V_O = 2.4V$			100	µA
I_{OS}	Output Short-Circuit Current*	$V_{CC} = 5.0V$		$V_O = 0V$	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = MAX				120	180	mA

*No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

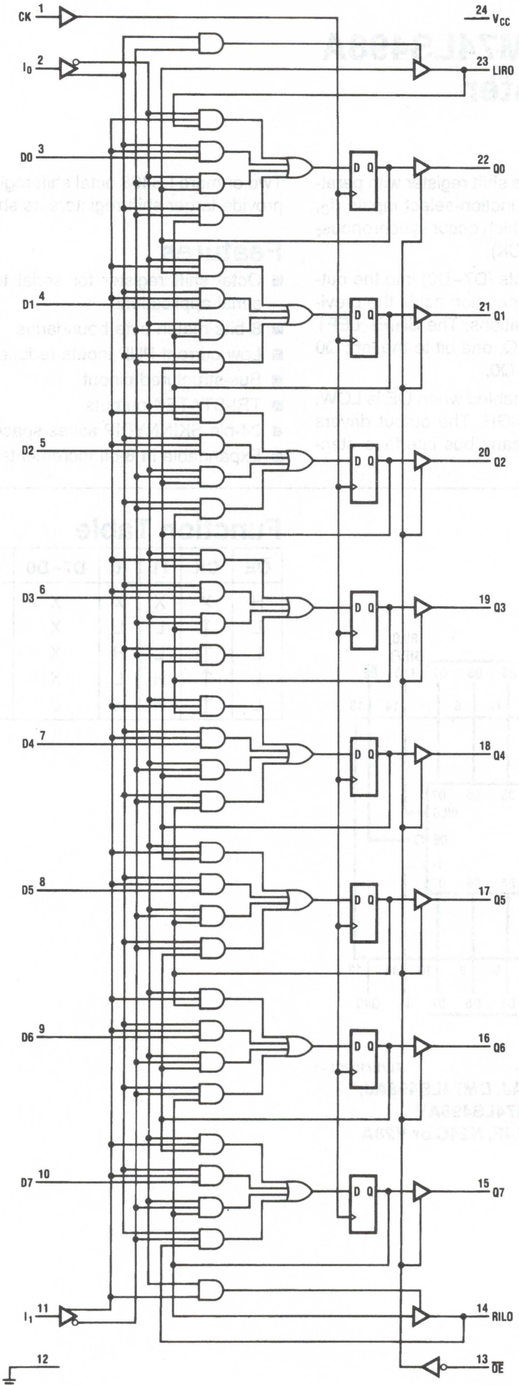
†All typical values are at $V_{CC} = 5V$, $T_A = 25°C$

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions (See Test Load)	Military Min	Military Typ	Military Max	Commercial Min	Commercial Typ	Commercial Max	Units
f_{MAX}	Maximum Clock Frequency		10.5			12.5			MHz
t_{PD}	I0, I1 to LIRO, RILO	$C_L = 50$ pF $R_1 = 200\Omega$ $R_2 = 390\Omega$		35	60		35	50	ns
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PD}	Clock to LIRO, RILO			55	95		55	80	ns
t_{PZX}	Output Enable Delay			35	55		35	45	ns
t_{PXZ}	Output Disable Delay			35	55		35	45	ns

Logic Diagram

Octal Shift Register


CK 1
I0 2
D0 3
D1 4
D2 5
D3 6
D4 7
D5 8
D6 9
D7 10
I1 11
12
24 VCC
23 LIRO
22 Q0
21 Q1
20 Q2
19 Q3
18 Q4
17 Q5
16 Q6
15 Q7
14 RILO
13 OE
D Q

TL/L/8331-3

National Semiconductor

DM54LS498A/DM74LS498A Octal Shift Register

General Description

The LS498A is an 8-bit synchronous shift register with parallel load and hold capability. Two function-select inputs (I_0, I_1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D7–D0) into the output register (Q7–Q0). The HOLD operation holds the previous value regardless of clock transitions. The SHIFT LEFT operation shifts the output register Q, one bit to the left; Q0 is replaced by LIRO. LIRO outputs Q0.

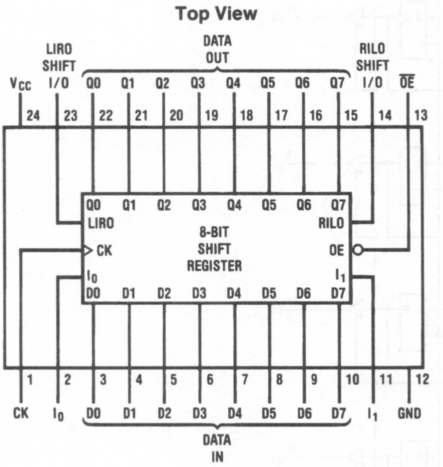
The output register (Q7–Q0)—is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Two or more LS498 octal shift registers may be cascaded to provide larger shift registers as shown in the application.

Features

- Octal shift register for serial to parallel and parallel to serial applications
- 8 bits match byte boundaries
- Low current PNP inputs reduce loading
- Bus-structured pinout
- TRI-STATE® outputs
- 24-pin SKINNYDIP saves space
- Expandable in 8-bit increments

Connection Diagram


Top View
LIRO SHIFT I/O
DATA OUT
RILO SHIFT I/O
V_{CC}
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
$\overline{OE}$
24 23 22 21 20 19 18 17 16 15 14 13
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
LIRO
RILO
8-BIT SHIFT REGISTER
CK
OE
I_0
I_1
D0 D1 D2 D3 D4 D5 D6 D7
1 2 3 4 5 6 7 8 9 10 11 12
CK I_0 D0 D1 D2 D3 D4 D5 D6 D7 I_1 GND
DATA IN

TL/L/10221–1

Order Number DM54LS498AJ, DM74LS498AJ, DM74LS498AN or DM74LS498AV
See NS Package Number J24F, N24C or V28A

Function Table

$\overline{OE}$	CK	I1	I0	D7–D0	Q7–Q0	Operation
H	X	X	X	X	Z	HI-Z
L	↑	L	L	X	L	HOLD
L	↑	L	H	X	SR(Q)	SHIFT RIGHT
L	↑	H	L	X	SL(Q)	SHIFT LEFT
L	↑	H	H	D	D	LOAD

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65° to +150°C
ESD Tolerance	>1000V

Czap = 100 pF
Rzap = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP 5-028

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55	25		0	25	75	°C
T_C	Operating Case Temperature			125				°C

Electrical Characteristics Series 24A Over Recommended Operating Temperature Range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	(Note 2)		2			V
V_{IL}	Low Level Input Voltage	(Note 2)				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−0.8	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = −2 mA MIL I_{OH} = −3.2 mA COM	2.4	2.9		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 12 mA MIL I_{OL} = 24 mA COM		0.3	0.5	V
I_{OZH}	Off-State Output Current (Note 3)	V_{CC} = Max V_{IL} = 0.8V V_{IH} = 2V	V_O = 2.4V			100	µA
I_{OZL}			V_O = 0.4V			−100	µA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current (Note 3)	V_{CC} = Max, V_I = 2.4V				25	µA
I_{IL}	Low Level Input Current (Note 3)	V_{CC} = Max, V_I = 0.4V			−0.04	−0.25	mA
I_{OS}	Output Short-Circuit Current	V_{CC} = 5V	V_O = 0V (Note 4)	−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max			135	180	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

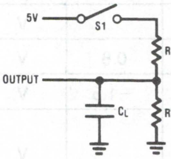
Note 3: I/O leakage as the worst case of IOZX or IIX, e.g., I_{IL} and IOZL.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage otherwise may result.

Switching Characteristics Over Operating Conditions

Symbol	Parameter		Test Conditions	Military			Commercial			Units
				Min	Typ	Max	Min	Typ	Max	
T_S	Setup Time from Input			40	20		30	20		ns
T_W	Width of Clock	High		20	7		15	7		ns
		Low		35	15		25	15		ns
T_{PD}	I0, I1 to LIRO, RILO		$C_L = 50$ pF		23	35		23	30	ns
T_{CLK}	Clock to Output		$C_L = 50$ pF		10	25		10	15	ns
T_{PZX}	Output Enable Delay		$C_L = 50$ pF		19	35		19	30	ns
T_{PX}	Output Disable Delay		$C_L = 5$ pF		15	35		15	30	ns
T_H	Hold Time			0	−15		0	−15		ns
f_{MAX}	Maximum Frequency			15.3	32		22.2	32		MHz

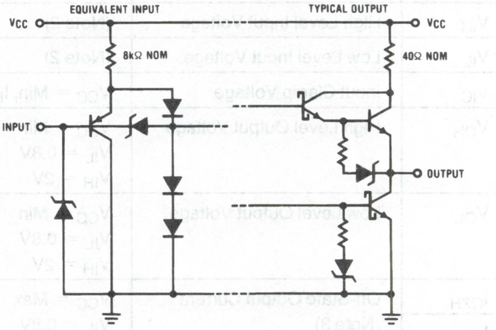
Test Load


5V
S1
R1
OUTPUT
CL
R2

MIL	COM'L
R1 = 390	R1 = 200
R2 = 750	R2 = 390

TL/L/10221-2

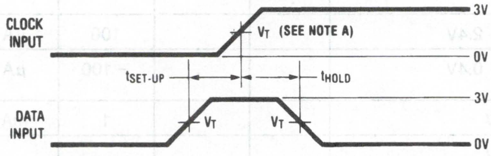
Schematic of Inputs and Outputs


EQUIVALENT INPUT
TYPICAL OUTPUT
VCC
VCC
8kΩ NOM
40Ω NOM
INPUT
OUTPUT

TL/L/10221-3

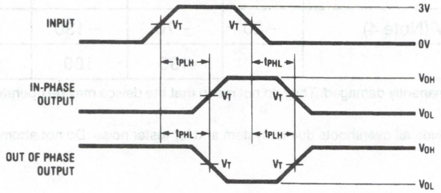
Test Waveforms

Set-Up and Hold


CLOCK INPUT
VT (SEE NOTE A)
3V
0V
tSET-UP
tHOLD
DATA INPUT
VT
VT
3V
0V

TL/L/10221-4

Propagation Delay


INPUT
VT
VT
3V
0V
tPLH
tPHL
IN-PHASE OUTPUT
VT
VT
VOH
VOL
tPHL
tPLH
OUT OF PHASE OUTPUT
VT
VT
VOH
VOL

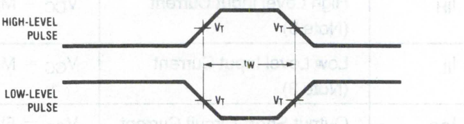
TL/L/10221-5

Note A: $V_T = 1.5V$.

Note B: C_L includes probe and jig capacitance.

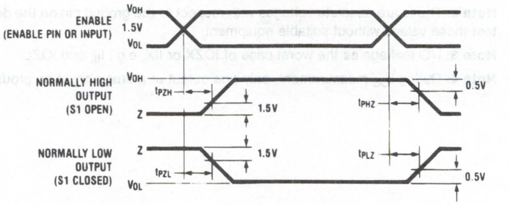
Note C: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Pulse Width


HIGH-LEVEL PULSE
VT
VT
tW
LOW-LEVEL PULSE
VT
VT

TL/L/10221-6

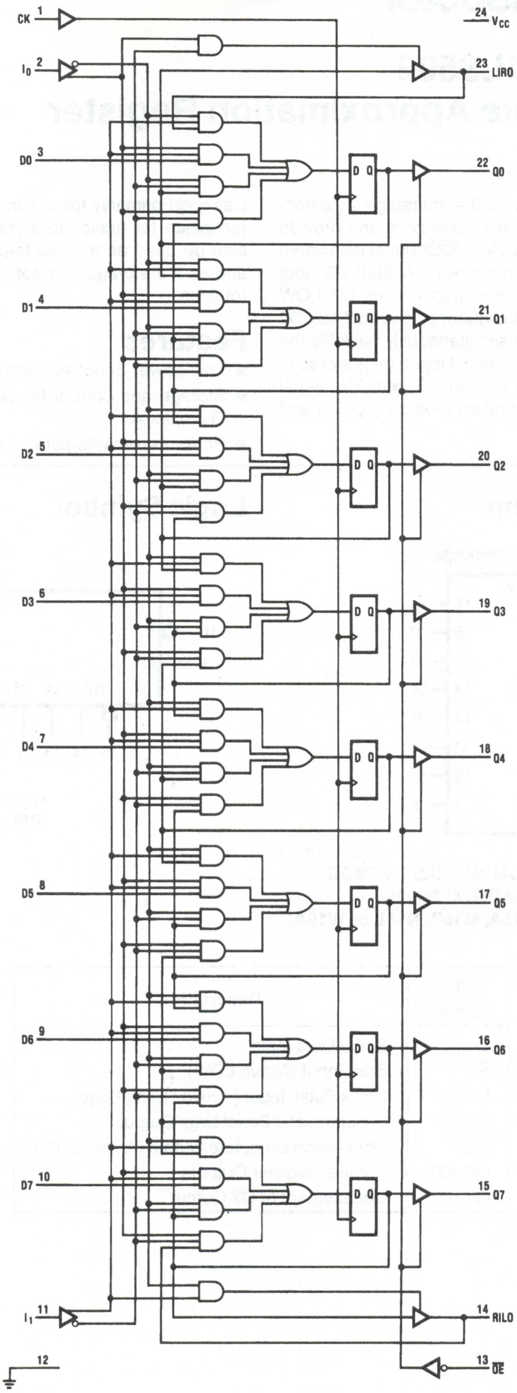
Enable and Disable


ENABLE (ENABLE PIN OR INPUT)
VOH
1.5V
VOL
NORMALLY HIGH OUTPUT (S1 OPEN)
VOH
Z
tPZH
1.5V
tPHZ
0.5V
NORMALLY LOW OUTPUT (S1 CLOSED)
Z
VOL
tPZL
1.5V
tPLZ
0.5V

TL/L/10221-7

Logic Diagram

Octal Shift Register


CK 1
I0 2
D0 3
D1 4
D2 5
D3 6
D4 7
D5 8
D6 9
D7 10
I1 11
12
24 VCC
23 LIRO
22 Q0
21 Q1
20 Q2
19 Q3
18 Q4
17 Q5
16 Q6
15 Q7
14 RILO
13 OE
D Q

TL/L/10221-8

National Semiconductor

54LS502/DM74LS502
8-Bit Successive Approximation Register

General Description

The LS502 is an 8-bit register with the interstage logic necessary to perform serial-to-parallel conversion and provide an active LOW Conversion Complete ($\overline{CC}$) signal coincident with storage of the eighth bit. An active LOW Start ($\overline{S}$) input performs synchronous initialization which forces Q7 LOW and all other outputs HIGH. Subsequent clocks shift this Q7 LOW signal downstream which simultaneously backfills the register such that the first serial data (D input) bit is stored in Q7, the second bit in Q6, the third in Q5, etc. The serial input data is also synchronized by an auxiliary flip-flop and brought out on Q_D.

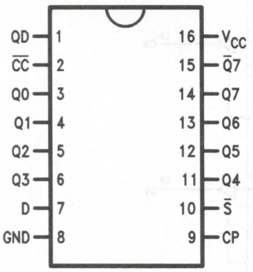
Designed primarily for use in the successive approximation technique for analog-to-digital conversion, the LS502 can also be used as a serial-to-parallel converter ring counter and as the storage and control element in recursive digital routines.

Features

- Low power Schottky version of 2502
- Storage and control for successive approximation A to D conversion
- Performs serial-to-parallel conversion

Connection Diagram

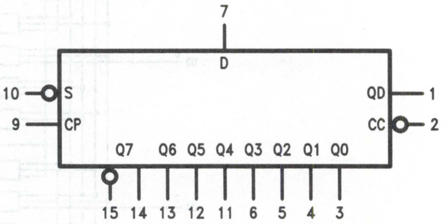
Dual-In-Line Package



TL/F/10189-1

Order Number 54LS502DMQB, 54LS502FMQB, DM74LS502WM or DM74LS502N
See NS Package Number J16A, M16B, N16E or W16A

Logic Symbol



TL/F/10189-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
D	Serial Data Input
$\overline{S}$	Start Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
Q_D	Synchronized Serial Data Output
$\overline{CC}$	Conversion Complete Output (Active LOW)
Q0–Q7	Parallel Register Outputs
$\overline{Q7}$	Complement of Q7 Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS502			DM74LS502			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW $\overline{S}$ to CP	5 5			5 5			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW $\overline{S}$ to CP	5 5			5 5			ns
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW D to CP	5 5			5 5			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW D to CP	5 5			5 5			ns
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	20 20			20 20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				65	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Note more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output loads)

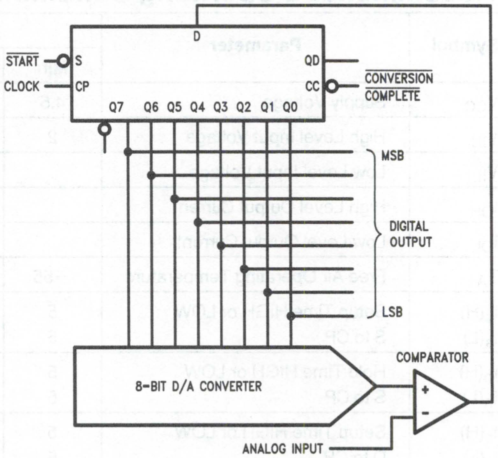
Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 15\ pF$		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	25		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n or $\overline{CC}$		35 25	ns

Functional Description

The register stages are composed of transparent RS latches arranged in master/slave pairs. The master and slave latches are enabled separately by non-overlapping complementary signals $\phi1$ and $\phi2$ derived internally from the CP input. Master latches are enabled when CP is LOW and slave latches are enabled when CP is HIGH. Information is transferred from master to slave, and thus to the outputs, by the LOW-to-HIGH transition of CP.

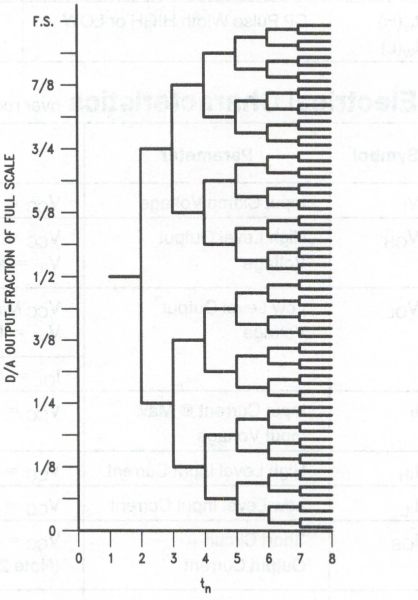
Initializing the register requires a LOW signal on $\overline{S}$ while exercising CP. With $\overline{S}$ and CP LOW, all master latches are SET (Q side HIGH). A LOW-to-HIGH CP transition, with $\overline{S}$ remaining LOW, then forces the slave latches to the condition wherein Q7 is LOW and all other register outputs, including $\overline{CC}$, are HIGH. This condition will prevail as long as $\overline{S}$ remains LOW, regardless of subsequent CP rising edge. To start the conversion process, $\overline{S}$ must return to the HIGH state. On the next CP rising edge, the information stored in the serial data input latch is transferred to Q_D and Q7, while Q6 is forced to the LOW state. On the rising edge of the next seven clocks, this LOW signal is shifted downstream, one bit at a time, while the serial data enters the register position one bit behind this LOW signal, as shown in the Truth Table. Note that after a serial data bit appears at a particular output, that register position undergoes no further changes. After the shifted LOW signal reaches $\overline{CC}$, the register is locked up and no further changes can occur until the register is initialized for the next conversion process.

Figure a shows a simplified hook-up of a LS502, a D/A converter and a comparator arranged to convert an analog input voltage into an 8-bit binary number by the successive approximation technique. *Figure b* is an idealized graph showing the various values that the D/A converter output voltage can assume in the course of the conversion. The vertical axis is calibrated in fractions of the full-scale output capability of the D/A converter and the horizontal axis represents the successive states of the Truth Table. At time t1, Q7 is LOW and Q6–Q0 are HIGH, causing the D/A output to be one-half of full scale. If the analog input voltage is greater than this voltage the comparator output (hence the D input of the LS502) will be LOW, and at times t2 the D/A output will rise to three-fourths of full scale because Q7 will remain LOW and contribute 50% while Q6 is forced LOW and contributes another 25%. On the other hand, if the analog input voltage is less than one-half of full scale, the comparator output will be HIGH and Q7 will go HIGH at t2. Q6 will still be forced LOW at t2, and the D/A output will decrease to 25% of full scale. Thus with each successive clock, the D/A output will change by smaller increments. When the conversion is completed at t9, the binary number represented by the register outputs will be the numerator of the fraction n/256, representing the analog input voltage as a fraction of the full scale output D/A converter.



TL/F/10189-4

FIGURE a.



TL/F/10189-5

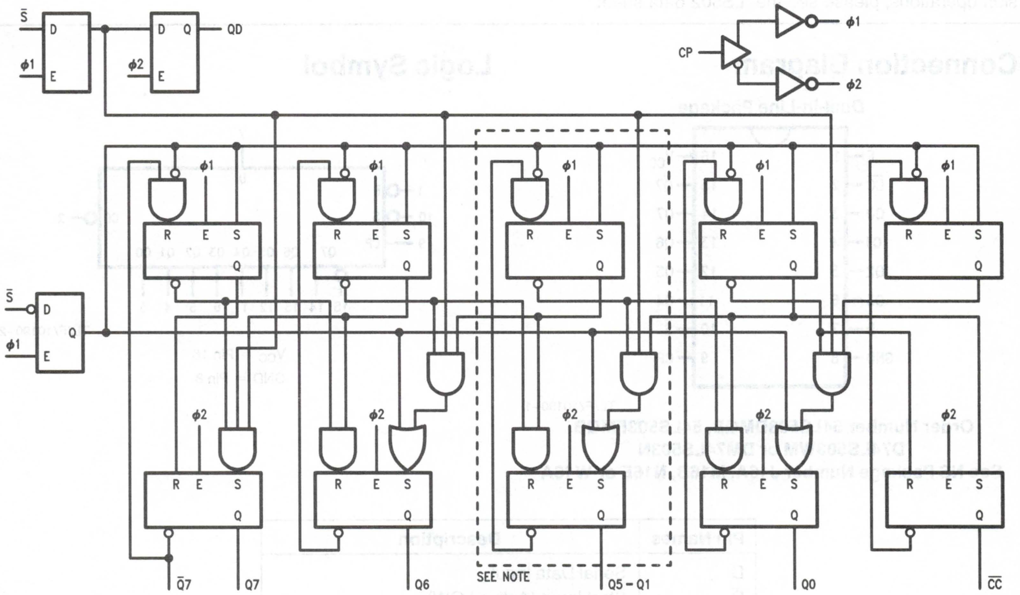
FIGURE b.

Truth Table

Time t_n	Inputs		Outputs									
	D	$\overline{S}$	Q_D	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{CC}$
0	X	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	X	L	H	H	H	H	H	H	H	H
2	D6	H	D7	D7	L	H	H	H	H	H	H	H
3	D6	H	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	H	X	D7	D6	D5	D4	D3	D2	D1	D0	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



$\overline{S}$
D
E
$\phi1$
D Q
QD
$\phi2$
CP
$\phi1$
$\phi2$
R E S
Q
D
Q
E
$\overline{Q7}$
Q7
Q6
SEE NOTE
Q5 – Q1
Q0
$\overline{CC}$

TL/F/10189-3

Note: Cell logic is repeated for register stages Q5 to Q1.

National Semiconductor

54LS503/DM74LS503
8-Bit Successive Approximation Register (with Expansion Control)

General Description

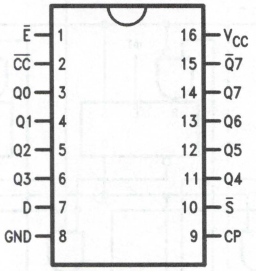
The 'LS503 register is basically the same as the 'LS502 except that it has an active LOW Enable ($\overline{E}$) input that is used in cascading two or more packages for longer word lengths. A HIGH signal on $\overline{E}$, after a START operation, forces Q7 HIGH and prevents the device from accepting serial data. With the $\overline{E}$ input of an 'LS503 connected to the $\overline{CC}$ output of a preceding (more significant) device, the 'LS503 will be inhibited until the preceding device is filled, causing its $\overline{CC}$ output to go LOW. This LOW signal then enables the 'LS503 to accept the serial data on subsequent clocks. For a description of the starting, shifting and conversion operations, please see the 'LS502 data sheet.

Features

- Performs serial-to-parallel conversion
- Expansion control for longer words
- Storage and control for successive approximation A to D conversion
- Low power Schottky version of 2503

Connection Diagram

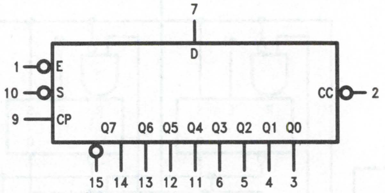
Dual-In-Line Package



TL/F/10190-1

Order Number 54LS503DMQB, 54LS503FMQB, D74LS503WM or DM74LS503N
See NS Package Number J16A, M16B, N16E or W16A

Logic Symbol



TL/F/10190-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
D	Serial Data Input
$\overline{S}$	Start Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
$\overline{E}$	Conversion Enable Input (Active LOW)
$\overline{CC}$	Conversion Complete Output (Active LOW)
Q0–Q7	Parallel Register Outputs
$\overline{Q7}$	Complement of Q7 Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS503			DM74LS503			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Voltage			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{S}$ to CP	5 5			5 5			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{S}$ to CP	5 5			5 5			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{S}$ to CP	5 5			5 5			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D to CP	5 5			5 5			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 20			20 20			ns

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				65	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

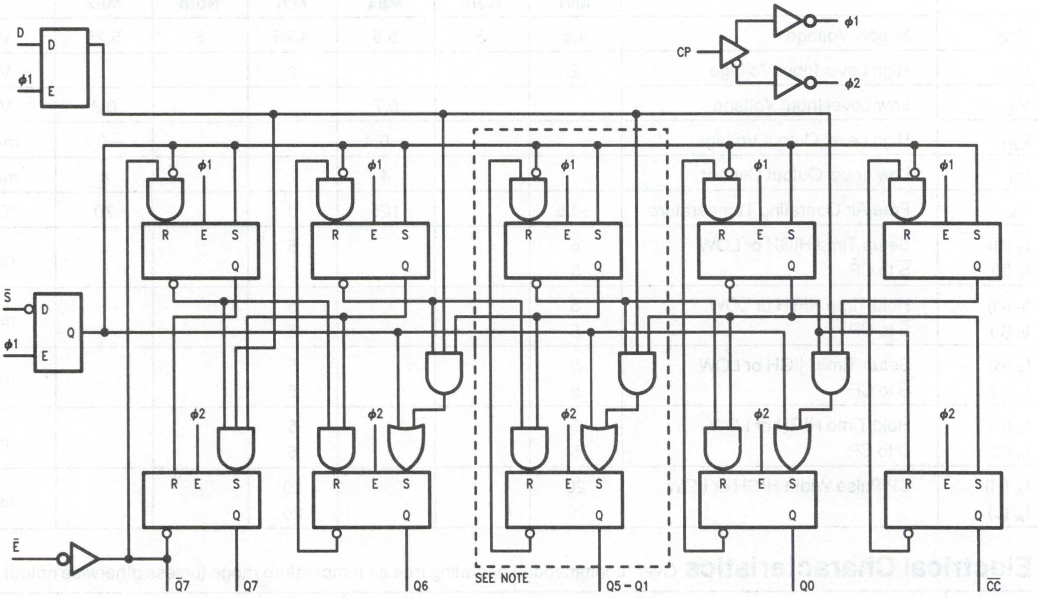
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Count Frequency	25		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Qn or $\overline{CC}$		35 25	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q7		20 24	ns

Logic Diagram

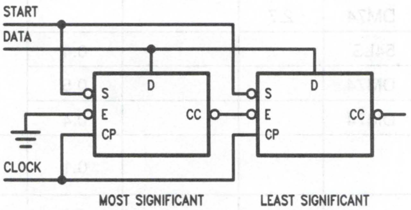


D
D
ϕ1
E
CP
ϕ1
ϕ2
ϕ1
R
E
S
Q
ϕ2
$\overline{S}$
D
Q
ϕ1
E
$\overline{E}$
$\overline{Q}$7
Q7
Q6
SEE NOTE
Q5 - Q1
Q0
$\overline{CC}$

TL/F/10190-3

Note: Cell logic is repeated for register stages Q5 to Q1.

Connection for Longer Word Lengths



START
DATA
S
D
E
CC
CP
S
D
E
CC
CP
CLOCK
MOST SIGNIFICANT
LEAST SIGNIFICANT

TL/F/10190-4

National Semiconductor

DM74LS533
Octal Transparent Latch with TRI-STATE® Outputs

General Description

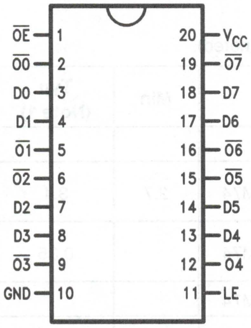
The 'LS533 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{\text{OE}}$) is LOW. When $\overline{\text{OE}}$ is HIGH the bus output is in the high impedance state. The 'LS533 is the same as the 'LS373, except that the outputs are inverted. For detailed specifications please see the 'LS373 data sheet, but note that the propagation delays from data to output are 5.0 ns longer for the 'LS533 than for the 'LS373.

Features

- Eight latches in a single package
- TRI-STATE outputs for bus interfacing

Connection Diagram

Dual-In-Line Package

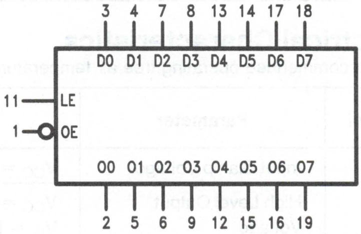


$\overline{\text{OE}}$ 1
$\overline{\text{O0}}$ 2
D0 3
D1 4
$\overline{\text{O1}}$ 5
$\overline{\text{O2}}$ 6
D2 7
D3 8
$\overline{\text{O3}}$ 9
GND 10
20 V_{CC}
19 $\overline{\text{O7}}$
18 D7
17 D6
16 $\overline{\text{O6}}$
15 $\overline{\text{O5}}$
14 D5
13 D4
12 $\overline{\text{O4}}$
11 LE

TL/F/9811-1

Order Number DM74LS533WM or DM74LS533N
See NS Package Number M20B or N20A

Logic Symbol



3 4 7 8 13 14 17 18
D0 D1 D2 D3 D4 D5 D6 D7
11 LE
1 OE
O0 O1 O2 O3 O4 O5 O6 O7
2 5 6 9 12 15 16 19

TL/F/9811-2

V_{CC} = Pin 20
GND = Pin 10

Pin Names	Description
D0, D7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{\text{OE}}$	Output Enable Input (Active LOW)
$\overline{\text{O0}}$–$\overline{\text{O7}}$	Complementary TRI-STATE Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS533			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM74	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM74		0.35	0.5	V
		I_{OL} = 12 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM74	−20		−100	mA
I_{CCZ}	Supply Current	V_{CC} = Max				46	mA
I_{OZL}	TRI-STATE Output Off Current LOW	V_{CC} = V_{CCH} V_{OZL} = 0.4V				−20.0	μA
I_{OZH}	TRI-STATE Output Off Current HIGH	V_{CC} = V_{CCH} V_{OZH} = 2.7V				20.0	μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF R_L = 2 kΩ		Units
		Min	**Max**	
t_{PLH} T_{PHL}	Propagation Delay Data to $\overline{Q}_x$		32 23	ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{Q}_x$		36 25	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}$ to $\overline{Q}_x$		22 2	ns
t_{PHZ} t_{PLZ}	Output Enable Time $\overline{OE}$ to $\overline{Q}_x$		34 27	ns

National Semiconductor

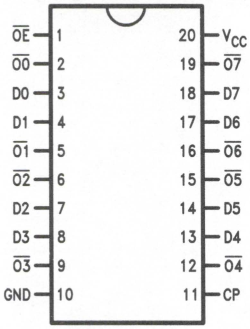
DM74LS534
Octal D-Type Flip-Flop (With TRI-STATE® Outputs)

General Description

The 'LS534 is a high speed, low power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus oriented applications. A buffered Clock (CP) and Output Enable ($\overline{\text{OE}}$) is common to all flip-flops. The 'LS534 is the same as the 'LS374 except that the outputs are inverted.

Connection Diagram

Dual-In-Line Package

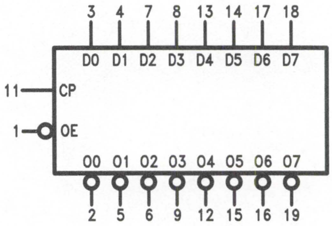


OE
1
O0
2
D0
3
D1
4
O1
5
O2
6
D2
7
D3
8
O3
9
GND
10
VCC
20
O7
19
D7
18
D6
17
O6
16
O5
15
D5
14
D4
13
O4
12
CP
11

TL/F/9812–1

Order Number DM74LS534WM or DM74LS534N
See NS Package Number M20B or N20A

Logic Symbol



3
4
7
8
13
14
17
18
D0
D1
D2
D3
D4
D5
D6
D7
11
CP
1
OE
O0
O1
O2
O3
O4
O5
O6
O7
2
5
6
9
12
15
16
19

TL/F/9812–2

V_{CC} = Pin 20
GND = Pin 10

Pin Name	Description
D0–D7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{\text{OE}}$	TRI-STATE Output Enable Input (Active LOW)
$\overline{\text{O}}$0–$\overline{\text{O}}$7	Complementary TRI-STATE Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS534			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Current			−2.6	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to $\overline{CP}$	20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to $\overline{CP}$	0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	15 15			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max V_{IH} = Min	2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 12 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−20	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max			20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)		45		mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output loads)

Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 45\ pF$		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	35		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		28 28	ns
t_{PZH} t_{PZL}	Output Enable Time		28 28	ns
t_{PHZ} t_{PLZ}	Output Disable Time		20 25	ns

Functional Description

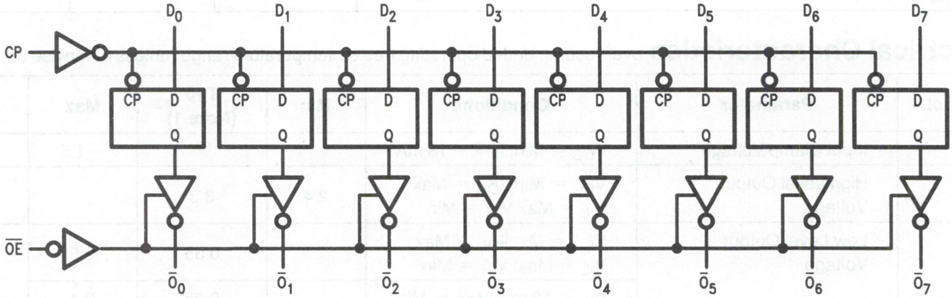
The '534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transistion. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	OE	O_n
H	↗	L	L
L	↗	L	H
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram


CP
D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
CP
D
Q
$\overline{OE}$
$\overline{O}_0$
$\overline{O}_1$
$\overline{O}_2$
$\overline{O}_3$
$\overline{O}_4$
$\overline{O}_5$
$\overline{O}_6$
$\overline{O}_7$

TL/F/9812-3

National Semiconductor

DM74LS540
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

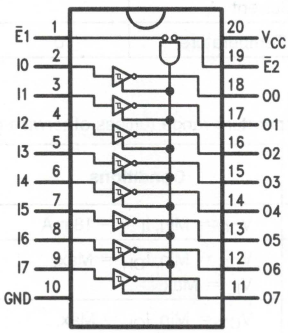
The DM74LS540 is similar in function to the 'LS240, except that the inputs and outputs are on opposite sides of the package (see Connection Diagram). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

Features

- Hysteresis at inputs to improve noise margin
- PNP inputs reduce loading
- TRI-STATE outputs drive bus lines
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors
- Fully TTL and CMOS compatible

Connection Diagram

Dual-In-Line Package



TL/F/9813-1

Order Number DM74LS540WM or DM74LS540N
See NS Package Number M20B or N20A

Pin Name	Description
Ē1, Ē2	Output Enable (Active Low)
I0–7	Data Inputs
O0–7	Data Outputs

Truth Table

Inputs			Outputs
E1	E2	D	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS540			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−3	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−50		−225	mA
I_{CC}	Supply Current	V_{CC} = Max			50	mA
I_{OZH}	TRI-STATE Output Off Current High	V_{CC} = V_{CCH}, V_{OZH} = 2.7V			20	μA
I_{OZL}	TRI-STATE Output Off Current Low	V_{CC} = V_{CCH}, V_{OZL} = 0.4V			−20	μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at at time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 or Test Waveforms and Output Loading)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH} t_{PHL}	Propagation Delay Data to Output	$C_L = 50$ pF		14 18	ns
t_{PZH} t_{PZL}	Output Enable Time	$R_L = 667\Omega$, $C_L = 50$ pF		23 30	ns
t_{PLZ} t_{PHZ}	Output Disable Time	$R_L = 667\Omega$, $C_L = 50$ pF		25 18	ns

*DC limits apply over operating temperature range; AC limits apply at $T_A = +25°$ and $V_{CC} = +5.0V$.

National Semiconductor

DM74LS563
Octal D-Type Latch with TRI-STATE® Outputs

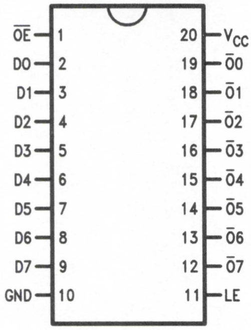
General Description

The ’LS563 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

This device is functionally indentical to the ’LS573, but has inverted outputs.

Connection Diagram

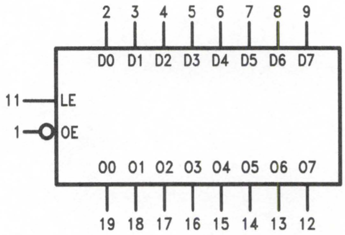
Dual-In-Line Package


$\overline{OE}$ 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 V_{CC}
19 $\overline{O}0$
18 $\overline{O}1$
17 $\overline{O}2$
16 $\overline{O}3$
15 $\overline{O}4$
14 $\overline{O}5$
13 $\overline{O}6$
12 $\overline{O}7$
11 LE

TL/F/10214–1

Order Number DM74LS563WM or DM74LS563N
See NS Package Number M20B or N20A

Logic Symbol


2 3 4 5 6 7 8 9
D0 D1 D2 D3 D4 D5 D6 D7
11 LE
1 OE
O0 O1 O2 O3 O4 O5 O6 O7
19 18 17 16 15 14 13 12

TL/F/10214–2

V_{CC} = Pin 20
GND = Pin 10

Pin Names	Description
D0–D7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
$\overline{O}0$–$\overline{O}7$	TRI-STATE Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS563			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2.6	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW Dn to LE	0 0			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW Dn to LE	10 10			ns
t_w (H) t_w (L)	LE Pulse Width HIGH or LOW	15 15			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 12 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−20	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max			20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			40	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Switching Characteristics

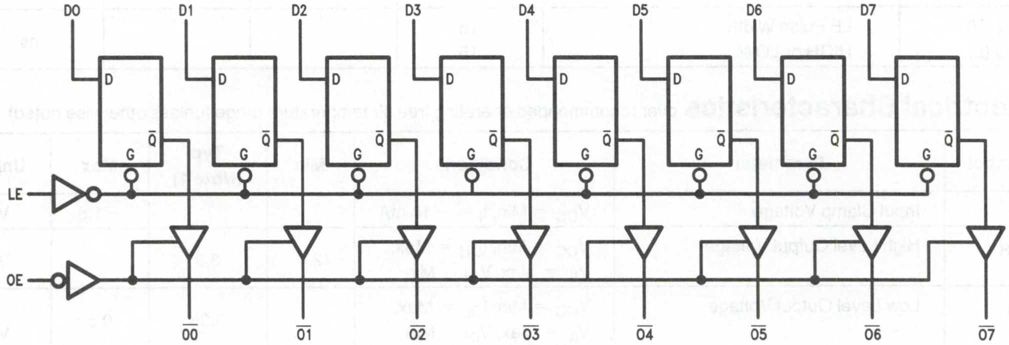
$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output loading)

Symbol	Parameter	$R_L = 2\ k\Omega$ $C_L = 15\ pF$		Units
		Min	**Max**	
t_{PLH} t_{PHL}	Propagation Delay Dn to On		23 25	ns
t_{PLH} t_{PHL}	Propagation Delay LE to On		35 35	ns
t_{PZH} t_{PZL}	Output Enable Time		28 36	ns
t_{PHZ} t_{PLZ}	Output Disable Time		20 25	ns

Functional Description

The 'LS563 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram


D0
D1
D2
D3
D4
D5
D6
D7
D
$\overline{Q}$
G
LE
OE
$\overline{O0}$
$\overline{O1}$
$\overline{O2}$
$\overline{O3}$
$\overline{O4}$
$\overline{O5}$
$\overline{O6}$
$\overline{O7}$

TL/F/10214-3

National Semiconductor

DM74LS564
Octal D-Type Flip-Flop (with TRI-STATE® Outputs)

General Description

The 'LS564 is a high speed low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition

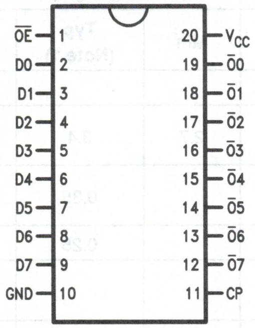
This device is functionally identical to the 'LS574, but has inverted outputs. For complete discussions of operations, truth tables, AC and DC electrical specifications, refer to the 'LS374 data sheet.

Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'LS574
- Input clamp diodes limit high speed termination effects
- Fully TTL and CMOS compatible

Connection Diagram

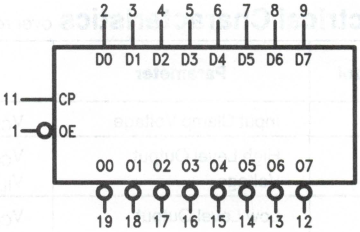
Dual-In-Line Package


$\overline{OE}$ 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 V_{CC}
19 $\overline{O}0$
18 $\overline{O}1$
17 $\overline{O}2$
16 $\overline{O}3$
15 $\overline{O}4$
14 $\overline{O}5$
13 $\overline{O}6$
12 $\overline{O}7$
11 CP

TL/F/10191-1

Order Number DM74LS564WM or DM74LS564N
See NS Package Number M20B or N20A

Logic Symbol


2 3 4 5 6 7 8 9
D0 D1 D2 D3 D4 D5 D6 D7
11 CP
1 OE
O0 O1 O2 O3 O4 O5 O6 O7
19 18 17 16 15 14 13 12

TL/F/10191-2

V_{CC} = Pin 20
GND = Pin 10

Pin Names	Description
D0–D7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	TRI-STATE® Output Enable Input (Active LOW)
$\overline{O}0$–$\overline{O}7$	TRI-STATE Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS564 Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2.6	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 12 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max			60	mA
I_{OZH}	TRI-STATE Output OFF Current HIGH	V_{CC} = V_{CCH}, V_{OZH} = 2.7V			20	μA
I_{OZL}	TRI-STATE Output OFF Current LOW	V_{CC} = V_{CCH}, V_{OZL} = 0.4V			−20	μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for test waveforms and output load)

Symbol	Parameter	Min	Max	Units
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}n$		28 28	ns
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ to $\overline{O}n$		28 28	ns
t_{PHZ} t_{PLZ}	Enable Time $\overline{OE}$ to $\overline{O}n$		20 25	ns
t_s	Setup Time Dn to CP	5		ns
t_h	Hold Time Dn to CP	5		ns
t_w (H) t_w (L)	Pulse Width (HIGH/LOW) CP	20 10		ns

National Semiconductor

DM74LS573
Octal D-Type Latch (with TRI-STATE® Outputs)

General Description

The 'LS573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

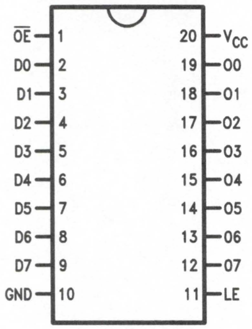
This device is functionally identical to the 'LS373, but has different pinouts. For truth tables, discussion of operations and AC and DC specifications, please refer to the 'LS373 data sheet.

Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'LS373
- Input clamp diodes limit high speed termination effects
- Fully TTL and CMOS compatible

Connection Diagram

Dual-In-Line Package

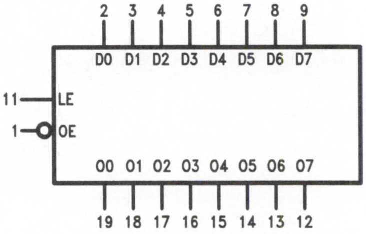


$\overline{OE}$ 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 V_{CC}
19 O0
18 O1
17 O2
16 O3
15 O4
14 O5
13 O6
12 O7
11 LE

TL/F/9814-1

Order Number DM74LS573WM or DM74LS573N
See NS Package Number M20B or N20A

Logic Symbol



2 3 4 5 6 7 8 9
D0 D1 D2 D3 D4 D5 D6 D7
11 LE
1 OE
O0 O1 O2 O3 O4 O5 O6 O7
19 18 17 16 15 14 13 12

TL/F/9814-2

V_{CC} = Pin 20
GND = Pin 10

Pin Names	Description
D0–D7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O0–O7	TRI-STATE Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Input Current			−2.6	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max			50	mA
I_{OZH}	TRI-STATE Output off Current High	V_{CC} = V_{CCH} V_{OZH} = 2.7V			20	μA
I_{OZL}	TRI-STATE Output off Current Low	V_{CC} = V_{CCH} V_{OZL} = 0.4V			−20	μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (see Section 1 for Test Waveforms and output loading)

Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 15\ pF$		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Data to Q		27 18	ns
t_{PLH} t_{PHL}	Propagation Delay LE to Q		36 25	ns
t_{PZH} t_{PZL}	TRI-STATE Enable Time $\overline{OE}$ to Q		20 25	ns
t_{PHZ} t_{PLZ}	TRI-STATE Enable Time $\overline{OE}$ to Q		20 25	ns
$t_s(H)$ $t_s(L)$	Setup Time (High/Low) Data to LE	3 7		ns
$t_h(H)$ $t_h(L)$	Hold Time (High/Low) Data to LE	3 7		ns
$t_w(H)$	Pulse Width (High) Data to LE	15		ns

National Semiconductor

DM74LS574
Octal D-Type Flip-Flop (with TRI-STATE® Outputs)

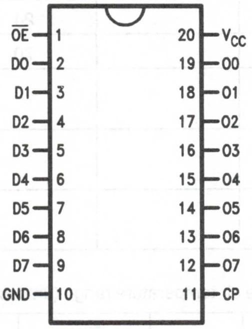
General Description

The 'LS574 is a high speed low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 'LS374 except for the pinouts.

Connection Diagram

Dual-In-Line Package

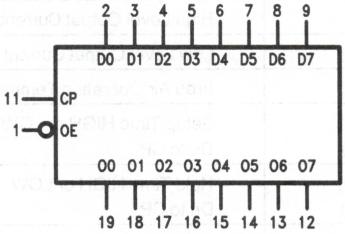


$\overline{OE}$ 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
GND 10
20 V_{CC}
19 O0
18 O1
17 O2
16 O3
15 O4
14 O5
13 O6
12 O7
11 CP

TL/F/9815-1

Order Number DM74LS574WM or DM74LS574N
See NS Package Number M20B or N20A

Logic Symbol



2 3 4 5 6 7 8 9
D0 D1 D2 D3 D4 D5 D6 D7
11 CP
1 OE
O0 O1 O2 O3 O4 O5 O6 O7
19 18 17 16 15 14 13 12

TL/F/9815-2

V_{CC} = Pin 20
GND = Pin 10

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions $V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	DM74LS574			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2.6	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW Dn to CP	20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW Dn to CP	0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	15 15			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 12 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−20	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max			20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−20	μA

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
I_{OS}	Short Circuit (Note 2) Output Current	V_{CC} = Max	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			45	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs at 0.4V.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for test waveforms and output load)

Symbol	Parameter	R_L = 2 kΩ, C_L = 45 pF		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	35		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to On		28 28	ns
t_{PZH} t_{PZL}	Output Enable Time		28 28	ns
t_{PHZ} t_{PLZ}	Output Disable Time		20 25	ns

Functional Description

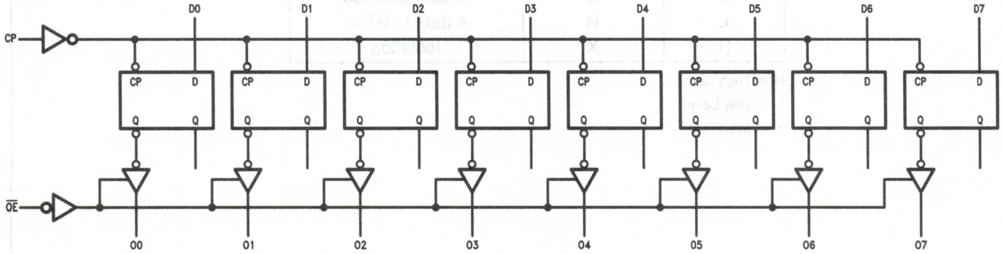
The LS574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Outputs Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedence state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs		Outputs	
Dn	CP	OE	On
H	↑	L	H
L	↑	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/9815-3

National Semiconductor

DM74LS645 Octal Bus Transceivers

General Description

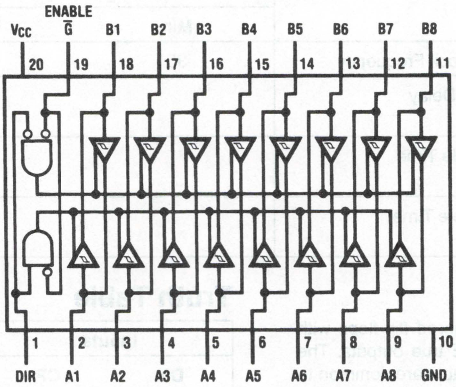
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

Features

- Bi-directional bus transceivers in high-density 20-pin packages
- Hysteresis at bus inputs improves noise margins
- TRI-STATE® outputs

Connection Diagram

Dual-In-Line Package


ENABLE
V_{CC}
$\overline{G}$
B1
B2
B3
B4
B5
B6
B7
B8
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
DIR
A1
A2
A3
A4
A5
A6
A7
A8
GND

TL/F/9056–1

Order Number DM74LS645WM or DM74LS645N
See NS Package Number M20B or N20A

Function Table

Control Inputs		'LS645
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High Level
L = Low Level
X = Irrelevant

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−55°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS645			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage (Note 1)	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.6	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (Note 2)			Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = 18 mA					−1.5	V
H_{YS}	Hysteresis ($V_{T+} - V_-$) A or B Input	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max		I_{OH} = −3 mA	2.4	3.4		V
				I_{OH} = Max	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max		I_{OL} = 12 mA		0.25	0.4	V
				I_{OL} = 24 mA		0.35	0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, G at 2V, V_O = 2.7V					20	µA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = Max, G at 2V V_O = 0.4V					−400	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	A or B	V_I = 5.5V			0.1	mA
			DIR or G	V_I = 7V			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_{IH} = 2.7					20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IL} = 0.4V					−0.4	mA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max			−40		−225	mA
I_{CC}	Total Supply Current	Outputs High		V_{CC} = Max, Outputs Open		48	70	mA
		Outputs Low				62	90	
		Outputs at Hi-Z				64	95	

Note 1: Voltage values are with respect to the network ground terminal.

Note 2: For conditions shown as Min or Max, use the appropriate value specified under Recommended Operating Conditions.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

Symbol	Parameter	From (Input) To (Output)	$R_L = 667\Omega$				Units
			$C_L = 45$ pF		$C_L = 5$ pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A to B		15			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to B		15			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to A		15			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to A		15			ns
t_{PZL}	Output Enable Time to Low Level	$\overline{G}$ to A		40			ns
t_{PZH}	Output Enable Time to High Level	$\overline{G}$ to A		40			ns
t_{PZL}	Output Enable Time to Low Level	$\overline{G}$ to B		40			ns
t_{PZH}	Output Enable Time to High Level	$\overline{G}$ to B		40			ns
t_{PLZ}	Output Disable Time to Low Level	$\overline{G}$ to A				25	ns
t_{PHZ}	Output Disable Time to High Level	$\overline{G}$ to A				25	ns
t_{PLZ}	Output Disable Time to Low Level	$\overline{G}$ to B				25	ns
t_{PHZ}	Output Disable Time to High Level	$\overline{G}$ to B				25	ns

National Semiconductor

54LS670/DM54LS670/DM74LS670 TRI-STATE® 4-by-4 Register Files

General Description

These register files are organized as 4 words of 4 bits each, and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits writing into one location, and reading from another word location, simultaneously.

Four data inputs are available to supply the word to be stored. Location of the word is determined by the write select inputs A and B, in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and go into the high impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data entry addressing separate from data read addressing and individual sense line — eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 ns typical) and the read time (24 ns typical). The register file has a non-volatile readout in that data is not lost when addressed.

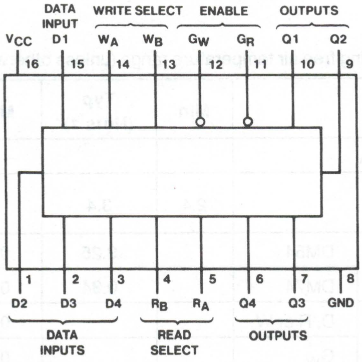
All inputs (except read enable and write enable) are buffered to lower the drive requirements to one normal Series 54LS/74LS load, and input clamping diodes minimize switching transients to simplify system design. High speed, double ended AND-OR-INVERT gates are employed for the read-address function and have high sink current, TRI-STATE outputs. Up to 128 of these outputs may be wire-AND connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

Features

- Alternate Military/Aerospace device (54LS670) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.
- For use as:
  - Scratch pad memory
  - Buffer storage between processors
  - Bit storage in fast multiplication designs
- Separate read/write addressing permits simultaneous reading and writing
- Organized as 4 words of 4 bits
- Expandable to 512 words of n-bits
- TRI-STATE versions of DM54LS170/DM74LS170
- Fast access times 20 ns typ

Connection Diagram

Dual-In-Line Package



TL/F/6436–1

Order Number 54LS670DMQB, 54LS670FMQB, 54LS670LMQB, DM54LS670J, DM54LS670W, DM74LS670M or DM74LS670N
See NS Package Number E20A, J16A, M16A, N16A or W16A

Function Tables

WRITE TABLE (SEE NOTES A, B, AND C)

Write Inputs			Word			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ TABLE (SEE NOTES A AND D)

Read Inputs			Outputs			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

Note A: H = High Level, L = Low Level, X = Don't Care, Z = High Impedance (Off).

Note B: (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

Note C: Q_0 = The level of Q before the indicated input conditions were established.

Note D: W0B1 = The first bit of word 0, etc.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS670			DM74LS670			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
t_W	Write Enable Pulse Width (Note 3)		25			25			ns
t_{SU}	Setup Time (Notes 1 & 3)	Data	10			10			ns
		W_A, W_B	15			15			
t_H	Hold Time (Notes 1 & 3)	Data	15			15			ns
		W_A, W_B	5			5			
t_{LATCH}	Latch Time for New Data (Notes 2 & 3)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: Times are with respect to the Write-Enable input. Write-Select time will protect the data written into the previous address. If protection of data in the previous address, t_{SETUP} (W_A, W_B) can be ignored. As any address selection sustained for the final 30 ns of the Write-Enable pulse and during t_H (W_A, W_B) will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

Note 2: Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

Note 3: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18\text{ mA}$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$		2.4	3.4		V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $I_{OL} = \text{Max}, V_{IH} = \text{Min}$	DM54		0.25	0.4	V
			DM74		0.34	0.5	
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ $V_I = 7V$	D, R or W			0.1	mA
			G_W			0.2	
			G_R			0.3	
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7V$	D, R or W			20	μA
			G_W			40	
			G_R			60	

Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	D, R, or W			−0.4	mA
			G_W			−0.8	
			G_R			−1.2	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	50	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Read Select to Q		40		50	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Read Select to Q		45		55	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Write Enable to Q		45		55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Write Enable to Q		50		60	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Q		45		55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Q		40		50	ns
t_{PZH}	Output Enable Time to High Level Output	Read Enable to Any Q		35		45	ns
t_{PZL}	Output Enable Time to Low Level Output	Read Enable to Any Q		40		50	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 4)	Read Enable to Any Q		50			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 4)	Read Enable to Any Q		35			ns

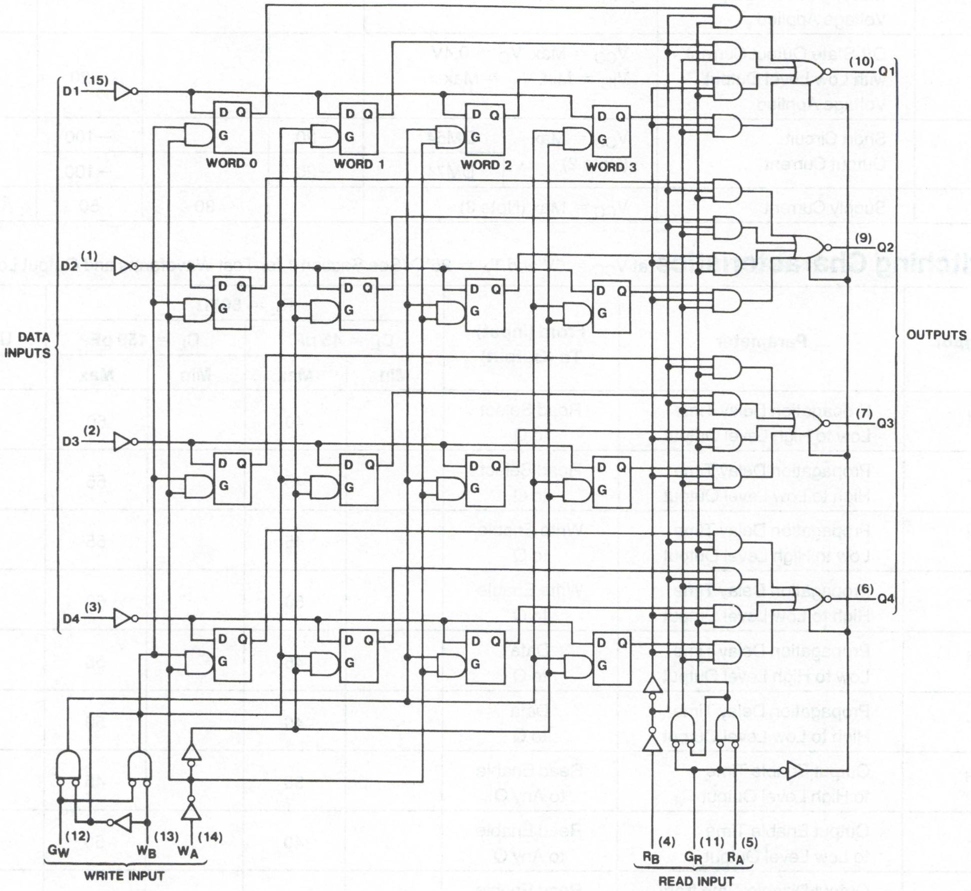
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with 4.5V applied to all DATA inputs and both ENABLE inputs, all ADDRESS inputs are grounded and all outputs are open.

Note 4: C_L = 5 pF.

Logic Diagram


D1 (15)
D2 (1)
D3 (2)
D4 (3)
DATA INPUTS
D Q
G
WORD 0
WORD 1
WORD 2
WORD 3
(10) Q1
(9) Q2
(7) Q3
(6) Q4
OUTPUTS
(12) GW
(13) WB
(14) WA
WRITE INPUT
(4) RB
(11) GR
(5) RA
READ INPUT

TL/F/6436-2

National Semiconductor

DM74LS952
Dual Rank 8-Bit TRI-STATE® Shift Registers

General Description

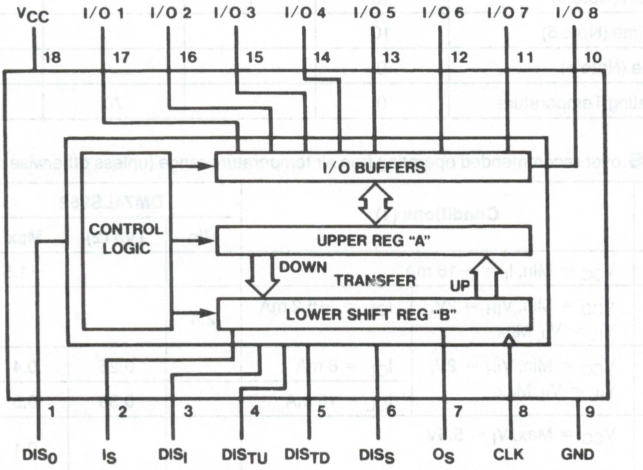
These circuits are TRI-STATE, edge-triggered, 8-bit I/O registers in parallel with 8-bit serial shift registers which are capable of operating in any of the following modes: parallel load from I/O pins to register "A", parallel transfer down from register "A" to serial shift register "B", parallel transfer up from shift register "B" to register "A", serial shift of register "B", synchronously clear. Since the registers are edge-triggered by the positive transition of the clock, the control lines which determine the mode or operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

Features

- Registers are edge-triggered by the positive transition of the clock
- All inputs are PNP transistors
- Input disable dominates over output disable
- Output high impedance state does not impede any other mode of operation
- 8-bit I/O pins are TRI-STATE buffers
- Typical shift frequency is 36 MHz
- Typical power dissipation is 305 mW
- All control inputs are active when in an "L" logic state
- Devices can be cascaded into N-bit word

Connection Diagram

Dual-In-Line Package



V_{CC}
I/O 1
I/O 2
I/O 3
I/O 4
I/O 5
I/O 6
I/O 7
I/O 8
18
17
16
15
14
13
12
11
10
I/O BUFFERS
CONTROL LOGIC
UPPER REG "A"
DOWN
TRANSFER
UP
LOWER SHIFT REG "B"
1
2
3
4
5
6
7
8
9
DIS_O
I_S
DIS_I
DIS_{TU}
DIS_{TD}
DIS_S
O_S
CLK
GND

TL/F/6437-1

Top View

Order Number DM74LS952N
See NS Package Number N18A

Pin Description

DIS_O—Output disable
I_S—Serial input
DIS_I—Input disable
DIS_{TU}—Transfer up disable
DIS_{TD}—Transfer down disable
DIS_S—Shift disable
O_S—Serial output
CLK—Clock
GND—Ground
I/O 1 . . . I/O 8—8-bit I/O pins
V_{CC}—Supply Voltage

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS952			Units
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High-Level Input Voltage	2			V
V_{IL}	Low-Level Input Voltage			0.8	V
I_{OH}	High-Level Output Current			−5.2	mA
I_{OL}	Low-Level Output Current			16	mA
f_{CLOCK}	Clock Frequency (Note 5)	0		25	MHz
Clock Pulse	High Pulse Width (Note 5)	25	17		ns
	Low Pulse Width (Note 5)	15	7		ns
$t_{SET\text{-}UP}$	Data Set-Up Time (Note 5)	10			ns
t_{HOLD}	Data Hold Time (Note 5)	0			ns
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (1)		DM74LS952			Units
				Min	Typ (2)	Max	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = V_{IL} Max	I_{OH} = −5.2 mA	2.4			V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = V_{IL} Max	I_{OL} = 8 mA		0.25	0.4	V
			I_{OL} = 16 mA		0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4V				−50	µA
I_{OS}	Short-Circuit Output Current	V_{CC} = Max (3)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (4)			61	99	mA
I_{OFF}	TRI-STATE I/O Current	V_{CC} = Max, V_{IH} = 2V	V_O = 2.4V			20	µA
			V_O = 0.4V			−20	µA

Note 1: For conditions shown as min or max, use the appropriate value specified under recommended operating conditions.

Note 2: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

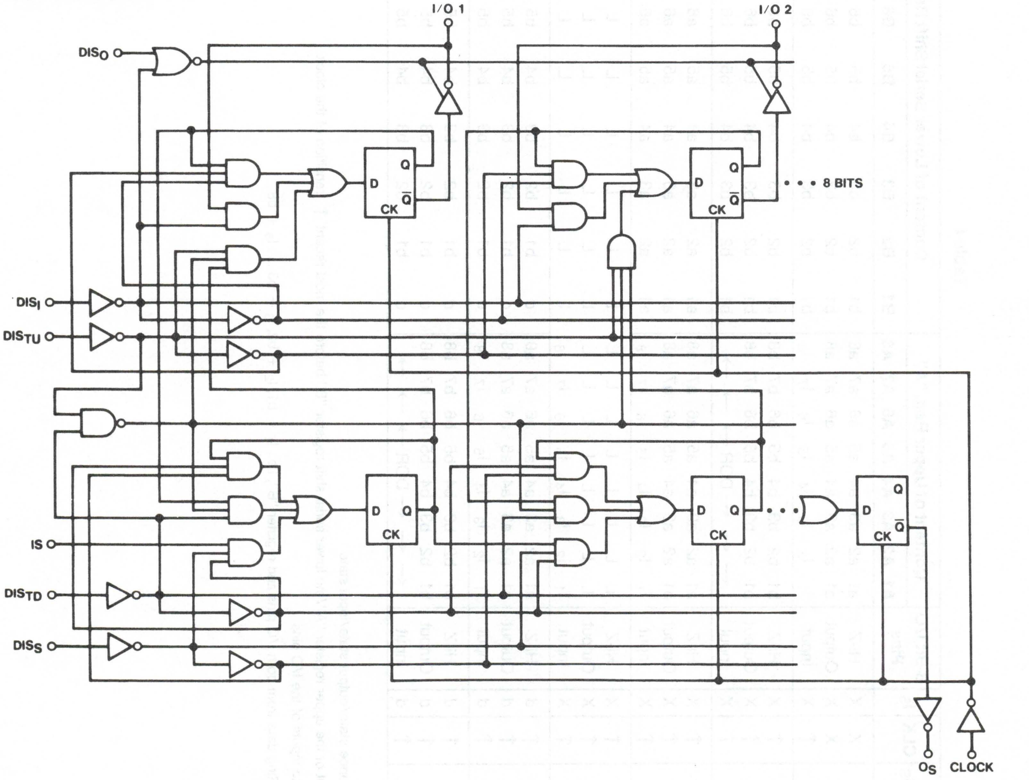
Note 4: I_{CC} is measured with serial output open, the clock and shift disable input at 2.4V. All other control inputs and I/O pins grounded.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	C_L = 15 pF, R_L = 1 kΩ	25		MHz
t_{PLH}	Propagation Delay Time, Low-to-High-Level from Clock to Any Outputs		7	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level from Clock to Any Output		10	48	ns
t_{ENABLE}	Enable Time from Any Control Inputs		5	24	ns
$t_{DISABLE}$	Disable Time from Any Control Inputs		6	27	ns
t_{PZH}	Output Enable Time to High Level		5	23	ns
t_{PZL}	Output Enable to Low Level		4	18	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF, R_L = 1 kΩ	5	23	ns
t_{PLZ}	Output Disable Time from Low Level		6	27	ns

Logic Diagram



TL/F/6437-2

Function Table

Table I

DIS_O	DIS_I	DIS_{TU}	DIS_{TD}	DIS_S	CLK	I_S	8-Bit I/O Pins	Content of Upper Reg. "A"								Content of Lower Serial Shift Reg. "B"								O_S	Comments
								A1	A2	A3	A4	A5	A6	A7	A8	B1	B2	B3	B4	B5	B6	B7	B8		
H	H	H	H	H	X	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Stable state
L	H	H	H	H	X	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	H	H	H	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Entering data from I/O to reg. "A"
H	H	L	H	H	↑	X	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Transfer data up from reg. "B" to reg. "A"
L	H	L	H	H	↑	X	Output	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	L	H	H	↑	X	Input	← ← ← DOR → → →								b1	b2	b3	b4	b5	b6	b7	b8	b8	Reg. "A" will OR data from I/O to reg. "B"
H	H	H	L	X	↑	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Transfer data down from reg. "A" to reg. "B"
L	H	H	L	X	↑	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	
X	L	H	L	X	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Entering data and transfer down
H	H	L	L	X	↑	X	Hi-Z	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	(1) Synchronously clear both registers to
L	H	L	L	X	↑	X	Output	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	(2) logic "L" level
X	L	L	L	X	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	L	L	L	L	L	L	L	L	L	(3) Enter data to reg. "A" clear reg. "B"
H	H	H	H	L	↑	d	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	Serial shifting in the lower reg. "B"
L	H	H	H	L	↑	d	Output	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	H	H	L	↑	d	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	d	b1	b2	b3	b4	b5	b6	b7	b7	Entering data and serial shifting
H	H	L	H	L	↑	d	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	Transfer up and serial shifting
L	H	L	H	L	↑	d	Output	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	L	H	L	↑	d	Input	← ← ← DOR → → →								d	b1	b2	b3	b4	b5	b6	b7	b7	DOR function and serial shifting

X ≡ Don't Care

Hi-Z/Output/Input/ ≡ High impedance state/output state/input state

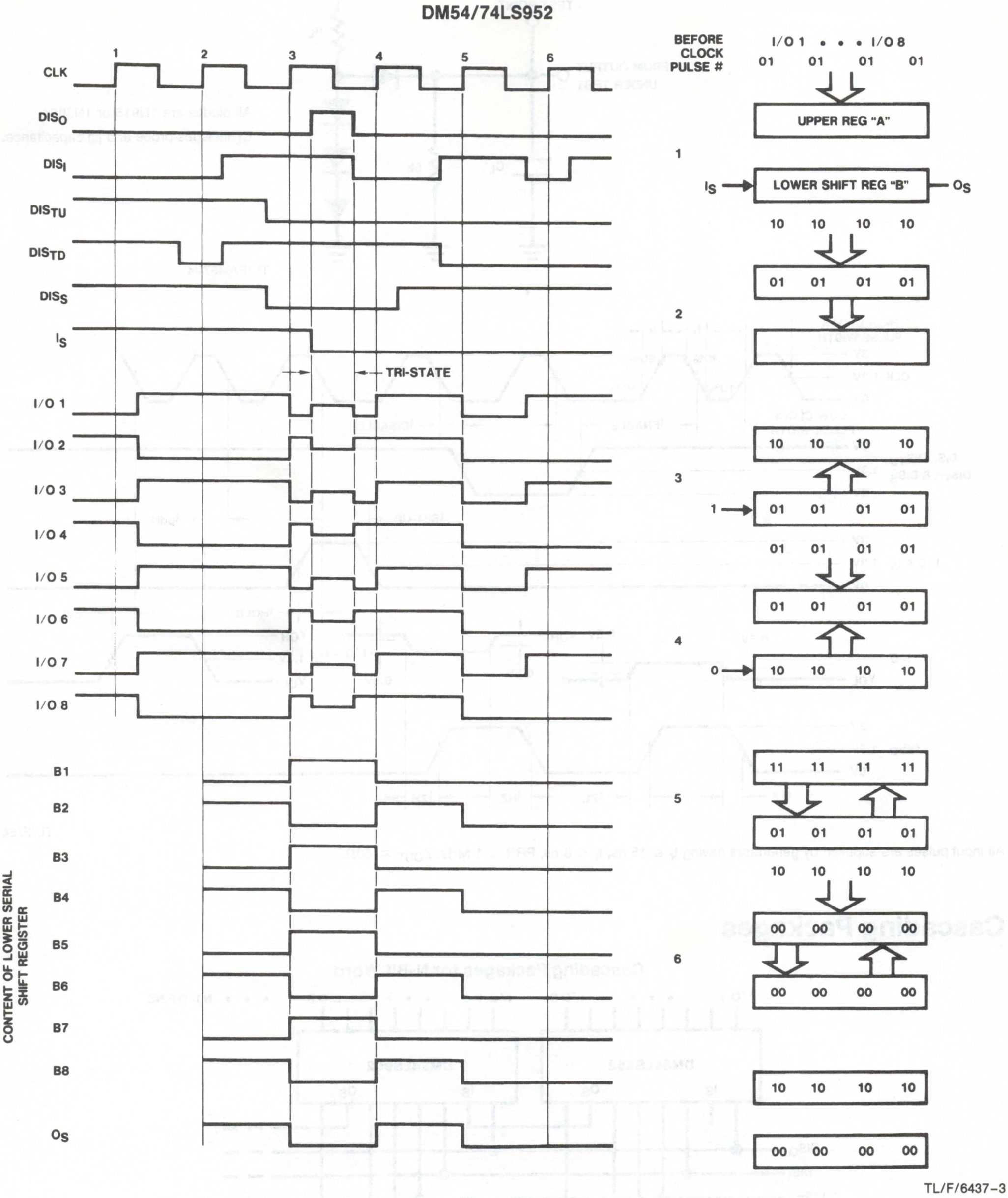
a1 . . . a8/b1 . . . b8 ≡ The content of the upper register "A"/the lower serial shift register "B" before the most recent ↑ transition of the clock

$I_1 \ldots I_8$ ≡ The level of steady state inputs of the I/O pins

DOR ≡ "Data ORing function" ORing data from both I/O pins and register "B", i.e., $I_1 + b1$, $I_2 + b2$, $I_3 + b3 \ldots I_8 + b8$

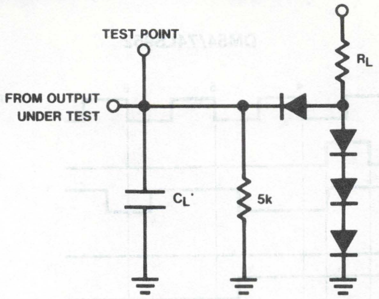
d ≡ Data of the serial input

Timing Diagram


DM54/74LS952
CLK
1
2
3
4
5
6
DIS_O
DIS_I
DIS_TU
DIS_TD
DIS_S
I_S
TRI-STATE
I/O 1
I/O 2
I/O 3
I/O 4
I/O 5
I/O 6
I/O 7
I/O 8
B1
B2
B3
B4
B5
B6
B7
B8
O_S
CONTENT OF LOWER SERIAL SHIFT REGISTER
BEFORE CLOCK PULSE #
I/O 1 • • • I/O 8
01 01 01 01
UPPER REG "A"
LOWER SHIFT REG "B"
I_S
O_S
10 10 10 10
01 01 01 01
11 11 11 11
00 00 00 00

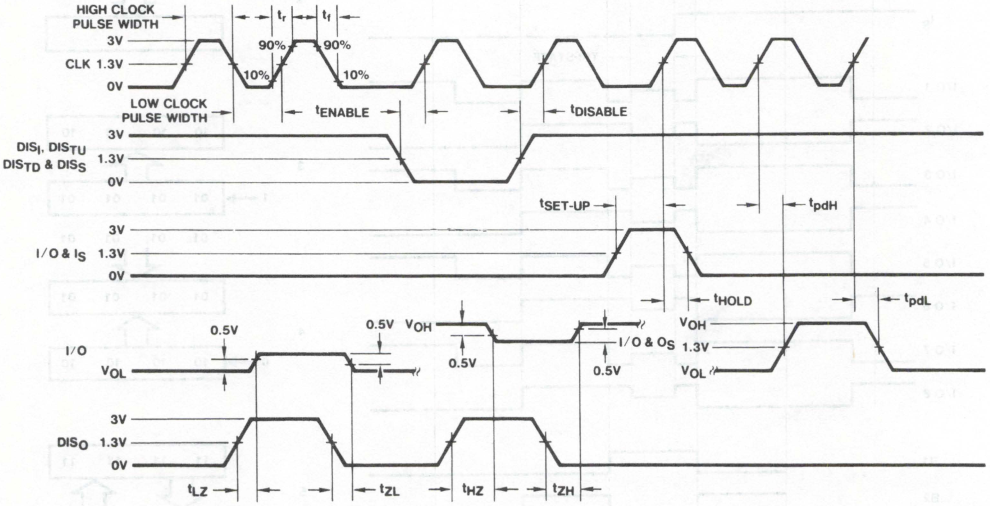
TL/F/6437-3

AC Test Circuit and Switching Time Waveforms


TEST POINT
FROM OUTPUT UNDER TEST
R_L
C_L*
5k

All diodes are 1N916 or 1N3064.
C_L includes probe and jig capacitance.

TL/F/6437-4

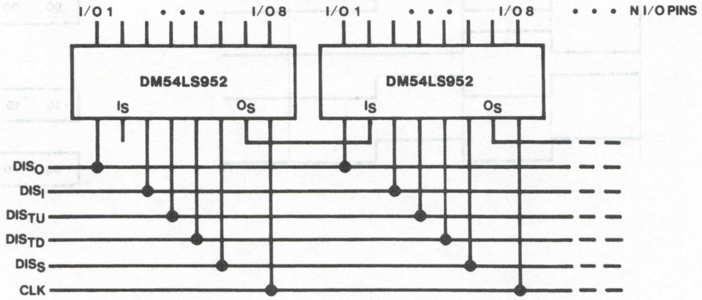

HIGH CLOCK PULSE WIDTH
t_r
t_f
3V
90%
90%
CLK 1.3V
10%
10%
0V
LOW CLOCK PULSE WIDTH
t_{ENABLE}
$t_{DISABLE}$
DIS_I, DIS_{TU} DIS_{TD} & DIS_S
3V
1.3V
0V
t_{SET-UP}
t_{pdH}
3V
I/O & I_S 1.3V
0V
t_{HOLD}
t_{pdL}
0.5V
0.5V V_{OH}
V_{OH}
I/O
V_{OL}
0.5V
I/O & O_S 1.3V
0.5V
V_{OL}
3V
DIS_O 1.3V
0V
t_{LZ}
t_{ZL}
t_{HZ}
t_{ZH}

TL/F/6437-5

All input pulses are supplied by generators having $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, $Z_{OUT} \approx 50\Omega$.

Cascading Packages

Cascading Packages for N-Bit Word


I/O 1
• • •
I/O 8
I/O 1
• • •
I/O 8
• • • N I/O PINS
DM54LS952
I_S
O_S
DM54LS952
I_S
O_S
DIS_O
DIS_I
DIS_{TU}
DIS_{TD}
DIS_S
CLK

TL/F/6437-6

National Semiconductor

DM74LS962
Dual Rank 8-Bit TRI-STATE® Shift Registers

General Description

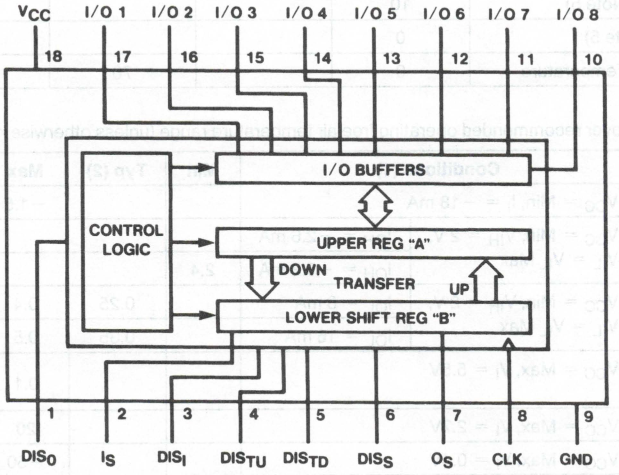
These circuits are TRI-STATE, edge-triggered, 8-bit I/O registers in parallel with 8-bit serial shift registers which are capable of operating in any of the following modes: parallel load from I/O pins to register "A", parallel transfer down from register "A" to serial shift register "B", parallel transfer up from shift register "B" to register "A", serial shift of register "B", or exchange data between register "A" and shift register "B". Since the registers are edge-triggered by the positive transition of the clock, the control lines which determine the mode or operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

Features

- Registers are edge-triggered by the positive transition of the clock
- All inputs are PNP transistors
- Input disable dominates over output disable
- Output high impedance state does not impede any other mode of operation
- 8-bit I/O pins are TRI-STATE buffers
- Typical shift frequency is 36 MHz
- Typical power dissipation is 305 mW
- All control inputs are active when in an "L" logic state
- Devices can be cascaded into N-bit word

Connection Diagram

Dual-In-Line Package



TL/F/6438-1

Top View

Order Number DM74LS962N

See NS Package Number N18A

Pin Description

DIS_O—Output disable

I_S—Serial input

DIS_I—Input disable

DIS_{TU}—Transfer up disable

DIS_{TD}—Transfer down disable

DIS_S—Shift disable

O_S—Serial output

CLK—Clock

GND—Ground

I/O 1 . . . I/O 8—8-bit I/O pins

V_{CC}—Supply Voltage

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS962			Units
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High-Level Input Voltage	2			V
V_{IL}	Low-Level Input Voltage			0.8	V
I_{OH}	High-Level Output Current			−5.2	mA
I_{OL}	Low-Level Output Current			16	mA
f_{CLOCK}	Clock Frequency (Note 5)	0		25	MHz
Clock Pulse	High Pulse Width (Note 5)	25	17		ns
	Low Pulse Width (Note 5)	15	7		ns
t_{SET-UP}	Data Set-Up Time (Note 5)	10			ns
t_{HOLD}	Data Hold Time (Note 5)	0			ns
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (1)		Min	Typ (2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = V_{IL} Max	I_{OH} = −2.6 mA				V
			I_{OH} = −5.2 mA	2.4			
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = V_{IL} Max	I_{OL} = 8 mA		0.25	0.4	V
			I_{OL} = 16 mA		0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4V				−50	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = Max (3)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (4)			61	99	mA
I_{OFF}	TRI-STATE I/O Current	V_{CC} = Max, V_{IH} = 2V	V_O = 2.4V			20	μA
			V_O = 0.4V			−20	μA

Note 1: For conditions shown as min or max, use the appropriate value specified under recommended operating conditions.

Note 2: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

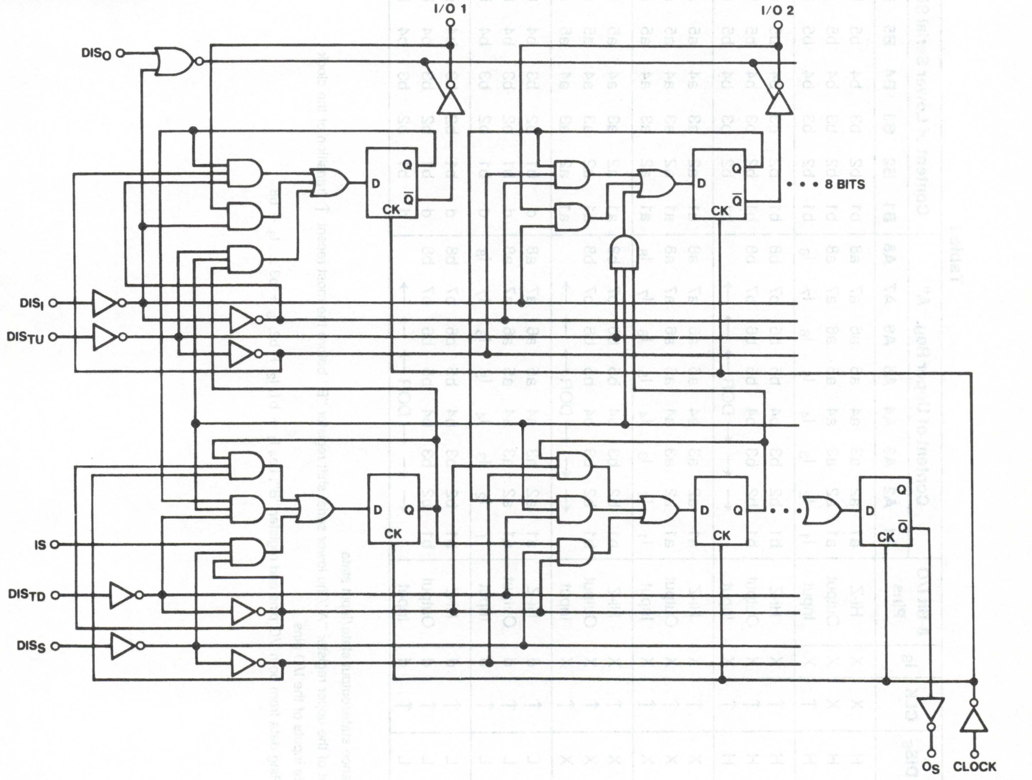
Note 4: I_{CC} is measured with serial output open, the clock and shift disable input at 2.4V. All other control inputs and I/O pins grounded.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	$C_L = 15$ pF, $R_L = 1$ kΩ	25		MHz
t_{PLH}	Propagation Delay Time, Low-to-High-Level from Clock to Any Outputs		7	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level from Clock to Any Outputs		10	48	ns
t_{ENABLE}	Enable Time from Any Control Inputs		5	24	ns
$t_{DISABLE}$	Disable Time from Any Control Inputs		6	27	ns
t_{ZH}	Output Enable Time to High Level		5	23	ns
t_{ZL}	Output Enable to Low Level		4	18	ns
t_{HZ}	Output Disable Time from High Level	$C_L = 5$ pF, $R_L = 1$ kΩ	5	23	ns
t_{LZ}	Output Disable Time from Low Level		6	27	ns

Logic Diagram



TL/F/6438–2

Function Table

Table I

DIS$_O$	DIS$_I$	DIS$_{TU}$	DIS$_{TD}$	DIS$_S$	CLK	I$_S$	8-Bit I/O Pins	Content of Upper Reg. "A"								Content of Lower Serial Shift Reg. "B"								O$_S$	Comments
								A1	A2	A3	A4	A5	A6	A7	A8	B1	B2	B3	B4	B5	B6	B7	B8		
H	H	H	H	H	X	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Stable state
L	H	H	H	H	X	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	H	H	H	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Entering data from I/O to reg. "A"
H	H	L	H	H	↑	X	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Transfer data up from reg. "B" to reg. "A"
L	H	L	H	H	↑	X	Output	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	L	H	H	↑	X	Input	← ← ← DOR → → →								b1	b2	b3	b4	b5	b6	b7	b8	b8	Reg. "A" will OR data from I/O to reg. "B"
H	H	H	L	X	↑	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Transfer data down from reg. "A" to reg. "B"
L	H	H	L	X	↑	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	
X	L	H	L	X	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Entering data and transfer down
H	H	L	L	X	↑	X	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	a1	a2	a3	a4	a5	a6	a7	a8	a8	(1) Exchange data between registers
L	H	L	L	X	↑	X	Output	b1	b2	b3	b4	b5	b6	b7	b8	a1	a2	a3	a4	a5	a6	a7	a8	a8	(2) Beside data exchanging, reg. "A"
X	L	L	L	X	↑	X	Input	← ← ← DOR → → →								a1	a2	a3	a4	a5	a6	a7	a8	a8	(3) will "OR" data from I/O and reg. "B"
H	H	H	H	L	↑	d	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	Serial shifting in the lower reg. "B"
L	H	H	H	L	↑	d	Output	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	H	H	L	↑	d	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	d	b1	b2	b3	b4	b5	b6	b7	b7	Entering data and serial shifting
H	H	L	H	L	↑	d	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	Transfer up and serial shifting
L	H	L	H	L	↑	d	Output	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	L	H	L	↑	d	Input	← ← ← DOR → → →								d	b1	b2	b3	b4	b5	b6	b7	b7	DOR function and serial shifting

X ≡ Don't Care

Hi-Z/Output/Input/ ≡ High impedance state/output state/input state

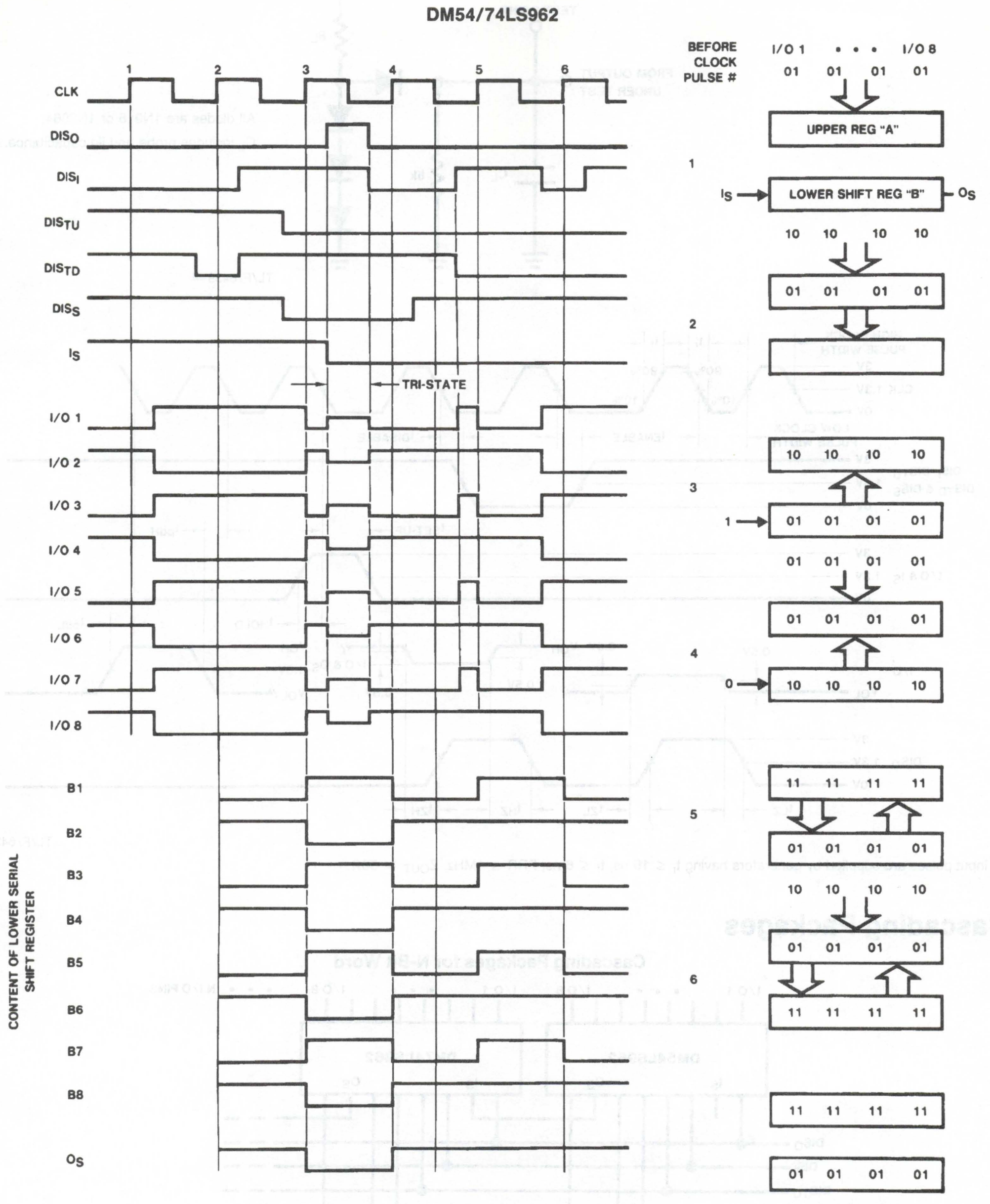
a1 . . . a8/b1 . . . b8 ≡ The content of the upper register "A"/the lower serial shift register "B" before the most recent ↑ transition of the clock

$I_1 \ldots I_8$ ≡ The level of steady state inputs of the I/O pins

DOR ≡ "Data ORing function" ORing data from both I/O pins and register "B", i.e., $I_1 + b1$, $I_2 + b2$, $I_3 + b3 \ldots I_8 + b8$

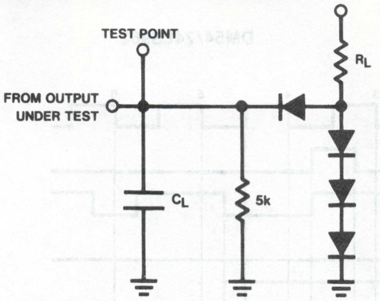
d ≡ Data of the serial input

Timing Diagram


DM54/74LS962
1
2
3
4
5
6
CLK
DIS_O
DIS_I
DIS_TU
DIS_TD
DIS_S
I_S
TRI-STATE
I/O 1
I/O 2
I/O 3
I/O 4
I/O 5
I/O 6
I/O 7
I/O 8
B1
B2
B3
B4
B5
B6
B7
B8
O_S
CONTENT OF LOWER SERIAL SHIFT REGISTER
BEFORE CLOCK PULSE #
I/O 1 • • • I/O 8
01 01 01 01
UPPER REG "A"
LOWER SHIFT REG "B"
I_S
O_S
10 10 10 10
01 01 01 01
10 10 10 10
1
01 01 01 01
01 01 01 01
01 01 01 01
0
10 10 10 10
11 11 11 11
01 01 01 01
10 10 10 10
01 01 01 01
11 11 11 11
11 11 11 11
01 01 01 01

TL/F/6438-3

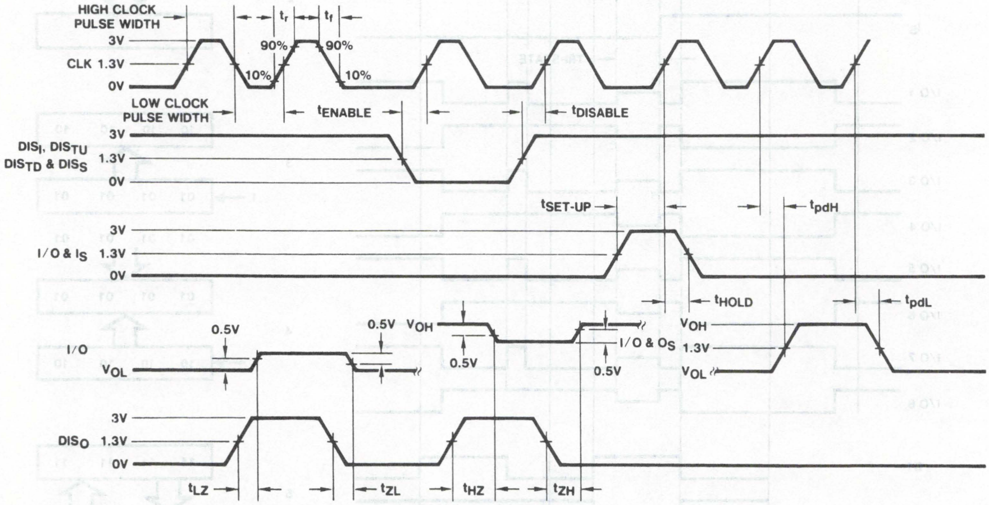
AC Test Circuit and Switching Time Waveforms


TEST POINT
FROM OUTPUT UNDER TEST
R_L
C_L
5k

All diodes are 1N916 or 1N3064.

C_L includes probe and jig capacitance.

TL/F/6438-4

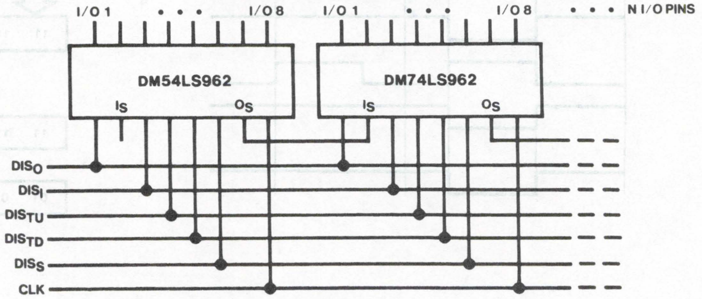

HIGH CLOCK PULSE WIDTH
t_r
t_f
3V
CLK 1.3V
0V
90%
90%
10%
10%
LOW CLOCK PULSE WIDTH
t_{ENABLE}
$t_{DISABLE}$
DIS_I, DIS_{TU} DIS_{TD} & DIS_S
3V
1.3V
0V
t_{SET-UP}
t_{pdH}
3V
I/O & I_S 1.3V
0V
t_{HOLD}
t_{pdL}
0.5V
0.5V
V_{OH}
I/O
V_{OL}
0.5V
0.5V
I/O & O_S
V_{OH}
1.3V
V_{OL}
3V
DIS_O 1.3V
0V
t_{LZ}
t_{ZL}
t_{HZ}
t_{ZH}

TL/F/6438-5

All input pulses are supplied by generators having $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR $\leq$ 1MHz, $Z_{OUT} \approx 50\Omega$.

Cascading Packages

Cascading Packages for N-Bit Word


I/O 1
• • •
I/O 8
I/O 1
• • •
I/O 8
• • • N I/O PINS
DM54LS962
I_S
O_S
DM74LS962
I_S
O_S
DIS_O
DIS_I
DIS_{TU}
DIS_{TD}
DIS_S
CLK

TL/F/6438-6

National Semiconductor

96LS02/DM96LS02
Dual Retriggerable Resettable Monostable Multivibrator

General Description

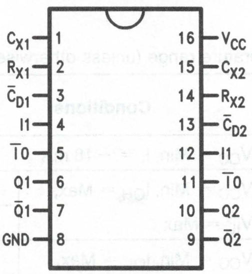
The 96LS02 is a dual retriggerable and resettable monostable multivibrator. The one-shot provides exceptionally wide delay range, pulse width stability, predictable accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. Resistor values up to 1.0 MΩ reduce required capacitor values. Hysteresis is provided on both trigger inputs of the 96LS02 for increased noise immunity.

Features

- Required timing capacitance reduced by factors of 10 to 100 over conventional designs
- Broad timing resistor range—1.0 kΩ to 2.0 MΩ
- Output Pulse Width is variable over a 2000:1 range by resistor control
- Propagation delay of 35 ns
- 0.3V hysteresis on trigger inputs
- Output pulse width independent of duty cycle
- 35 ns to ∞ output pulse width range

Connection Diagram

Dual-In-Line Package



TL/F/9816–1

Order Number 96LS02DMQB, 96LS02FMQB, DM96LS02M or DM96LS02N
See NS Package Number J16A, M16A, N16E or W16A

Pin Names	Description
$\overline{I0}$	Trigger Input (Active Falling Edge)
$\overline{I0}$	Schmitt Trigger Input (Active Falling Edge)
I1	Schmitt Trigger Input (Active Rising Edge)
$\overline{C}_D$	Direct Clear Input (Active LOW)
Q	True Pulse Output
$\overline{Q}$	Complementary Pulse Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
96LS Military	−55°C to +125°C
DM96LS Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	96LS02 (MIL)			DM96LS02 (COM)			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	MIL	2.5			V
			COM	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	MIL			0.4	V
			COM		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	COM		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−100	mA
			COM	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				36	mA
V_{T+}	Positive-Going Threshold Voltage, $\overline{I}0$, I1					2.0	V
V_{T-}	Negative-Going Threshold Voltage, $\overline{I}0$, I1		MIL	0.7			V
			COM	0.8			

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	96LS (MIL)		DM96LS (COM)		Units
		$C_L = 15$ pF		$C_L = 15$ pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay $\overline{I0}$ to Q		45		55	ns
t_{PHL}	Propagation Delay $\overline{I0}$ to $\overline{Q}$		33		50	ns
t_{PLH}	Propagation Delay I1 to Q		45		60	ns
t_{PHL}	Propagation Delay I1 to $\overline{Q}$		33		55	ns
t_{PHL}	Propagation Delay $\overline{C_D}$ to Q		25		30	ns
t_{PLH}	Propagation Delay $\overline{C_D}$ to $\overline{Q}$		30		35	ns
$t_w(L)$	$\overline{I0}$ Pulse Width LOW	15		15		ns
$t_w(H)$	I1 Pulse With HIGH	30		30		ns
$t_w(L)$	$\overline{C_D}$ Pulse Width LOW	22		22		ns
$t_w(H)$	Minimum Q Pulse Width HIGH	20	70	25	55	ns
t_w	Q Pulse Witdh	4.25	5.0	4.1	4.5	μs
R_X	Timing Resistor Range*			1	1000	kΩ
t	Change in Q Pulse Width over Temperature				1.0	%
t	Change in Q Pulse Width over V_{CC} Range				0.8 1.5	%

*Applies only over commercial V_{CC} and T_A range for 96S02.

Functional Description

The 96LS02 dual retriggerable resettable monostable multivibrator has two DC coupled trigger inputs per function, one active LOW ($\overline{I0}$) and one active HIGH (I1). The I1 input and $\overline{I0}$ input of the 96LS02 utilize an internal Schmitt trigger with hysteresis of 0.3V to provide increased noise immunity. The use of active HIGH and LOW inputs allows either rising or falling edge triggering and optional non-retriggerable operation. The inputs are DC coupled making triggering independent of input transition times. When input conditions for triggering are met, the Q output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger which occurs during the timing cycle will retrigger the circuit and result in Q remaining HIGH. The output pulse may be terminated (Q to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the $\overline{Q}$ output to $\overline{I0}$ or the Q output to I1. Differential sensing techniques are used to obtain excellent stability over temperature and power supply variations and a feedback Darlington capacitor discharge circuit minimizes pulse width variation from unit to unit. Schottky TTL output stages provide high switching speeds and output compatibility with all TTL logic families.

Operation Notes

TIMING

1. An external resistor (R_X) and an external capacitor (C_X) are required as shown in the Logic Diagram. The value of R_X may vary from 1.0 kΩ to 1.0 MΩ (96LS02).

2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to V_{CC}/R_X the timing equations may not represent the pulse width obtained.

3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 1 (15), the (−) terminal to pin 2(14) and R_X. Pin 1(15) will remain positive with respect to pin 2(14) during the timing cycle.

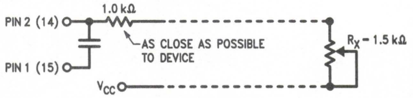
4. The output pulse width t_w for $R_X \geq 10$ kΩ and $C_X \geq$ 1000 pF is determined as follows:

$$t_w = 0.43\, R_X C_X$$

Where R_X is in kΩ, C_X is in pF, t is in ns *or* R_X is in kΩ, C_X is in μF, t is in ms.

5. The output pulse width for $R_X < 10$ kΩ or $C_X < 1000$ pF should be determined from pulse width versus C_X or R_X graphs.

6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



TL/F/9816-4

Operation Notes (Continued)

7. Under any operating condition, C_X and R_X (Min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

8. V_{CC} and ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and ground leads do not cause interaction between one shots. Use of a 0.01 μF to 0.1 μF bypass capacitor between V_{CC} and ground located near the circuit is recommended.

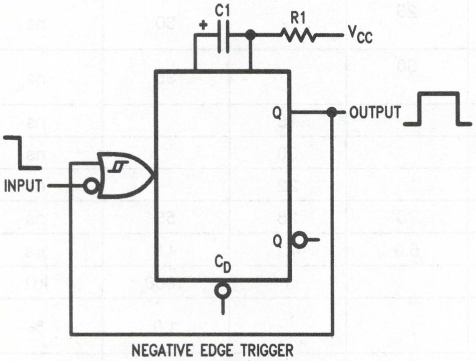
TRIGGERING

1. The minimum negative pulse width into $\overline{I}0$ is 8.0 ns; the minimum positive pulse width into I1 is 12 ns.

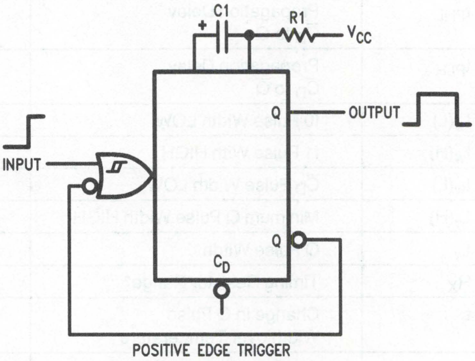
2. Input signals to the 96LS02 exhibiting slow or noisy transitions can use either trigger as both are Schmitt triggers.

3. When non-retriggerable operation is required, i.e., when input triggers are to be ignored during quasi-stable state, input latching is used to inhibit retriggering.

4. An overriding active LOW level direct clear is provided on each multivibrator. By applying a LOW to the clear, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW. A LOW-to-HIGH transition on $\overline{C}_D$ will not trigger the 96LS02. If the $\overline{C}_D$ input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.



TL/F/9816-5



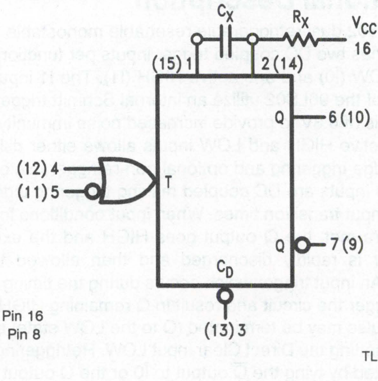
TL/F/9816-6

Triggering Truth Table

Pin No's. 5(11)	4(12)	3(13)	Operation
H → L	L	H	Trigger
H	L → H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level ≥ V_{IH}
L = LOW Voltage Level ≤ V_{IL}
X = Immaterial (either H or L)
H → L = HIGH to LOW Voltage Level Transition
L → H = LOW to HIGH Voltage Level Transition

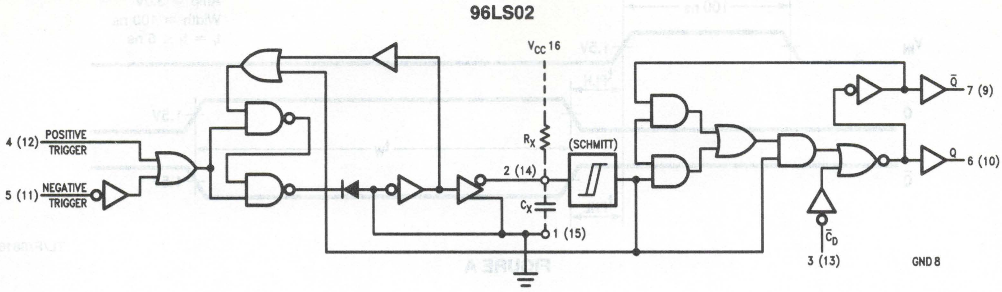
Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

TL/F/9816-2

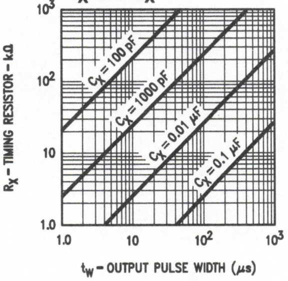
Logic Diagram


96LS02
V_{CC} 16
R_X
(SCHMITT)
2 (14)
C_X
1 (15)
4 (12) POSITIVE TRIGGER
5 (11) NEGATIVE TRIGGER
$\bar{Q}$ 7 (9)
Q 6 (10)
$\bar{C}_D$
3 (13)
GND 8

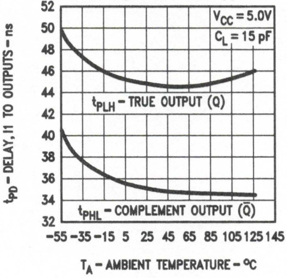
TL/F/9816-3

Typical Performance Characteristics

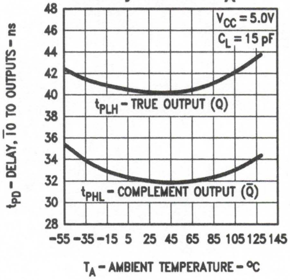
Output t_W vs R_X and C_X



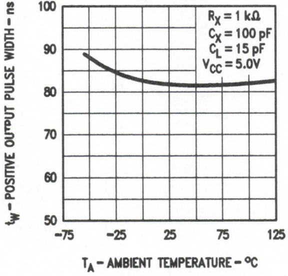
I1 Delay Time vs T_A



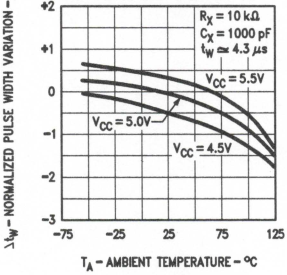
$\bar{I}0$ Delay Time vs T_A



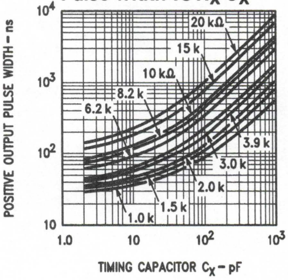
Output t_W vs T_A



Normalized Δt_W vs T_A

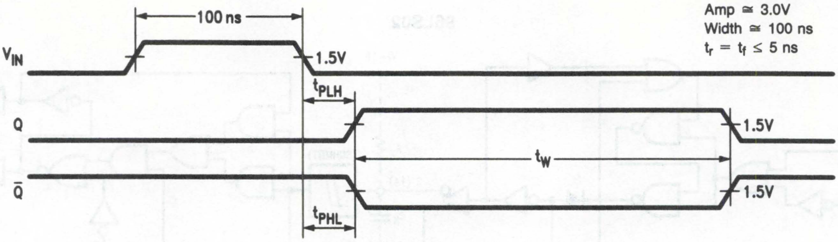


Pulse Width vs R_X C_X



TL/F/9816-7

Input Pulse
f ≅ 100 kHz
Amp ≅ 3.0V
Width ≅ 100 ns
$t_r = t_f \leq 5$ ns


100 ns
V_{IN}
1.5V
t_{PLH}
Q
1.5V
t_W
$\overline{Q}$
1.5V
t_{PHL}

TL/F/9816-8

FIGURE A

Section 3
Schottky

Section 3—Schottky

Schottky—Commercial Products

DM74S00 Quad 2-Input NAND Gate 3-3
DM74S02 Quad 2-Input NOR Gate 3-5
DM74S03 Quad 2-Input NAND Gate with Open-Collector Outputs 3-7
DM74S04 Hex Inverter 3-9
DM74S05 Hex Inverter with Open-Collector Outputs 3-11
DM74S08 Quad 2-Input AND Gate 3-13
DM74S09 Quad 2-Input AND Gate with Open-Collector Outputs 3-15
DM74S10 Triple 3-Input NAND Gate 3-17
DM74S11 Triple 3-Input AND Gate 3-19
DM74S20 Dual 4-Input NAND Gate 3-21
DM74S30 8-Input NAND Gate 3-23
DM74S32 Quad 2-Input OR Gate 3-25
DM74S40 Dual 4-Input NAND Buffer 3-27
DM74S51 Dual 2-Wide 2-Input AND-OR-INVERT Gate 3-29
DM74S64 4-Wide AND-OR-INVERT Gate 3-31
DM74S74 Dual Positive-Edge-Triggered D Flip-Flop with Preset, Clear, and Complementary Outputs 3-33
DM74S86 Quad 2-Input EXCLUSIVE-OR Gate 3-36
DM74S109 Dual Positive-Edge-Triggered J-$\overline{\text{K}}$ Flip-Flop with Preset, Clear, and Complementary Outputs 3-38
DM74S112 Dual Negative-Edge-Triggered J-K Flip-Flop with Preset, Clear, and Complementary Outputs 3-41
DM74S113 Dual Negative-Edge-Triggered J-K Flip-Flop with Preset and Complementary Outputs 3-44
DM74S132 Quad 2-Input Schmitt Trigger NAND Gate 3-47
DM74S133 13-Input NAND Gate 3-50
DM74S138 3-to-8 Line Decoder/Demultiplexer 3-52
DM74S139 Dual 2-to-4 Line Decoder/Demultiplexer 3-52
DM74S140 Dual 4-Input NAND 50Ω Line Driver 3-56
DM74S151 1-of-8 Line Data Selector/Multiplexer with Complementary Outputs 3-59
DM74S153 Dual 1-of-4 Line Data Selector/Multiplexer 3-63
DM74S157 Quad 2-to-1 Line Data Selector/Multiplexer 3-66
DM74S158 Quad 2-to-1 Line Inverting Data Selector/Multiplexer 3-66
DM74S161 Synchronous 4-Bit Binary Counter with Asynchronous Clear 3-71
DM74S163 Synchronous 4-Bit Binary Counter with Synchronous Clear 3-71
DM74S174 Hex D Flip-Flop with Clear 3-77
DM74S175 Quad D Flip-Flop with Clear and Complementary Outputs 3-77
DM74S181 Arithmetic Logic Unit/Function Generator 3-81
DM74S182 Look-Ahead Carry Generator 3-90
DM74S194 4-Bit Bidirectional Universal Shift Register 3-94
DM74S195 4-Bit Parallel Access Shift Register 3-98
DM74S240 Octal TRI-STATE Inverting Buffer/Line Driver/Line Receiver 3-102
DM74S241 Octal TRI-STATE Buffer/Line Driver/Line Receiver 3-102
DM74S244 Octal TRI-STATE Buffer/Line Driver/Line Receiver 3-102
DM74S251 TRI-STATE 1-of-8 Line Data Selector/Multiplexer with Complementary Outputs 3-105
DM74S253 Dual TRI-STATE 1-of-4 Line Data Selector/Multiplexer 3-109

Schottky—Commercial Products (Continued)

DM74S257 Quad TRI-STATE 2-to-1 Line Data Selector/Multiplexer 3-112
DM74S258 Quad TRI-STATE 2-to-1 Line Inverting Data Selector/Multiplexer 3-112
DM74S280 9-Bit Parity Generator/Checker 3-117
DM74S283 4-Bit Binary Adder with Fast Carry 3-121
DM74S299 TRI-STATE 8-Bit Universal Shift/Storage Register 3-125
DM74S373 Octal TRI-STATE Transparent D Latch 3-130
DM74S374 Octal TRI-STATE Positive-Edge-Triggered D Flip-Flop 3-130
DM74S381 Arithmetic Logic Unit/Function Generator 3-135
DM93S00 4-Bit Universal Shift Register 3-139
DM93S41 4-Bit Arithmetic Logic Unit 3-142
DM93S43 4-Bit by 2-Bit Twos Complement Multiplier 3-149
DM93S46 High Speed 6-Bit Identity Comparator 3-153
DM93S47 High Speed 6-Bit Identity Comparator 3-157
DM93S62 9-Input Parity Checker/Generator 3-160
DM96S02 Dual Retriggerable Resettable Monostable Multivibrator (One-Shot) 3-165

Schottky—Mil/Aero Products

DM54S00 Quad 2-Input NAND Gate 3-3
DM54S02 Quad 2-Input NOR Gate 3-5
DM54S04 Hex Inverter 3-9
DM54S08 Quad 2-Input AND Gate 3-13
DM54S10 Triple 3-Input NAND Gate 3-17
DM54S11 Triple 3-Input AND Gate 3-19
DM54S20 Dual 4-Input NAND Gate 3-21
DM54S30 8-Input NAND Gate 3-23
DM54S32 Quad 2-Input OR Gate 3-25
DM54S40 Dual 4-Input NAND Buffer 3-27
DM54S64 4-Wide AND-OR-INVERT Gate 3-31
DM54S74 Dual Positive-Edge-Triggered D Flip-Flop with Preset, Clear, and Complementary Outputs 3-33
DM54S86 Quad 2-Input EXCLUSIVE-OR Gate 3-36
DM54S112 Dual Negative-Edge-Triggered J-K Flip-Flop with Preset, Clear, and Complementary Outputs 3-41
DM54S113 Dual Negative-Edge-Triggered J-K Flip-Flop with Preset and Complementary Outputs 3-44
DM54S133 13-Input NAND Gate 3-50
DM54S138 3-to-8 Line Decoder/Demultiplexer 3-52
DM54S139 Dual 2-to-4 Line Decoder/Demultiplexer 3-52
DM54S140 Dual 4-Input NAND 50Ω Line Driver 3-56
DM54S151 1-of-8 Line Data Selector/Multiplexer with Complementary Outputs 3-59
DM54S153 Dual 1-of-4 Line Data Selector/Multiplexer 3-63
DM54S157 Quad 2-to-1 Line Data Selector/Multiplexer 3-66
DM54S158 Quad 2-to-1 Line Inverting Data Selector/Multiplexer 3-66
DM54S161 Synchronous 4-Bit Binary Counter with Asynchronous Clear 3-71
DM54S163 Synchronous 4-Bit Binary Counter with Synchronous Clear 3-71
DM54S174 Hex D Flip-Flop with Clear 3-77
DM54S175 Quad D Flip-Flop with Clear and Complementary Outputs 3-77
DM54S181 Arithmetic Logic Unit/Function Generator 3-81
DM54S182 Look-Ahead Carry Generator 3-90
DM54S194 4-Bit Bidirectional Universal Shift Register 3-94
DM54S195 4-Bit Parallel Access Shift Register 3-98
DM54S240 Octal TRI-STATE Inverting Buffer/Line Driver/Line Receiver 3-102
DM54S241 Octal TRI-STATE Buffer/Line Driver/Line Receiver 3-102

Section 3—Schottky (Continued)

Schottky—Mil/Aero Products (Continued)

DM54S244 Octal TRI-STATE Buffer/Line Driver/Line Receiver 3-102
DM54S251 TRI-STATE 1-of-8 Line Data Selector/Multiplexer with Complementary Outputs .. 3-105
DM54S253 Dual TRI-STATE 1-of-4 Line Data Selector/Multiplexer 3-109
DM54S257 Quad TRI-STATE 2-to-1 Line Data Selector/Multiplexer 3-112
DM54S258 Quad TRI-STATE 2-to-1 Line Inverting Data Selector/Multiplexer 3-112
DM54S280 9-Bit Parity Generator/Checker 3-117
DM54S283 4-Bit Binary Adder with Fast Carry 3-121
DM54S373 Octal TRI-STATE Transparent D Latch 3-130
DM54S374 Octal TRI-STATE Positive-Edge-Triggered D Flip-Flop 3-130

National Semiconductor

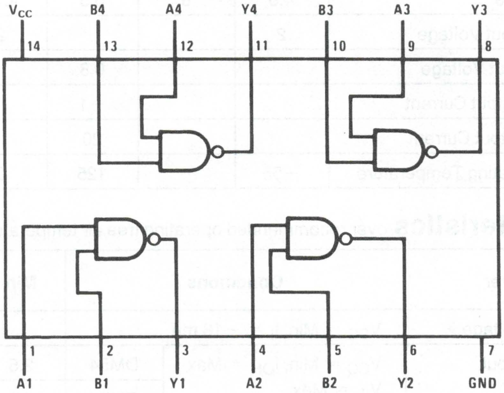
DM54S00/DM74S00 Quad 2-Input NAND Gates

General Description

This device contains four independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



V_{CC}
B4
A4
Y4
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
Y1
A2
B2
Y2
GND

TL/F/6489–1

Order Number DM54S00J, DM54S00W, DM74S00M or DM74S00N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S00			DM74S00			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			10	16	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			20	36	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	4.5	2	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	5	2	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time and the duration should not exceed one second.

National Semiconductor

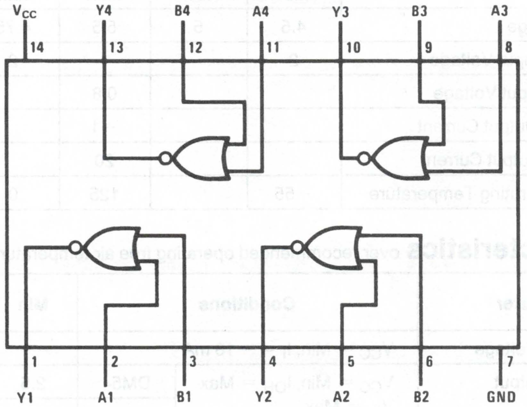
DM54S02/DM74S02 Quad 2-Input NOR Gates

General Description

This device contains four independent gates each of which performs the logic NOR function.

Connection Diagram

Dual-In-Line Package



V_{CC}
Y4
B4
A4
Y3
B3
A3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
Y1
A1
B1
Y2
A2
B2
GND

TL/F/6490-1

Order Number DM54S02J, DM54S02W or DM74S02N
See NS Package Number J14A, N14A or W14B

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S02			DM74S02			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			17	29	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			26	45	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 280\Omega$				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	1.5	5.5	2	7.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	1.5	5.5	2	7.5	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM74S03 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

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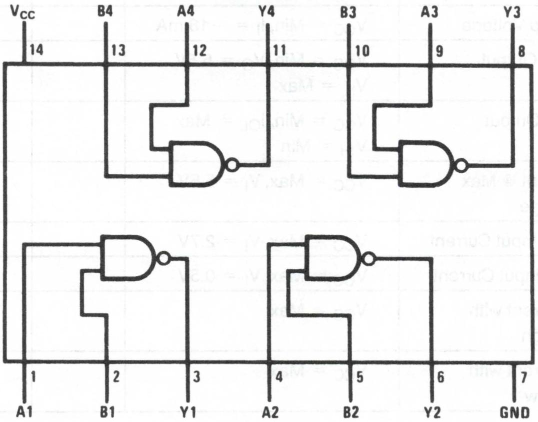
Connection Diagram

Dual-In-Line Package



TL/F/6491-1

Order Number DM74S03N
See NS Package Number N14A

Function Table

$Y = \overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74S03			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Voltage			5.5	V
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		6.0	13.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		20	36	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	7.5	3	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	7	3	11	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

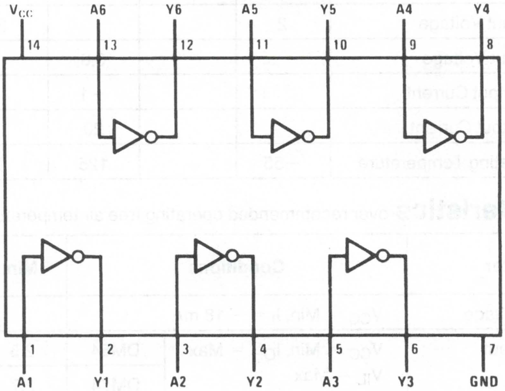
DM54S04/DM74S04 Hex Inverting Gates

General Description

This device contains six independent gates each of which performs the logic INVERT function.

Connection Diagram

Dual-In-Line Package



VCC
A6
Y6
A5
Y5
A4
Y4
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
Y1
A2
Y2
A3
Y3
GND

TL/F/6442-1

Order Number DM54S04J, DM54S04W, DM74S04M or DM74S04N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S04			DM74S04			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			15	24	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			30	54	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 280\Omega$				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	4.5	2	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	5	2	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM74S05 Hex Inverters with Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

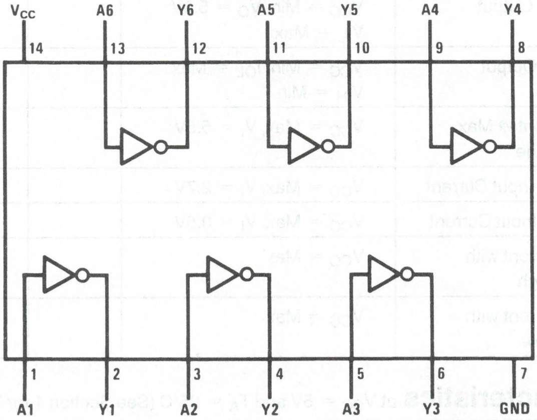
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6443–1

Order Number DM74S05M or DM74S05N
See NS Package Number M14A or N14A

Function Table

$Y = \overline{A}$

Input	Output
A	**Y**
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Voltage			5.5	V
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18\text{ mA}$			−1.2	V
I_{CEX}	High Level Output Current	$V_{CC} = \text{Min}, V_O = 5.5\text{V}$ $V_{IL} = \text{Max}$			250	μA
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}$			0.5	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5\text{V}$			1	mA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.7\text{V}$			50	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.5\text{V}$			−2	mA
I_{CCH}	Supply Current with Outputs High	$V_{CC} = \text{Max}$		9	19.8	mA
I_{CCL}	Supply Current with Outputs Low	$V_{CC} = \text{Max}$		30	54	mA

Switching Characteristics at $V_{CC} = 5\text{V}$ and $T_A = 25°\text{C}$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 280\Omega$				Units
		$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	7.5	3	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	7	3	11	ns

Note 1: All typicals are at $V_{CC} = 5\text{V}$, $T_A = 25°\text{C}$.

National Semiconductor

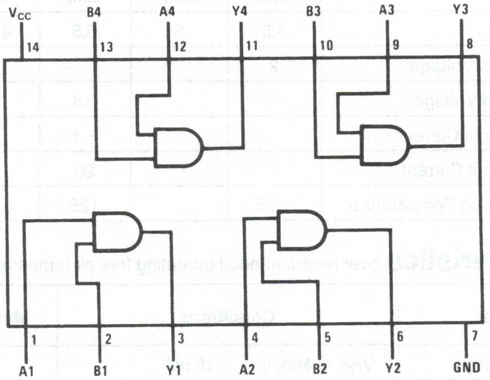
DM54S08/DM74S08 Quad 2-Input AND Gates

General Description

This device contains four independent gates each of which performs the logic AND function.

Connection Diagram

Dual-In-Line Package



V_{CC}
B4
A4
Y4
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
Y1
A2
B2
Y2
GND

TL/F/6444-1

Order Number DM54S08J, DM54S08W or DM74S08N
See NS Package Number J14A, N14A or W14B

Function Table

Y = AB

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S08			DM74S08			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			18	32	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			32	57	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 280\Omega$				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2.5	7	3	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2.5	7.5	3	11	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM74S09 Quad 2-Input AND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require an external pull-up resistor for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

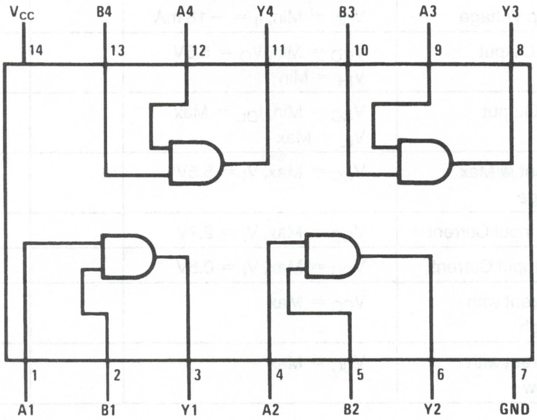
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6465-1

Order Number DM74S09N
See NS Package Number N14A

Function Table

Y = AB

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74S09			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Voltage			5.5	V
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IH} = Min			250	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max			0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		18	32	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		32	57	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

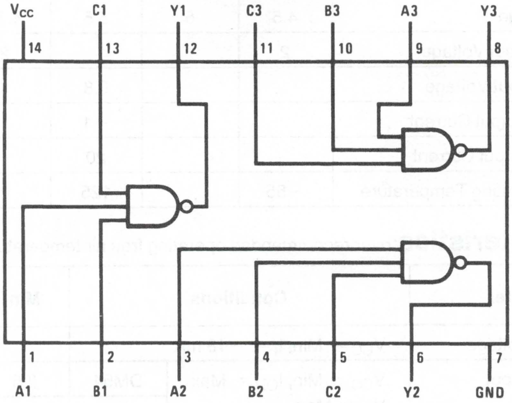
DM54S10/DM74S10 Triple 3-Input NAND Gates

General Description

This device contains three independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



V_{CC}
C1
Y1
C3
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
A2
B2
C2
Y2
GND

TL/F/6446–1

Order Number DM54S10J, DM54S10W or DM74S10N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{ABC}$

Inputs			Output
A	**B**	**C**	**Y**
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S10			DM74S10			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			7.5	12	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			15	27	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	4.5	2	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	5	2	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

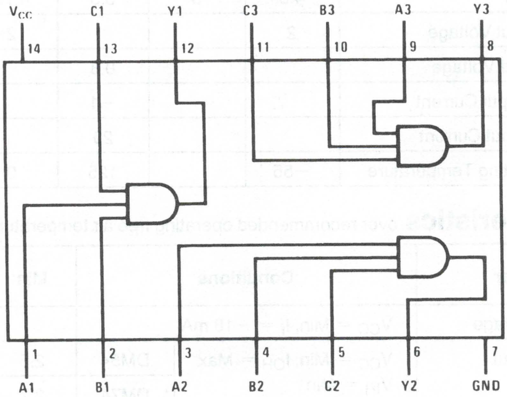
DM54S11/DM74S11 Triple 3-Input AND Gates

General Description

This device contains three independent gates each of which performs the logic AND function.

Connection Diagram

Dual-In-Line Package



V_{CC}
C1
Y1
C3
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
A2
B2
C2
Y2
GND

TL/F/6447-1

Order Number DM54S11J, DM54S11W or DM74S11N
See NS Package Number J14A, N14A or W14B

Function Table

$$Y = ABC$$

Inputs			Output
A	**B**	**C**	**Y**
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S11			DM74S11			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			13.5	24	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			24	42	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 280\Omega$				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2.5	7	3	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2.5	7.5	3	11	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

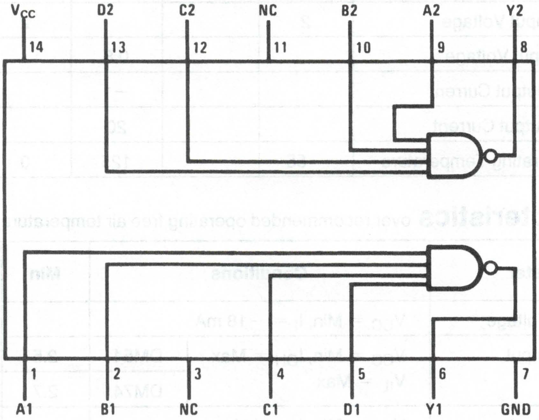
DM54S20/DM74S20 Dual 4-Input NAND Gates

General Description

This device contains two independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



V_{CC}
D2
C2
NC
B2
A2
Y2
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
NC
C1
D1
Y1
GND

TL/F/6449–1

Order Number DM54S20J, DM54S20W or DM74S20N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	**B**	**C**	**D**	**Y**
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S20			DM74S20			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			5	8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			10	18	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (see Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 280\Omega$				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	4.5	2	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	5	2	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

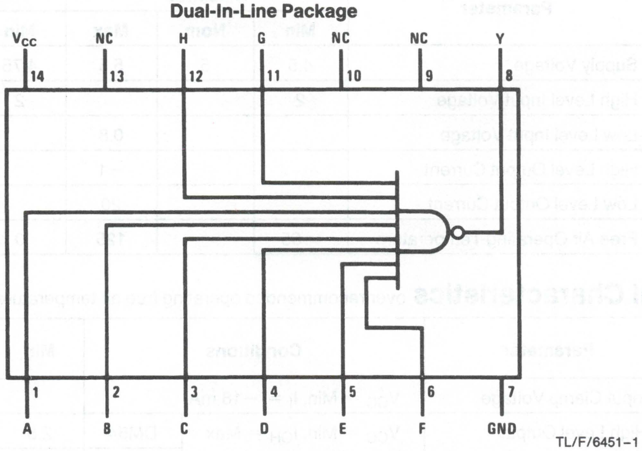
National Semiconductor

DM54S30/DM74S30 8-Input NAND Gate

General Description

This device contains a single gate which performs the logic NAND function.

Connection Diagram


Dual-In-Line Package
V_{CC}
NC
H
G
NC
NC
Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A
B
C
D
E
F
GND
TL/F/6451–1

Order Number DM54S30J, DM54S30W or DM74S30N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{ABCDEFGH}$

Inputs	Output
A thru H	Y
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S30			DM74S30			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			3	5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			5.5	10	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 280\Omega$				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	6	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	7	3	10	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

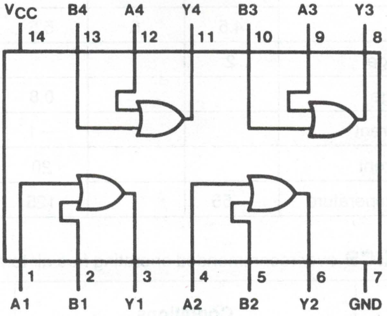
DM54S32/DM74S32 Quad 2-Input OR Gates

General Description

This device contains four independent gates each of which performs the logic OR function.

Connection Diagram

Dual-In-Line Package


V_{CC}
B4
A4
Y4
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
Y1
A2
B2
Y2
GND

TL/F/6452–1

Order Number DM54S32J, DM54S32W or DM74S32N
See NS Package Number J14A, N14A or W14B

Function Table

Y = A + B

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S32			DM74S32			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			18	32	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			38	68	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 280\Omega$				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	7	2	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	7	2	9	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

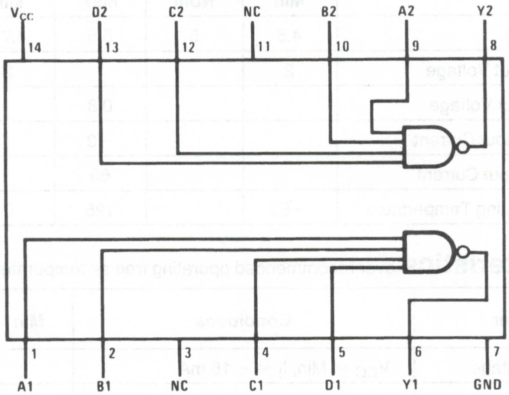
DM54S40/DM74S40 Dual 4-Input NAND Buffers

General Description

This device contains two independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package


V_{CC}
D2
C2
NC
B2
A2
Y2
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
NC
C1
D1
Y1
GND

TL/F/6453–1

Order Number DM54S40J, DM54S40W or DM74S40N
See NS Package Number J14A, N14A or W16B

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S40			DM74S40			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−3			−3	mA
I_{OL}	Low Level Output Current			60			60	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				100	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−50		−225	mA
			DM74	−50		−225	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			10	18	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			25	44	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 93Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	6.5	3	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	6.5	3	9	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

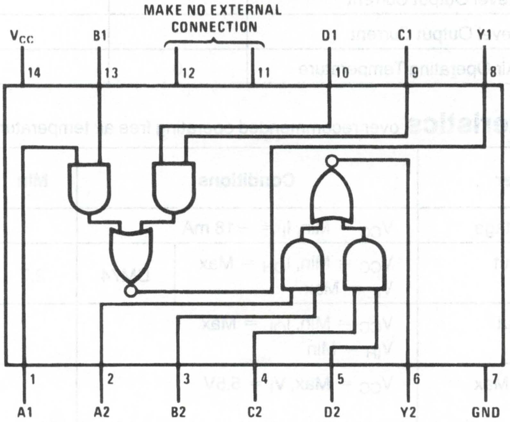
DM74S51 Dual 2-Wide 2-Input AND-OR-INVERT Gates

General Description

This device contains two independent combinations of gates each of which performs the logic AND-OR-INVERT function.

Connection Diagram

Dual-In-Line Package


MAKE NO EXTERNAL CONNECTION
V_{CC}
B1
D1
C1
Y1
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
A2
B2
C2
D2
Y2
GND

TL/F/6454–1

Order Number DM74S51N
See NS Package Number N14A

Function Table

$$Y = \overline{AB + CD}$$

Inputs				Output
A	**B**	**C**	**D**	**Y**
H	H	X	X	L
X	X	H	H	L
All other combinations				H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74S51 Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−1	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	DM74	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−40		−100	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			8.2	17.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			14	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 280\Omega$				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	5.5	3	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	5.5	3	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

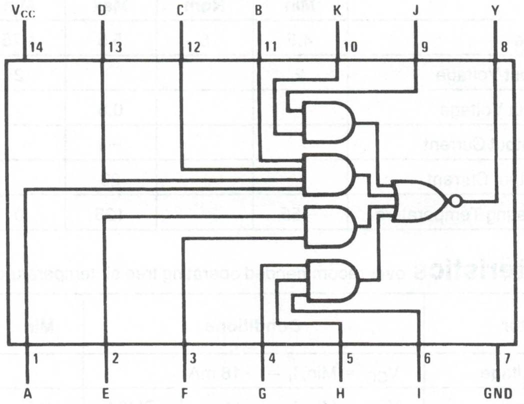
DM54S64/DM74S64 4-Wide AND-OR-INVERT Gates

General Description

This device contains a combination of gates which performs the logic AND-OR-INVERT function.

Connection Diagram

Dual-In-Line Package



TL/F/6455–1

Order Number DM54S64J, DM54S64W or DM74S64N
See NS Package Number J14A, N14A or W14B

Function Table

$$Y = \overline{ABCD + EF + GHI + JK}$$

Inputs											Output
A	B	C	D	E	F	G	H	I	J	K	Y
H	H	H	H	X	X	X	X	X	X	X	L
X	X	X	X	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S64			DM74S64			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			7	12.5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			8.5	16	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	5.5	3	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	5.5	3	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

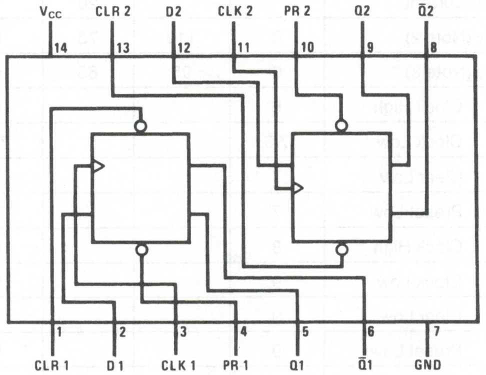
DM54S74/DM74S74
Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6457-1

Order Number DM54S74J, DM54S74W, DM74S74M or DM74S74N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
PR	**CLR**	**CLK**	**D**	**Q**	**$\overline{Q}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Logic Level
X = Either Low or High Logic Level
L = Low Logic Level
↑ = Positive-going Transition
* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to its inactive (high) level.
Q_0 = The output logic level of Q before the indicated input conditions were established.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM54S74			DM74S74			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	110	75	0	110	75	MHz
f_{CLK}	Clock Frequency (Note 3)		0	95	65	0	95	65	MHz
t_W	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	7.3			7.3			
		Clear Low	7			7			
		Preset Low	7			7			
t_W	Pulse Width (Note 3)	Clock High	8			8			ns
		Clock Low	9			9			
		Clear Low	9			9			
		Preset Low	9			9			
t_{SU}	Setup Time (Notes 1 & 2)		3↑			3↑			ns
t_{SU}	Setup Time (Notes 1 & 3)		3↑			3↑			ns
t_H	Input Hold Time (Notes 1 & 2)		2↑			2↑			ns
t_H	Input Hold Time (Notes 1 & 3)		2↑			2↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge at the clock pulse is used for reference.

Note 2: $C_L = 15$ pF, $R_L = 280\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: $C_L = 50$ pF, $R_L = 280\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	D			50	μA
			Clear			150	
			Preset			100	
			Clock			100	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	D			−2	mA
			Clear			−6	
			Preset			−4	
			Clock			−4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max, (Note 3)			30	50	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock is grounded.

Note 4: Clear is tested with preset high and preset is tested with clear high.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		75		65		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		6		9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		6		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Clock High)	Preset to $\overline{Q}$		13.5		17	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Clock Low)	Preset to $\overline{Q}$		8		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Clock High)	Clear to Q		13.5		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Clock Low)	Clear to Q		8		13	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		9		12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		9		14	ns

National Semiconductor

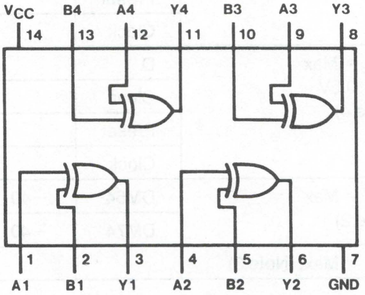
DM54S86/DM74S86 Quad 2-Input Exclusive-OR Gates

General Description

This device contains four independent gates each of which performs the logic Exclusive-OR function.

Connection Diagram

Dual-In-Line Package


V_{CC}
B4
A4
Y4
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
Y1
A2
B2
Y2
GND

TL/F/6458-1

Order Number DM54S86J, DM54S86W or DM74S86N
See NS Package Number J14A, N14A or W14B

Function Table

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S86			DM74S86			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			35	50	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)			50	75	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) to (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to Y		10.5		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			10		13	ns

National Semiconductor

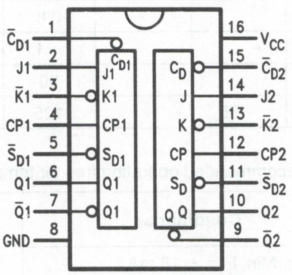
DM74S109 Dual $J\overline{K}$ Positive Edge-Triggered Flip-Flop

General Description

This device consists of two high speed, completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop (refer to 'S74 data sheet) by connecting the J and $\overline{K}$ inputs together.

Connection Diagram

Dual-In-Line Package


1
$\overline{C}_{D1}$
2
J1
3
$\overline{K}1$
4
CP1
5
$\overline{S}_{D1}$
6
Q1
7
$\overline{Q}1$
8
GND
C_{D1}
J1
K1
CP1
S_{D1}
Q1
Q1
16
V_{CC}
15
$\overline{C}_{D2}$
14
J2
13
$\overline{K}2$
12
CP2
11
$\overline{S}_{D2}$
10
Q2
9
$\overline{Q}2$
C_D
J
K
CP
S_D
Q
Q

TL/F/9802–1

Order Number DM74S109N
See NS Package Number N16E

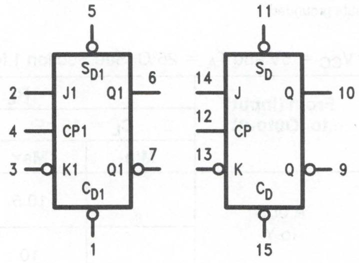
Truth Table

Inputs		Outputs	
@ t_n		@ $t_n + 1$	
J	K	Q	Q
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse
H = HIGH Voltage Level
L = LOW Voltage Level

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Logic Symbol


5
S_{D1}
2
J1
Q1
6
4
CP1
3
K1
Q1
7
C_{D1}
1
11
S_D
14
J
Q
10
12
CP
13
K
Q
9
C_D
15

TL/F/9802–2

V_{CC} = Pin 16
GND = Pin 8

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range DM74S	 0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation*

Recommended Operating Conditions

Symbol	Parameter	DM74S109			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−1	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time J_n or $\overline{K}_n$ to CP_n	6.0 6.0			ns
t_h (H) t_h (L)	Hold Time J_n or $\overline{K}_n$ to CP_n	0 0			ns
t_w (H) t_w (L)	CP_n Pulse Width	7.0 6.5			ns
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	6.0			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2.0	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max V_{CP} = 0V			52	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

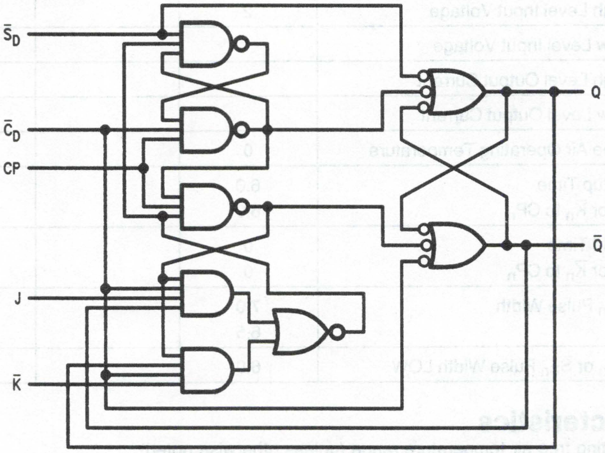
$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15$ pF $R_L = 280\Omega$		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	75		MHz
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$		9.0 11	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		6.0 11	ns

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Logic Diagram (one half shown)



TL/F/9802-3

National Semiconductor

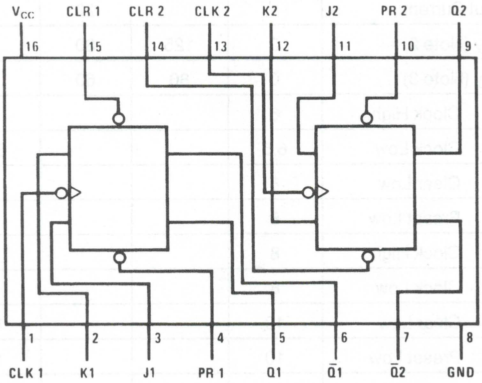
DM54S112/DM74S112 Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs can be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6459–1

Order Number DM54S112J or DM74S112N
See NS Package Number J16A or N16E

Function Table

Inputs					Outputs	
PR	**CLR**	**CLK**	**J**	**K**	**Q**	**$\overline{Q}$**
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↓ = Negative going edge of pulse.

Q_0 = The output logic level of Q before the indicated input conditions were established.

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to its inactive (high) level.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM54S112			DM74S112			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	125	80	0	125	80	MHz
f_{CLK}	Clock Frequency (Note 3)		0	80	60	0	80	60	MHz
t_W	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	6.5			6.5			
		Clear Low	8			8			
		Preset Low	8			8			
t_W	Pulse Width (Note 3)	Clock High	8			8			ns
		Clock Low	8			8			
		Clear Low	10			10			
		Preset Low	10			10			
t_{SU}	Setup Time (Notes 1 & 4)		7↓			7↓			ns
t_H	Input Hold Time (Notes 1 & 4)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge at the clock pulse is used for reference.

Note 2: $C_L = 15$ pF, $R_L = 280\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: $C_L = 50$ pF, $R_L = 280\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 4: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	J, K			50	μA
			Clear			100	
			Preset			100	
			Clock			100	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	J, K			−1.6	mA
			Clear			−7	
			Preset			−7	
			Clock			−4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	50	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Note 4: Clear is tested with preset high and preset is tested with clear high.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		80		60		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		7		12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		7		12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		7		12	ns

National Semiconductor

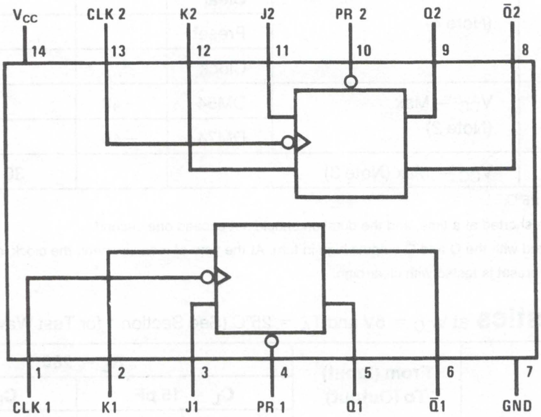
DM54S113/DM74S113 Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs may be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset input will set the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6460-1

Order Number DM54S113J or DM74S113N
See NS Package Number J14A or N14A

Function Table

Inputs				Outputs	
PR	**CLK**	**J**	**K**	**Q**	**$\overline{Q}$**
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level
X = Either Low or High Logic Level
L = Low Logic Level
↓ = Negative going edge of pulse.
Q_0 = The output logic level of Q before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM54S113			DM74S113			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	125	80	0	125	80	MHz
f_{CLK}	Clock Frequency (Note 3)		0	80	60	0	80	60	MHz
t_W	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	6.5			6.5			
		Preset Low	8			8			
t_W	Pulse Width (Note 3)	Clock High	8			8			ns
		Clock Low	8			8			
		Preset Low	10			10			
t_{SU}	Setup Time (Notes 1 & 4)		7↓			7↓			ns
t_H	Input Hold Time (Notes 1 & 4)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge at the clock pulse is used for reference.

Note 2: $C_L = 15$ pF, $R_L = 280\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: $C_L = 50$ pF, $R_L = 280\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 4: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	J, K			50	μA
			Preset			100	
			Clock			100	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V	J, K			−1.6	mA
			Preset			−7	
			Clock			−4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max, (Note 3)			30	50	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		80		60		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		7		12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		7		12	ns

National Semiconductor

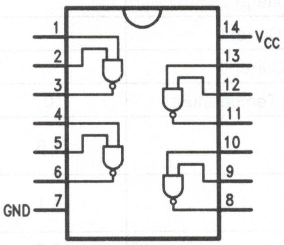
DM74S132
Quad 2-Input Schmitt Trigger NAND Gate

General Description

This device contains four independent gates that perform the logic NAND function. Each gate has two inputs that are Schmitt Triggers.

Connection Diagram

Dual-In-Line Package



TL/F/9803-1

Order Number DM74S132N
See NS Package Number N14A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for acutal device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74S132			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−1	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C
V_{T+}	Positive-Going Threshold Voltage	1.6		1.9	V
V_{T-}	Negative-Going Threshold Voltage	1.1		1.4	V
$V_{T+}-V_{T-}$	Hysteresis Voltage	0.2			V
I_{T+}	Input Current at Positive-Going Threshold	−0.9**			mA
I_{T-}	Input Current at Negative-Going Threshold	−1.1**			mA

*DC limits apply over operating temperature range; AC limits apply at $T_A = +25°C$ and $V_{CC} = +5.0V$. **Typical Value.

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2.0	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−40		−100	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			44	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			68	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 280\Omega$		Units
		$C_L = 15$ pF		
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		10.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		13	ns

National Semiconductor

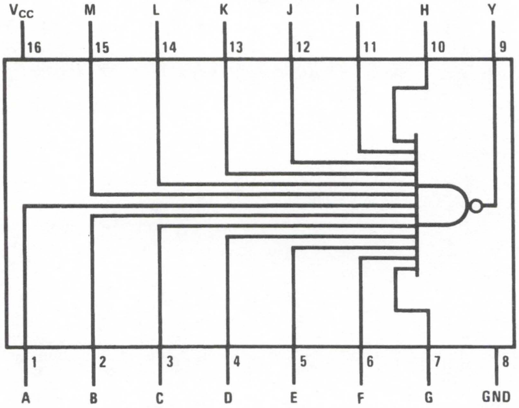
DM54S133/DM74S133 13-Input NAND Gate

General Description

This device contains a single gate which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



V_{CC}
M
L
K
J
I
H
Y
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
A
B
C
D
E
F
G
GND

TL/F/6462-1

Order Number DM54S133J, DM74S133M or DM74S133N
See NS Package Number J16A, M16A or N16E

Function Table

$Y = \overline{ABCDEFGHIJKLM}$

Inputs	Output
A thru M	**Y**
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S133			DM74S133			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			3	5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			5.5	10	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	6	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	7	3	10	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S138/DM74S138, DM54S139/DM74S139 Decoders/Demultiplexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The S138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The S139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

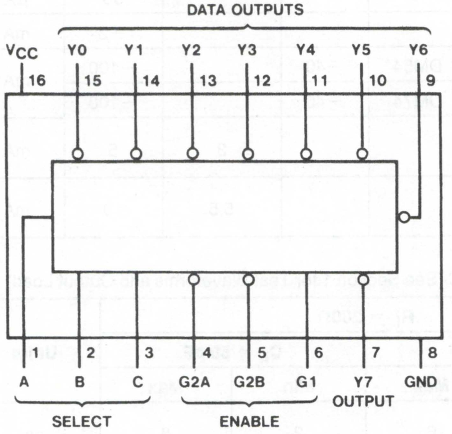
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  Memory decoders
  Data transmission systems
- S138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- S139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay time (3 levels of logic)
  S138 8 ns
  S139 7.5 ns
- Typical power dissipation
  S138 245 mW
  S139 300 mW

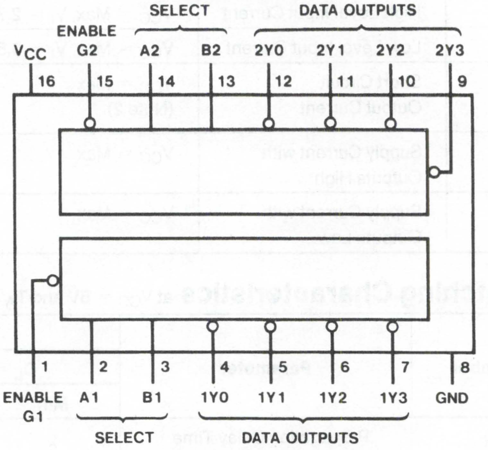
Connection Diagrams

Dual-In-Line Package


DATA OUTPUTS
VCC
Y0
Y1
Y2
Y3
Y4
Y5
Y6
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
A
B
C
G2A
G2B
G1
Y7
GND
OUTPUT
SELECT
ENABLE

TL/F/6466–1

Dual-In-Line Package


SELECT
DATA OUTPUTS
ENABLE
VCC
G2
A2
B2
2Y0
2Y1
2Y2
2Y3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
ENABLE
G1
A1
B1
1Y0
1Y1
1Y2
1Y3
GND
SELECT
DATA OUTPUTS

TL/F/6466–2

Order Number DM54S138J, DM54S139J, DM54S138W, DM54139W, DM74S138N or DM74S139N
See NS Package Number J16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55° C to +125°C
DM74S	0° C to +70°C
Storage Temperature Range	−65° C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S138,S139			DM74S138,S139			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current (S138)	V_{CC} = Max (Note 3)			49	74	mA
I_{CC}	Supply Current (S139)	V_{CC} = Max (Note 3)			60	90	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs enabled and open.

'S138 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) to (Output)	Levels of Delay	R_L = 280Ω				Units
				C_L = 15 pF		C_L = 50 pF		
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	2		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	2		10.5		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	3		12		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	3		12		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	2		8		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	2		11		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	3		11		13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	3		11		14	ns

'S139 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) to (Output)	Levels of Delay	R_L = 280Ω				Units
				C_L = 15 pF		C_L = 50 pF		
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	2		7.5		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	2		10		13	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	3		12		13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	3		12		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	2		8		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	2		10		13	ns

Function Tables

S138

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* G2 = G2A + G2B

H = high level, L = low level, X = don't care (either low or high logic level)

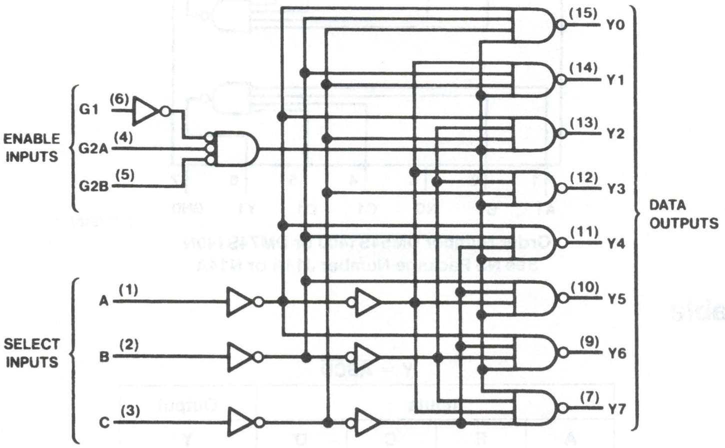
S139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care (either low or high logic level)

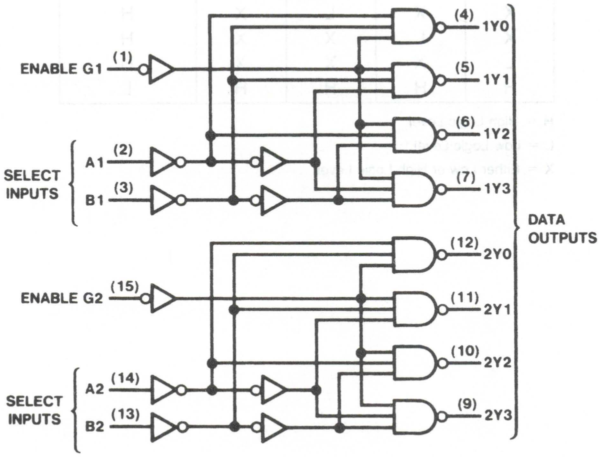
Logic Diagrams

S138


ENABLE INPUTS
G1 (6)
G2A (4)
G2B (5)
SELECT INPUTS
A (1)
B (2)
C (3)
(15) Y0
(14) Y1
(13) Y2
(12) Y3
(11) Y4
(10) Y5
(9) Y6
(7) Y7
DATA OUTPUTS

TL/F/6466-3

S139


ENABLE G1 (1)
SELECT INPUTS
A1 (2)
B1 (3)
ENABLE G2 (15)
SELECT INPUTS
A2 (14)
B2 (13)
(4) 1Y0
(5) 1Y1
(6) 1Y2
(7) 1Y3
(12) 2Y0
(11) 2Y1
(10) 2Y2
(9) 2Y3
DATA OUTPUTS

TL/F/6466-4

National Semiconductor

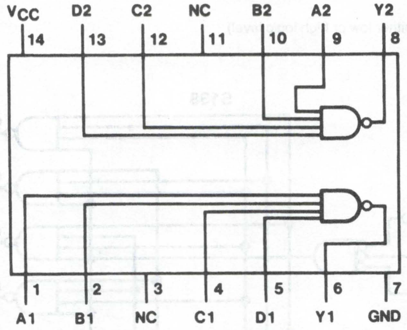
DM54S140/DM74S140
Dual 4-Input NAND 50Ω Line Driver

General Description

This device contains two independent line driver gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



V_{CC}
D2
C2
NC
B2
A2
Y2
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
NC
C1
D1
Y1
GND

TL/F/6467-1

Order Number DM54S140J or DM74S140N
See NS Package Number J14A or N14A

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	**B**	**C**	**D**	**Y**
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S140			DM74S140			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−3			−3	mA
I_{OL}	Low Level Output Current			60			60	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = Max I_{OH} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
		V_{IL} = 0.5V, R_O = 50Ω to GND		2.0			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				100	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−50		−225	mA
			DM74	−50		−225	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			10	18	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			25	44	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 93\Omega$				Units
		$C_L = 50$ pF		$C_L = 150$ pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	6.5	3	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	6.5	3	9	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor

DM54S151/DM74S151 1-of-8 Data Selector/Multiplexer with Complementary Outputs

General Description

These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The 'S151 selects one-of-eight data sources. The 'S151 has a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high and the Y output low.

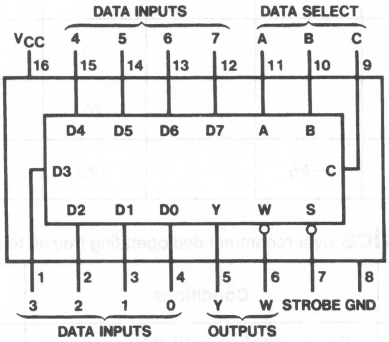
The 'S151 features complementary W and Y outputs.

Features

- Select one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time, data input to W output 4.5 ns
- Typical power dissipation 225 mW

Connection Diagram

Dual-In-Line Package



TL/F/6468-1

Order Number DM54S151J, DM54S151W or DM74S151N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = don't care

D0, D1 . . . D7 = the level of the respective D input

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S151			DM74S151			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			45	70	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

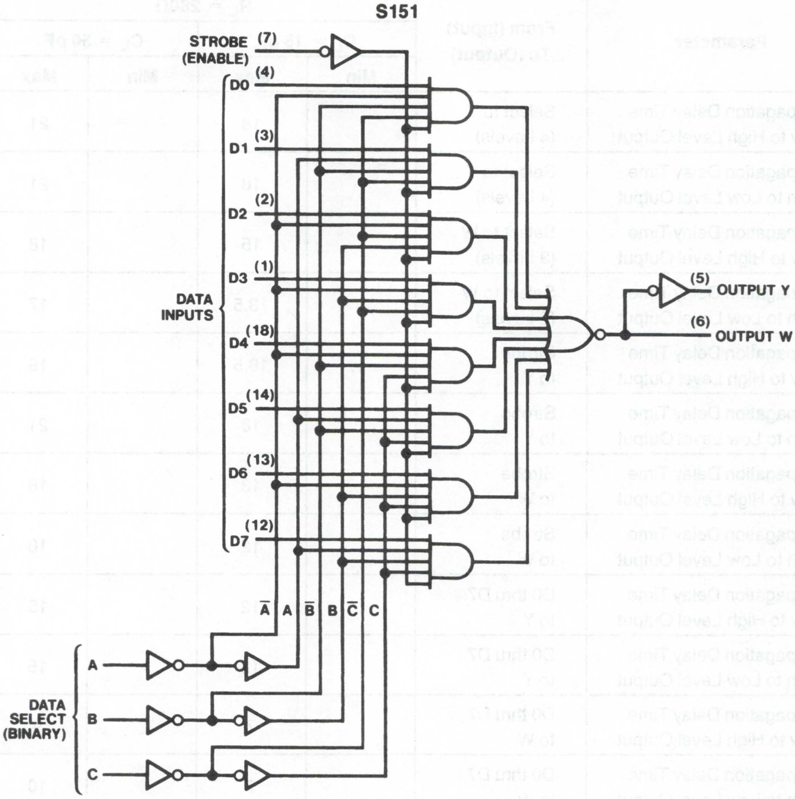
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the strobe and data select inputs at 4.5V, all other inputs and outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			$C_L = 15$ pF		$C_L = 50$ pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y (4 Levels)		18		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y (4 Levels)		18		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to W (3 Levels)		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to W (3 Levels)		13.5		17	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		16.5		19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		18		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to W		13		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to W		12		16	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D0 thru D7 to Y		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D0 thru D7 to Y		12		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D0 thru D7 to W		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D0 thru D7 to W		7		10	ns

Logic Diagram


S151
STROBE (ENABLE) (7)
(4) D0
(3) D1
(2) D2
(1) D3
(18) D4
(14) D5
(13) D6
(12) D7
DATA INPUTS
A̅ A B̅ B C̅ C
DATA SELECT (BINARY)
A
B
C
(5) OUTPUT Y
(6) OUTPUT W

TL/F/6468-2

National Semiconductor

DM54S153/DM74S153 Dual 1 of 4 Line Data Selectors/Multiplexers

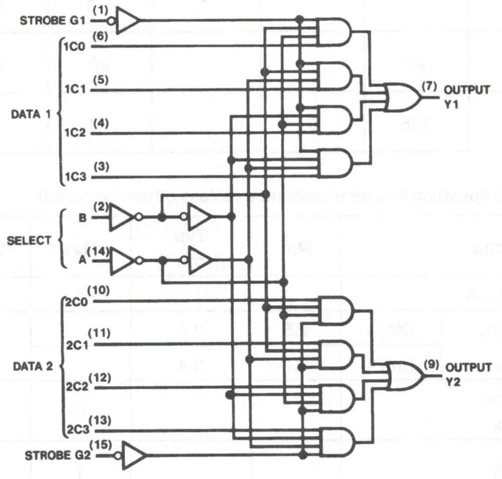
General Description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

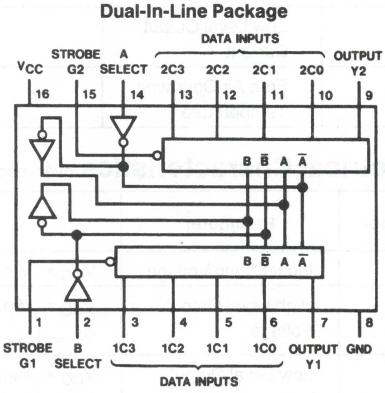
- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low-impedance, totem-pole outputs
- Typical average propagation delay times
  From data 6 ns
  From strobe 9.5 ns
  From select 12 ns
- Typical power dissipation 225 mW

Logic and Connection Diagrams



STROBE G1 (1)
DATA 1
1C0 (6)
1C1 (5)
1C2 (4)
1C3 (3)
(7) OUTPUT Y1
SELECT
B (2)
A (14)
DATA 2
2C0 (10)
2C1 (11)
2C2 (12)
2C3 (13)
(9) OUTPUT Y2
STROBE G2 (15)

TL/F/6469-1



Dual-In-Line Package
DATA INPUTS
VCC
STROBE G2
A SELECT
2C3
2C2
2C1
2C0
OUTPUT Y2
16
15
14
13
12
11
10
9
B B̄ A Ā
B B̄ A Ā
1
2
3
4
5
6
7
8
STROBE G1
B SELECT
1C3
1C2
1C1
1C0
OUTPUT Y1
GND
DATA INPUTS

TL/F/6469-2

Order Number DM54S153J or DM74S153N
See NS Package Number J16A or N16E

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperture Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S153			DM74S153			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			45	70	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		9		12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		9		12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		18		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		18		21	ns
t_{PLH}	Propagtion Delay Time Low to High Level Output	Strobe to Y		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		13.5		17	ns

National Semiconductor

DM54S157/DM74S157, DM54S158/DM74S158 Quad 1 of 2 Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The S157 presents true data whereas the S158 presents inverted data to minimize propagation delay time.

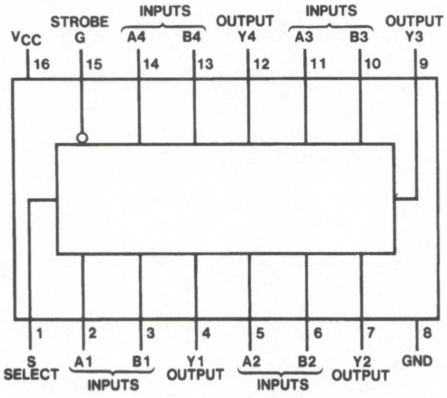
Applications

- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Features

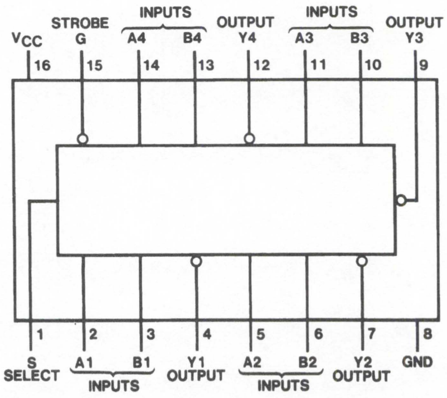
- Buffered inputs and outputs
- Typical propagation time
  S157 5 ns
  S158 4 ns
- Typical power dissipation
  S157 250 mW
  S158 195 mW

Connection Diagrams (Dual-In-Line Packages)


STROBE
INPUTS
OUTPUT
INPUTS
OUTPUT
V_{CC}
G
A4
B4
Y4
A3
B3
Y3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
S
SELECT
A1
B1
INPUTS
Y1
OUTPUT
A2
B2
INPUTS
Y2
OUTPUT
GND

TL/F/6470-1

Order Number DM54S157J, DM54S157W or DM74S157N
See NS Package Number J16A, N16E or W16A


STROBE
INPUTS
OUTPUT
INPUTS
OUTPUT
V_{CC}
G
A4
B4
Y4
A3
B3
Y3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
S
SELECT
A1
B1
INPUTS
Y1
OUTPUT
A2
B2
INPUTS
Y2
OUTPUT
GND

TL/F/6470-2

Order Number DM54S158J, DM54S158W or DM74S158N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs				Output Y	
Strobe	**Select**	**A**	**B**	**S157**	**S158**
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S157			DM74S157			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'S157 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min I_{OH} = Max V_{IL} = Max V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	S or G			100	µA
			A or B			50	
I_{IL}	High Level Input Current	V_{CC} = Max V_I = 0.5V	S or G			−4	mA
			A or B			−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			50	78	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured 4.5V applied to all inputs and all outputs open.

'S157 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		7.5		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		6.5		10	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		12.5		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		12		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		15		17	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		15		17	ns

Recommended Operating Conditions

Symbol	Parameter	DM54S158			DM74S158			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

’S158 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min I_{OH} = Max V_{IL} = Max V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	S or G			100	μA
			A or B			50	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V	S or G			−4	mA
			A or B			−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			39	61	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)				81	mA

’S158 Switching Characteristics at V_{CC} = 5V and T_A = 25 °C

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		6		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		6		9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		11.5		12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		12		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		12		15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

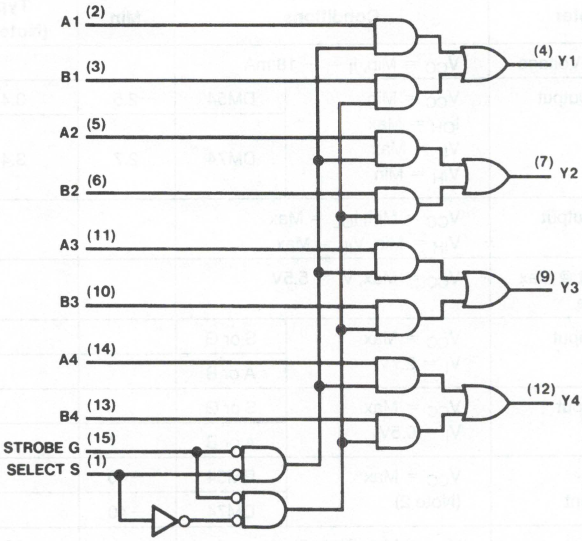
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open and all inputs at 4.5V.

Note 4: I_{CC2} is measured with B, G, and S inputs grounded, A inputs at 4.5V, and all outputs open.

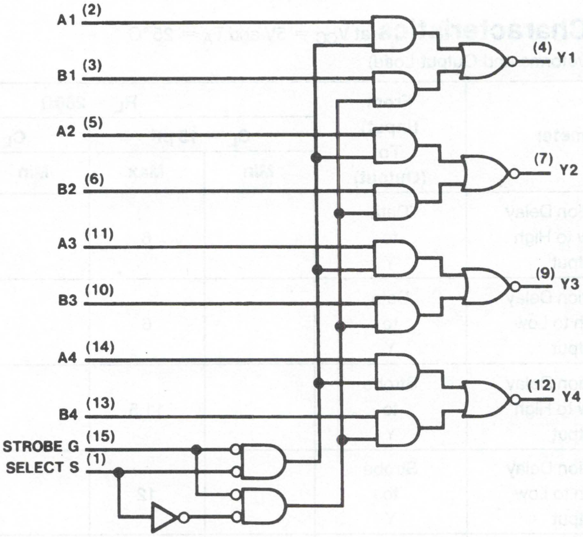
Logic Diagrams

S157


A1 (2)
B1 (3)
A2 (5)
B2 (6)
A3 (11)
B3 (10)
A4 (14)
B4 (13)
STROBE G (15)
SELECT S (1)
(4) Y1
(7) Y2
(9) Y3
(12) Y4

TL/F/6470-3

S158


A1 (2)
B1 (3)
A2 (5)
B2 (6)
A3 (11)
B3 (10)
A4 (14)
B4 (13)
STROBE G (15)
SELECT S (1)
(4) Y1
(7) Y2
(9) Y3
(12) Y4

TL/F/6470-4

National Semiconductor

DM54S161/DM74S161, DM54S163/DM74S163 Synchronous 4-Bit Binary Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. They are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input.

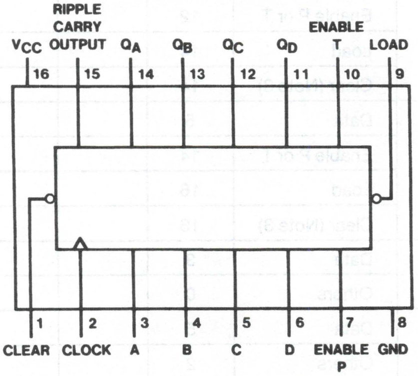
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs

Connection Diagram

Dual-In-Line Package



TL/F/6471–1

Order Number DM54S161J, DM54S163J, DM54S161W, DM74S161N, or DM74S163N
See NS Package Number J16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

See Section 1 for Test Waveforms and Output Load

Symbol	Parameter		DM54S161/163			DM74S161/163			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 1)		0		40	0		40	MHz
	Clock Frequency (Note 2)		0		35	0		35	
t_W	Pulse Width (Note 1)	Clock	10			10			ns
		Clear (Note 4)	10			10			
	Pulse Width (Note 2)	Clock	12			12			
		Clear (Note 4)	12			12			
t_{SU}	Setup Time (Note 1)	Data	4			4			ns
		Enable P or T	12			12			
		Load	14			14			
		Clear (Note 3)	14			14			
	Setup Time (Note 2)	Data	5			5			
		Enable P or T	14			14			
		Load	16			16			
		Clear (Note 3)	16			16			
t_H	Hold Time (Note 1)	Data	3			3			ns
		Others	0			0			
	Hold Time (Note 2)	Data	5			5			
		Others	2			2			
t_{REL}	Load or Clear Release Time (Note 1)		12			12			ns
	Load or Clear Release Time (Note 2)		14			14			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF, $R_L = 280\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 2: $C_L = 50$ pF, $R_L = 280\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: Applies only to the 'S163 which has synchronous clear inputs.

Note 4: Applies only to the 'S161 which has asynchronous clear inputs.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min I_{OH} = Max V_{IL} = Max V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	Low Level Input Current	V_{CC} = Max V_I = 2.7V	CLK, Data			50	μA
			Others	−10		−200	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V	Enable T			−4	mA
			Others			−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			95	160	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

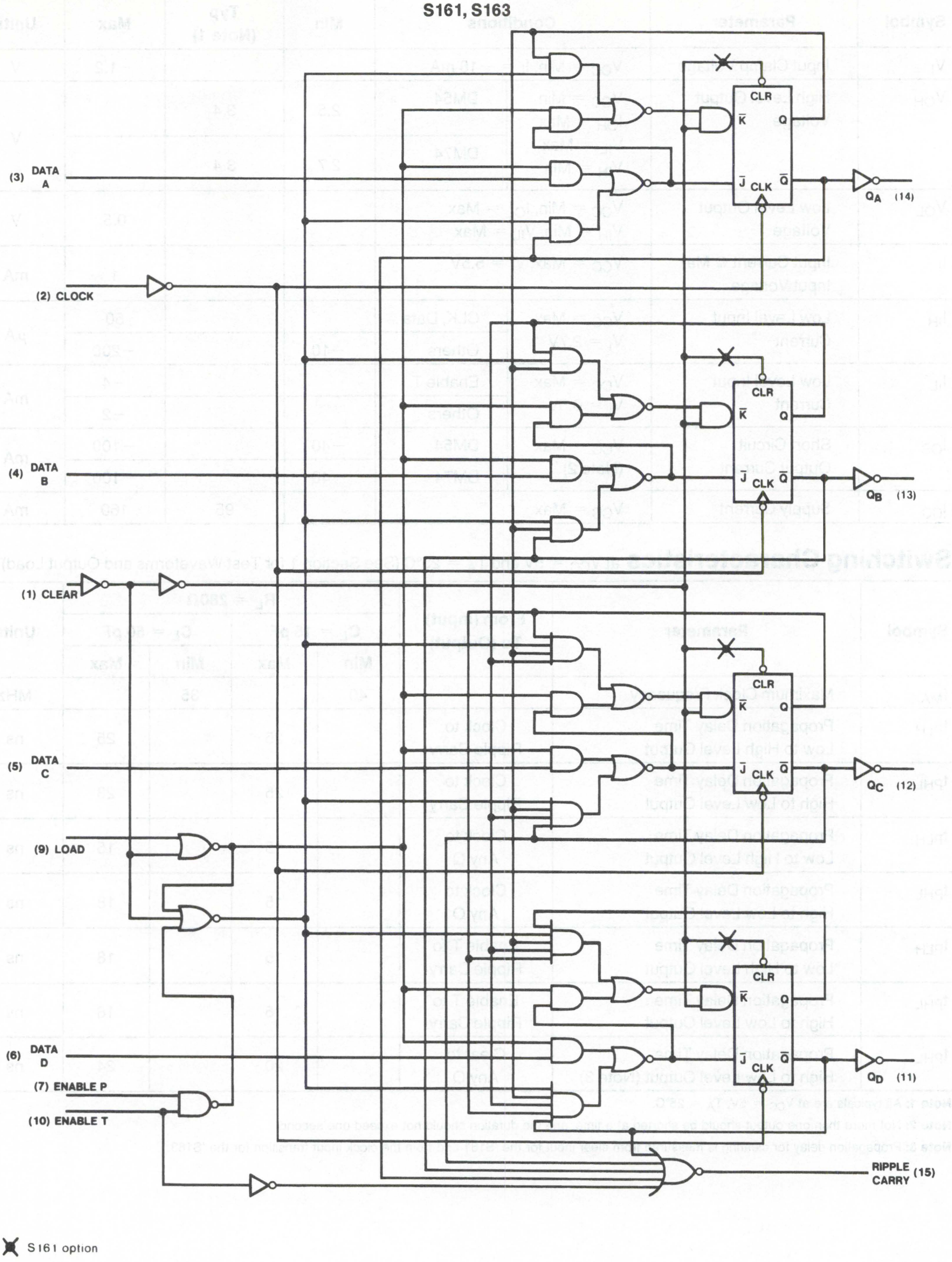
Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		40		35		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		25		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		25		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		15		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		15		18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 3)	Clear to Any Q		20		24	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Propagation delay for clearing is measured from clear input for the 'S161 and from the clock input transition for the 'S163.

Logic Diagram

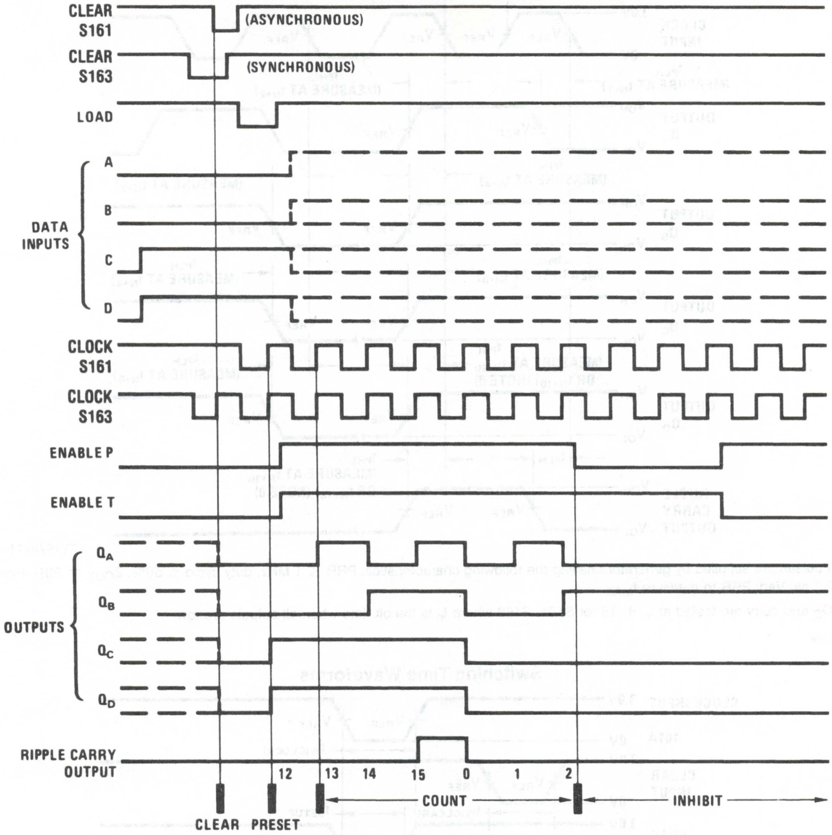


S161, S163
(3) DATA A
(2) CLOCK
(4) DATA B
(1) CLEAR
(5) DATA C
(9) LOAD
(6) DATA D
(7) ENABLE P
(10) ENABLE T
CLR
K̄
Q
J̄
CLK
Q̄
Q_A (14)
Q_B (13)
Q_C (12)
Q_D (11)
RIPPLE CARRY (15)
S161 option

TL/F/6471–2

Timing Diagram

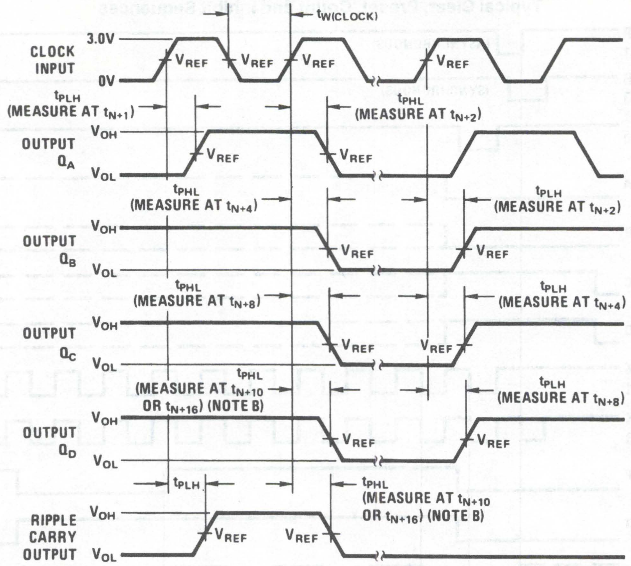
S161, S163 Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences


CLEAR S161
(ASYNCHRONOUS)
CLEAR S163
(SYNCHRONOUS)
LOAD
DATA INPUTS
A
B
C
D
CLOCK S161
CLOCK S163
ENABLE P
ENABLE T
OUTPUTS
Q_A
Q_B
Q_C
Q_D
RIPPLE CARRY OUTPUT
12
13
14
15
0
1
2
COUNT
INHIBIT
CLEAR
PRESET

TL/F/6471-3

Parameter Measurement Information

Switching Time Waveforms


tW(CLOCK)
3.0V
CLOCK INPUT
0V
VREF
tPLH (MEASURE AT tN+1)
tPHL (MEASURE AT tN+2)
OUTPUT QA
VOH
VOL
tPHL (MEASURE AT tN+4)
tPLH (MEASURE AT tN+2)
OUTPUT QB
tPHL (MEASURE AT tN+8)
tPLH (MEASURE AT tN+4)
OUTPUT QC
tPHL (MEASURE AT tN+10 OR tN+16) (NOTE B)
tPLH (MEASURE AT tN+8)
OUTPUT QD
tPLH
tPHL (MEASURE AT tN+10 OR tN+16) (NOTE B)
RIPPLE CARRY OUTPUT

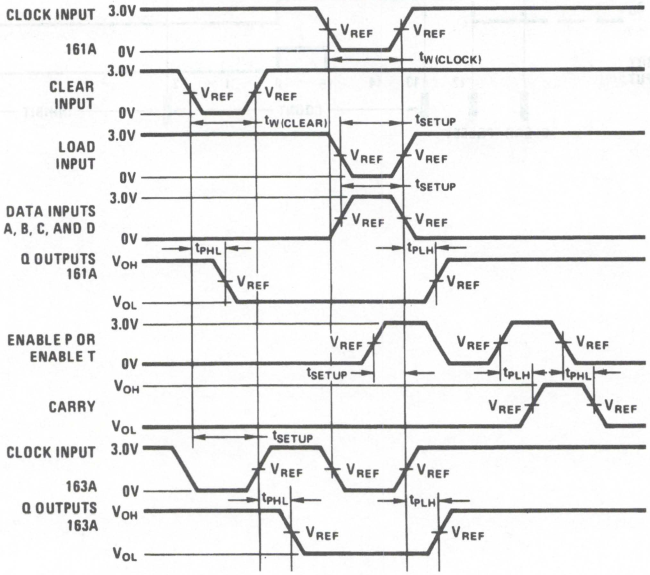
TL/F/6471–4

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. For S161/163, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at $t_n + 16$ for S161, S163 where t_n is the bit time when all outputs are low.

Note C: $V_{REF} = 1.5V$.

Switching Time Waveforms


CLOCK INPUT 161A
3.0V
0V
VREF
tW(CLOCK)
CLEAR INPUT
tW(CLEAR)
tSETUP
LOAD INPUT
tSETUP
DATA INPUTS A, B, C, AND D
tPHL
tPLH
Q OUTPUTS 161A
VOH
VOL
ENABLE P OR ENABLE T
tSETUP
tPLH
tPHL
CARRY
tSETUP
CLOCK INPUT 163A
tPHL
tPLH
Q OUTPUTS 163A

TL/F/6471–5

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. $t_r \le 2.5$ ns, $t_f \le 2.5$ ns. Vary PRR to measure f_{MAX}.

Note B: Enable P and enable T setup times are measured at $t_n + 0$.

Note C: $V_{REF} = 1.5V$.

National Semiconductor

DM54S174/DM74S174, DM54S175/DM74S175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

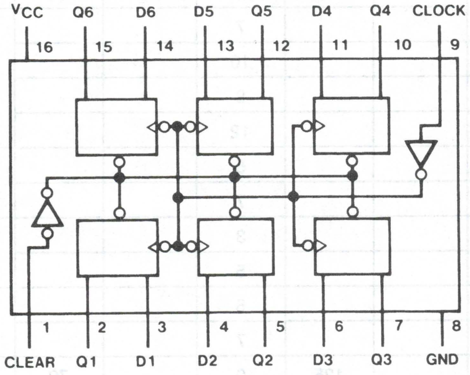
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- S174 contain six flip-flops with single-rail outputs.
- S175 contain four flip-flops with double-rail outputs.
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 110 MHz
- Typical power dissipation per flip-flop 75mW

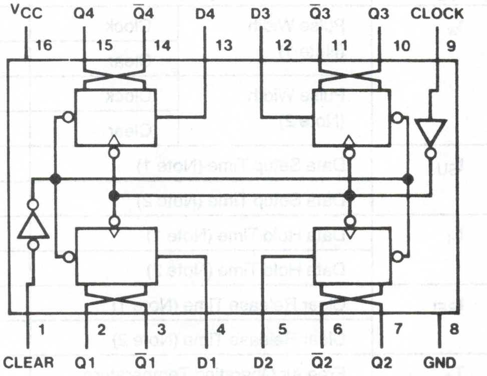
Connection Diagrams

Dual-In-Line Package


V_{CC}
Q6
D6
D5
Q5
D4
Q4
CLOCK
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
CLEAR
Q1
D1
D2
Q2
D3
Q3
GND

TL/F/6472-1

Dual-In-Line Package


V_{CC}
Q4
$\overline{Q4}$
D4
D3
$\overline{Q3}$
Q3
CLOCK
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
CLEAR
Q1
$\overline{Q1}$
D1
D2
$\overline{Q2}$
Q2
GND

TL/F/6472-2

Order Number DM54S174J, DM54S175J, DM54S175W, DM74S174N or DM74S175N
See NS Package Number J16A, N16E or W16A

Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = S175 only

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions See Section 1 for Test Waveforms and Output Load

Symbol	Parameter		DM54S174			DM74S175			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 1)		0	110	75	0	110	75	MHz
f_{CLK}	Clock Frequency (Note 2)		0	90	65	0	90	65	MHz
t_W	Pulse Width (Note 1)	Clock	7			7			ns
		Clear	10			10			
	Pulse Width (Note 2)	Clock	9			9			
		Clear	12			12			
t_{SU}	Data Setup Time (Note 1)		5			5			ns
	Data Setup Time (Note 2)		7			7			
t_H	Data Hold Time (Note 1)		3			3			ns
	Data Hold Time (Note 2)		5			5			
t_{REL}	Clear Release Time (Note 1)		5			5			ns
	Clear Release Time (Note 2)		7			7			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF, $R_L = 280\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 2: $C_L = 50$ pF, $R_L = 280\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current (S174)	V_{CC} = Max (Note 3)			90	144	mA
I_{CC}	Supply Current (S175)	V_{CC} = Max (Note 3)			60	96	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		75		65		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		17		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (S175 Only)	Clear to $\overline{Q}$		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		22		23	ns

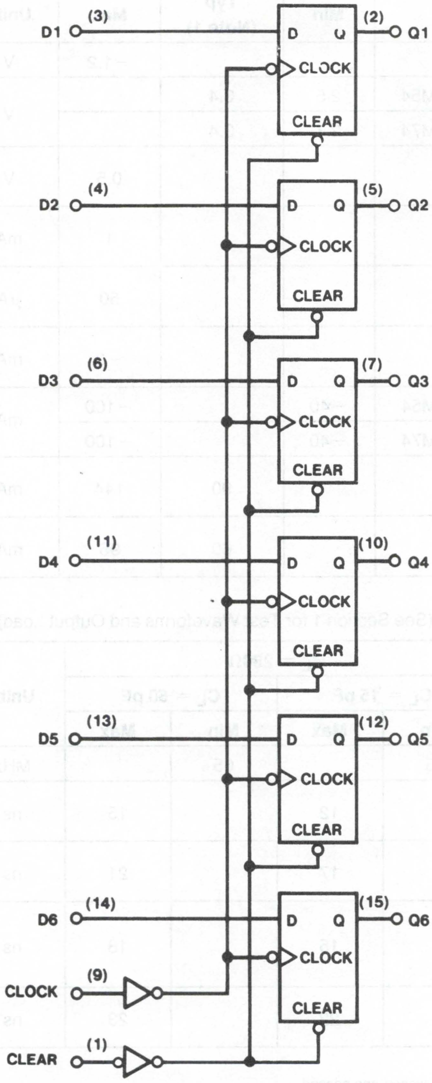
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open and 4.5V applied to all DATA and CLEAR inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the CLOCK input.

Logic Diagrams

S174


D1 (3)
D Q
CLOCK
CLEAR
(2) Q1
D2 (4)
(5) Q2
D3 (6)
(7) Q3
D4 (11)
(10) Q4
D5 (13)
(12) Q5
D6 (14)
(15) Q6
CLOCK (9)
CLEAR (1)

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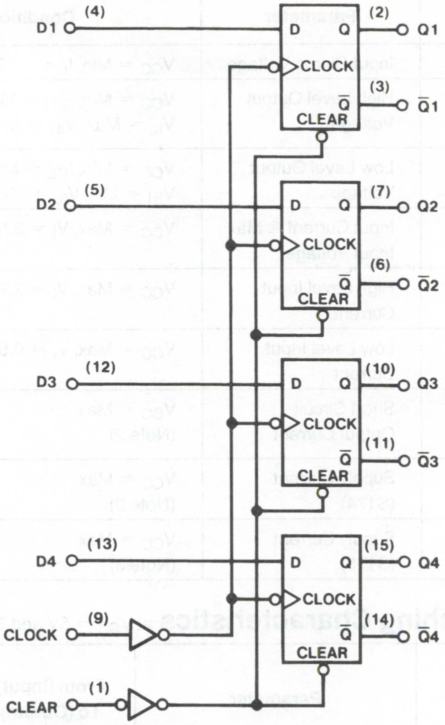
S175


D1 (4)
D Q
CLOCK
Q̄
CLEAR
(2) Q1
(3) Q̄1
D2 (5)
(7) Q2
(6) Q̄2
D3 (12)
(10) Q3
(11) Q̄3
D4 (13)
(15) Q4
(14) Q̄4
CLOCK (9)
CLEAR (1)

TL/F/6472-4

National Semiconductor

DM54S181/DM74S181 Arithmetic Logic Unit/Function Generators

General Description

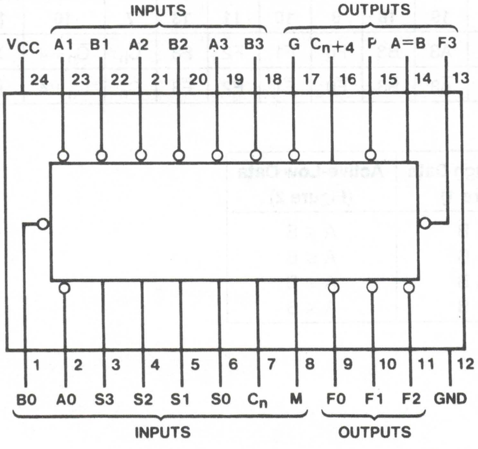
These arithmetic logic units (ALU)/function generators perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (P and G) for the four bits in the package. When used in conjunction with the DM54S182/DM74S182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown below illustrate how little time is required for addition of longer words, when full carry look-ahead is employed. The method of cascading 182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the DM54S182/DM74S182. (Continued)

Features

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - EXCLUSIVE-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high-speed operations on long words

Connection Diagram

Dual-In-Line Package



TL/F/6473–1

Order Number DM54S181J or DM74S181N
See NS Package Number J24A or N24A

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
P	15	Carry Propagate Output
$C_n + 4$	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

General Description (Continued)

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition, where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to provide A—B.

The S181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_n+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requriements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The DM54S181/DM74S181 can be used with the signal designations of either *Figure 1* or *Figure 2*.

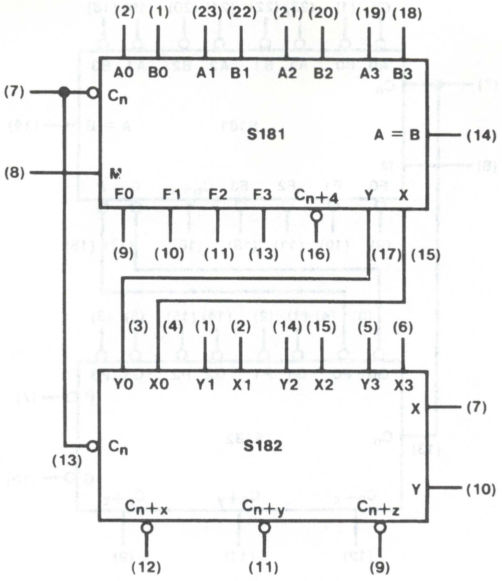
The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table I; those obtained with the signal designations of *Figure 2* are given in Table II.

Number of Bits	Typical Addition Times	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	20 ns	1	0	None
5 to 8	30 ns	2	0	Ripple
9 to 16	30 ns	3 or 4	1	Full Look-Ahead
17 to 64	50 ns	5 to 16	2 to 5	Full Look-Ahead

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table I)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_n+4$	X	Y
Active-Low Data (Table II)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_n+4	$\overline{P}$	$\overline{G}$

Input C_n	Output C_n+4	Active-High Data (Figure 1)	Active-Low Data (Figure 2)
H	H	$A \leq B$	$A \leq B$
H	L	$A \leq B$	$A \leq B$
L	H	$A \leq B$	$A \leq B$
L	L	$A \leq B$	$A \leq B$

General Description (Continued)



(2) (1) (23) (22) (21) (20) (19) (18)
A0 B0 A1 B1 A2 B2 A3 B3
(7)
C_n
S181
A = B
(14)
(8)
M
F0 F1 F2 F3 C_{n+4} Y X
(9) (10) (11) (13) (16) (17) (15)
(3) (4) (1) (2) (14) (15) (5) (6)
Y0 X0 Y1 X1 Y2 X2 Y3 X3
X
(7)
C_n
(13)
S182
Y
(10)
C_{n+x} C_{n+y} C_{n+z}
(12) (11) (9)

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FIGURE 1

TABLE I

Selection				Active High Data		
				M = H Logic Functions	M = L; Arithmetic Operations	
S3	S2	S1	S0		C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A Plus 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	$F = \overline{AB}$	$F = A + \overline{B}$	$F = (A + \overline{B})$ Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	$F = \overline{AB}$	$F = A$ Plus $A\overline{B}$	$F = A$ Plus $A\overline{B}$ Plus 1
L	H	L	H	$F = \overline{B}$	$F = (A + B)$ Plus $A\overline{B}$	$F = (A + B)$ Plus $A\overline{B}$ Plus 1
L	H	H	L	$F = A \oplus B$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ Minus 1	$F = A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	$F = (A + \overline{B})$ Plus AB	$F = (A + \overline{B})$ Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	$F = (A + \overline{B})$ Plus A	$F = (A + \overline{B})$ Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

*Each bit is shifted to the next more significant position.

General Description (Continued)

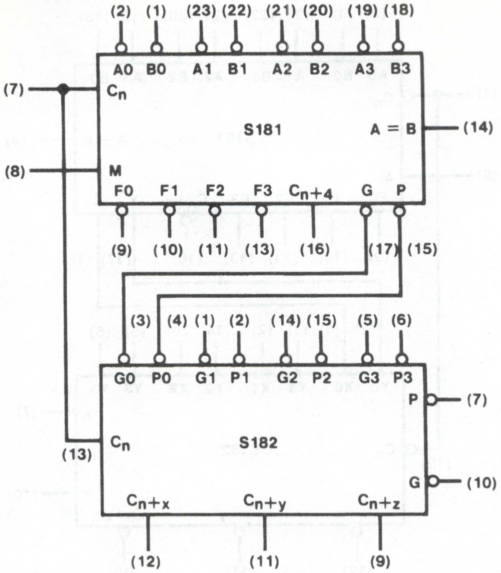
(2)
(1)
(23)
(22)
(21)
(20)
(19)
(18)
A0
B0
A1
B1
A2
B2
A3
B3
(7)
Cn
S181
A = B
(14)
(8)
M
F0
F1
F2
F3
Cn+4
G
P
(9)
(10)
(11)
(13)
(16)
(17)
(15)
(3)
(4)
(1)
(2)
(14)
(15)
(5)
(6)
G0
P0
G1
P1
G2
P2
G3
P3
P
(7)
Cn
(13)
S182
G
(10)
Cn+x
Cn+y
Cn+z
(12)
(11)
(9)

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FIGURE 2

TABLE II

Selection				Active Low Data		
				M = H Logic Functions	M = L; Arithmetic Operations	
S3	**S2**	**S1**	**S0**		C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A Minus 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	$F = \overline{A} + B$	$F = A\overline{B}$ Minus 1	$F = A\overline{B}$
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	$F = \overline{A + B}$	$F = A$ Plus $(A + \overline{B})$	$F = A$ Plus $(A + \overline{B})$ Plus 1
L	H	L	H	$F = \overline{B}$	F = AB Plus (A + B)	$F = AB$ Plus $(A + \overline{B})$ Plus 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A + \overline{B}$	$F = A + \overline{B}$	$F = (A + \overline{B})$ Plus 1
H	L	L	L	$F = \overline{A}B$	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	$F = A \oplus B$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	$F = A\overline{B}$ Plus (A + B)	$F = A\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F = A + A\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	$F = A\overline{B}$ Plus A	$F = A\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage (A = B Output)	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S181			DM74S181			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (A = B Output)			5.5			5.5	V
I_{OH}	High Level Output Current (All Except A = B)			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{CEX}	High Level Output Current (A = B Output)	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OH}	High Level Output Voltage (All Except A = B)	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Mode			50	μA
			A or B			150	
			S			200	
			Carry			250	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V	Mode			−2	mA
			A or B			−6	
			S			−8	
			Carry			−10	
I_{OS}	Short Circuit Output Current (Any Output Except A = B)	V_{CC} = Max (Note 2)		−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			120	220	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured for the following conditions: A. S0 through S3, M, and A inputs at 4.5V, all other inputs grounded and all outputs open. B. S0 through S3 and M inputs at 4.5V, all other inputs grounded and all outputs open.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM54/74 S181				Units
					$R_L = 280\Omega$, $C_L = 15$ pF		$R_L = 280\Omega$, $C_L = 50$ pF		
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		C_n	C_n+4		10.5		14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					10.5		14	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{\text{SUM}}$ mode)	Any A or B	C_n+4		18.5		22	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					18.5		22	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{\text{DIFF}}$ mode)	Any A or B	C_n+4		23		27	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					23		27	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V ($\overline{\text{SUM}}$ or $\overline{\text{DIFF}}$ mode)	C_n	Any F		12		14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12		14	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{\text{SUM}}$ mode)	Any A or B	G		12		15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12		15	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{\text{DIFF}}$ mode)	Any A or B	G		15		19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					15		20	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{\text{SUM}}$ mode)	Any A or B	P		12		15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12		15	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{\text{DIFF}}$ mode)	Any A or B	P		15		19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					15		20	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{\text{SUM}}$ mode)	A_i or B_i	F_i		16.5		20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					16.5		20	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{\text{DIFF}}$ mode)	A_i or B_i	F_i		20		24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					22		24	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 4.5V (logic mode)	A_i or B_i	F_i		20		24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					22		24	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{\text{DIFF}}$ mode)	Any A or B	A = B		23		26	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					30		33	

Parameter Measurement Information

Logic Mode Test Table
Function Inputs: S1 = S2 = M = 4.5V, S0 = S3 = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase

$\overline{\text{SUM}}$ Mode Test Table
Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	A_i	B_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} t_{PHL}	C_n	None	None	All A	All B	Any F or C_n+4	In-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase

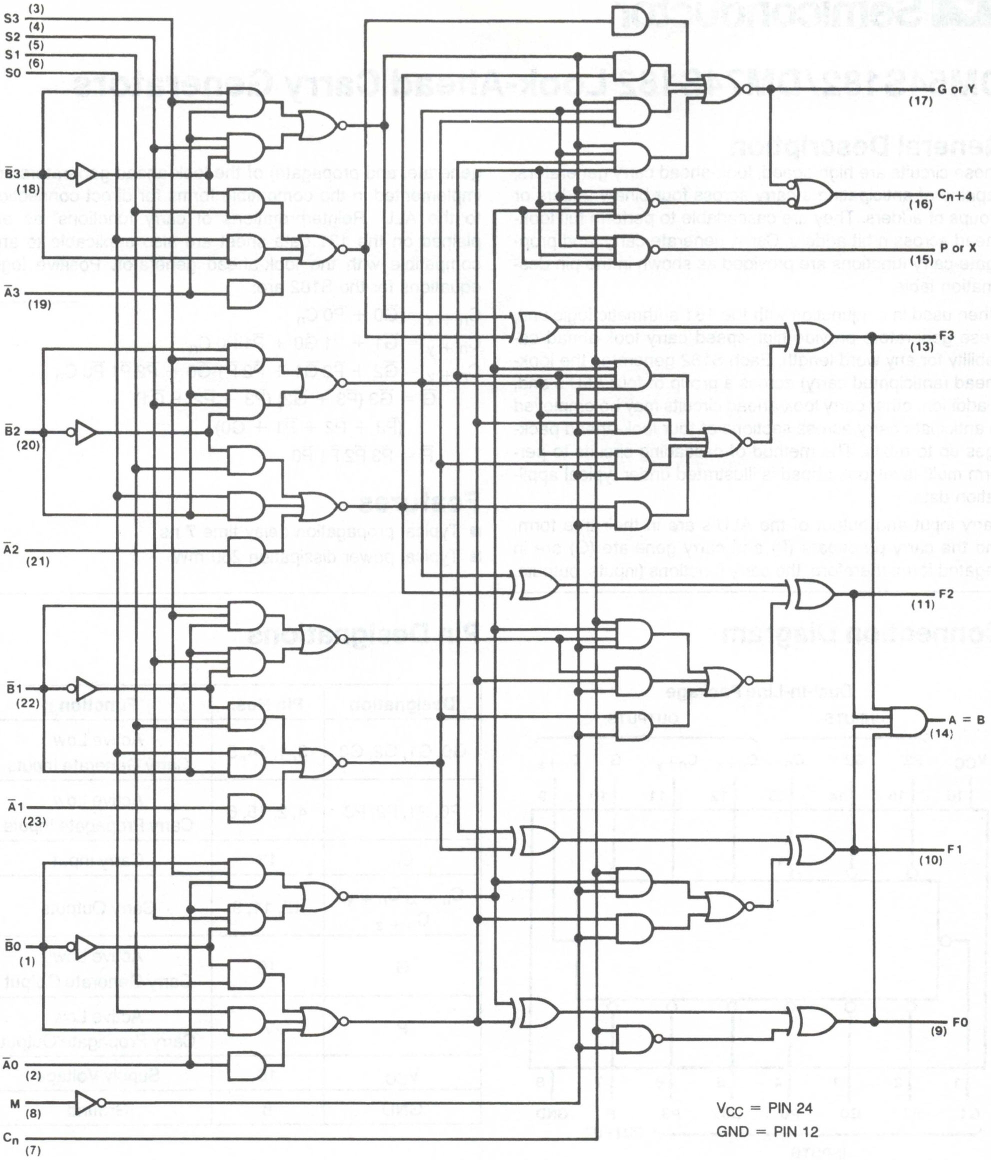
Parameter Measurement Information (Continued)

DIFF Mode Test Table

Function Inputs: S1 = S2 = 4.5V, S0 = S3 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	F_i	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	F_i	Out-of-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	G	In-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PLH} t_{PHL}	C_n	None	None	All A and B	None	$C_n + 4$ or any F	In-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A, B, C_n	$C_n + 4$	Out-of-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	None	Remaining A, B, C_n	$C_n + 4$	In-Phase

Logic Diagram


S3 (3)
S2 (4)
S1 (5)
S0 (6)
B̄3 (18)
Ā3 (19)
B̄2 (20)
Ā2 (21)
B̄1 (22)
Ā1 (23)
B̄0 (1)
Ā0 (2)
M (8)
C_n (7)
G or Y (17)
C_{n+4} (16)
P or X (15)
F3 (13)
F2 (11)
A = B (14)
F1 (10)
F0 (9)

V_{CC} = PIN 24

GND = PIN 12

TL/F/6473-4

National Semiconductor

DM54S182/DM74S182 Look-Ahead Carry Generators

General Description

These circuits are high-speed, look-ahead carry generators, capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the 181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the S182 are:

$$C_{n+x} = \overline{G0} + \overline{P0}\, C_n$$

$$C_{n+y} = \overline{G1} + \overline{P1}\,\overline{G0} + \overline{P1}\,\overline{P0}\, C_n$$

$$C_{n+z} = \overline{G2} + \overline{P2}\,\overline{G1} + \overline{P2}\,\overline{P1}\,\overline{G0} + \overline{P2}\,\overline{P1}\,\overline{P0}\, C_n$$

$$\overline{G} = \overline{G3}\,(\overline{P3} + \overline{G2})\,(\overline{P3} + \overline{P2} + \overline{G1})$$
$$(\overline{P3} + \overline{P2} + \overline{P1} + \overline{G0})$$

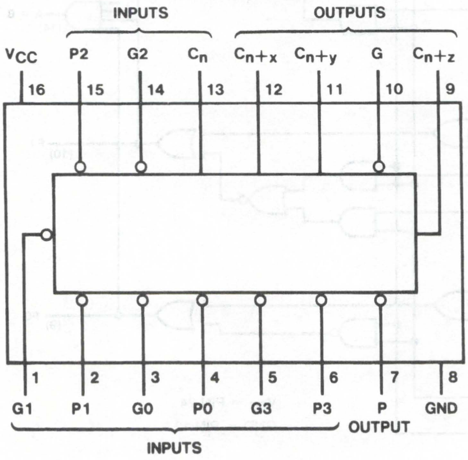
$$\overline{P} = \overline{P3}\,\overline{P2}\,\overline{P1}\,\overline{P0}$$

Features

- Typical propagation delay time 7 ns
- Typical power dissipation 260 mW

Connection Diagram

Dual-In-Line Package



TL/F/6474-1

Order Number DM54S182J or DM74S182N
See NS Package Number J16A or N16E

Pin Designations

Designation	Pin Nos.	Function
G0, G1, G2, G3	3, 1, 14, 5	Active Low Carry Generate Inputs
P0, P1, P2, P3	4, 2, 15, 6	Active Low Carry Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	Carry Outputs
G	10	Active Low Carry Generate Output
P	7	Active Low Carry Propagate Output
V_{CC}	16	Supply Voltage
GND	8	Ground

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S182			DM74S182			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	P0, P1 or G3			200	μA
			P3			100	
			P2			150	
			C_n			50	
			G0, G2			350	
			G1			400	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V	P0, P1 or G3			−8	mA
			P3			−4	
			P2			−6	
			C_n			−2	
			G0, G2			−14	
			G1			−16	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)	DM54		39	55	mA
			DM74		39	55	
I_{CCL}	Supply Currents with Outputs Low	V_{CC} = Max (Note 4)	DM54		69	99	mA
			DM74		69	109	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

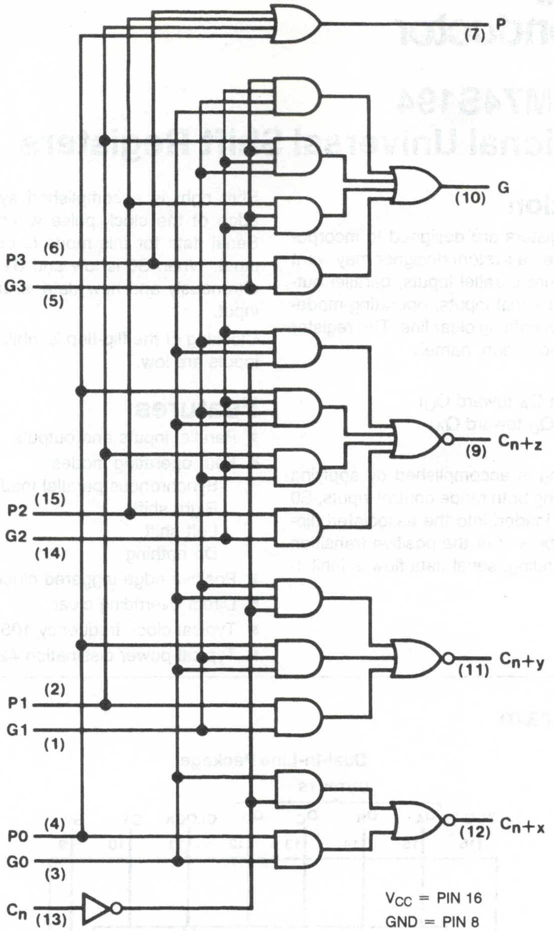
Note 3: I_{CCH} is measured with all outputs open, inputs P3 and G3 at 4.5V, and all other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open, inputs G0, G1, and G2 at 4.5V, and all other inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Min	
t_{PLH}	Propagation Delay Time Low to High Level Output	GN or PN to $C_{n\,+\,x,\,y,\,z}$		7		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	GN or PN to $C_{n\,+\,x,\,y,\,z}$		7		11	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	GN or PN to G		7.5		11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	GN or PN to G		10.5		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	PN to P		6.5		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	PN to P		10		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C_n to $C_{n\,+\,x,\,y,\,z}$		10		13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C_n to $C_{n\,+\,x,\,y,\,z}$		10.5		14	ns

Logic Diagram


(7) P
(10) G
(9) C_{n+z}
(11) C_{n+y}
(12) C_{n+x}
(6)
P3
G3
(5)
(15)
P2
G2
(14)
(2)
P1
G1
(1)
(4)
P0
G0
(3)
C_n (13)

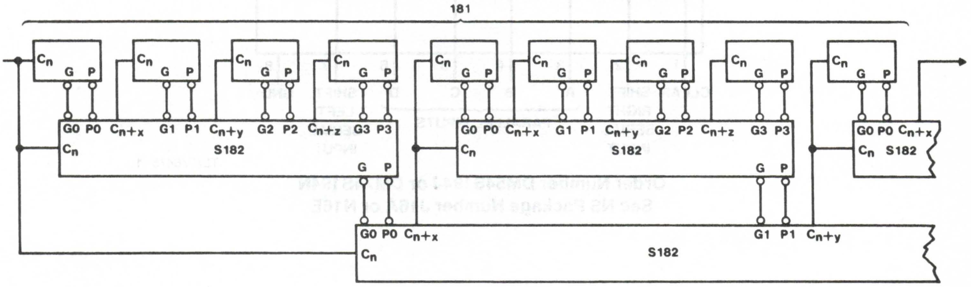
V_{CC} = PIN 16

GND = PIN 8

TL/F/6474-2

Typical Application

64-Bit ALU, Full-Carry Look Ahead in Three Levels


181
C_n
G
P
G0 P0 C_{n+x} G1 P1 C_{n+y} G2 P2 C_{n+z} G3 P3
C_n
S182
G
P
G0 P0 C_{n+x}
C_n S182
G0 P0 C_{n+x}
C_n
G1 P1 C_{n+y}
S182

TL/F/6474-3

A and B inputs, and F outputs of 181 are not shown.

National Semiconductor

DM54S194/DM74S194
4-Bit Bidirectional Universal Shift Registers

General Description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

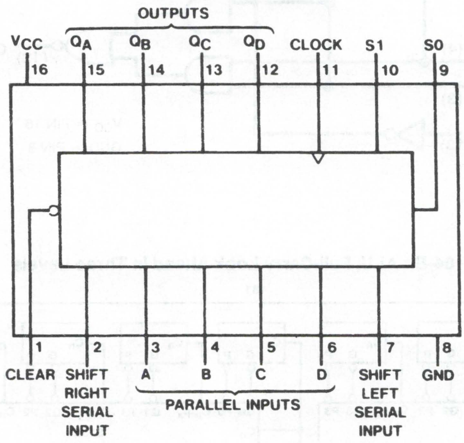
Clocking of the flip-flop is inhibited when both mode control inputs are low.

Features

- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear
- Typical clock frequency 105 MHz
- Typical power dissipation 425 mW

Connection Diagram

Dual-In-Line Package



TL/F/6475-1

Order Number DM54S194J or DM74S194N
See NS Package Number J16A or N16E

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54S194			DM74S194			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 1)		0	105	70	0	105	70	MHz
f_{CLK}	Clock Frequency (Note 2)		0	90	60	0	90	60	MHz
t_W	Pulse Width (Note 3)	Clock	7			7			ns
		Clear	12			12			
t_{SU}	Setup Time (Note 3)	Mode	11			11			ns
		Data	5			5			
t_H	Hold Time (Note 3)		3			3			ns
t_{REL}	Clear Release Time (Note 3)		9			9			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF, $R_L = 280\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 2: $C_L = 50$ pF, $R_L = 280\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, $V_I = 5.5V$				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, $V_I = 2.7V$				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, $V_I = 0.5V$				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			85	135	mA

Note 4: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the SERIAL inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CLOCK.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω C_L = 15 pF Min	R_L = 280Ω C_L = 15 pF Max	R_L = 280Ω C_L = 50 pF Min	R_L = 280Ω C_L = 50 pF Max	Units
f_{MAX}	Maximum Clock Frequency		70		60		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		16.5		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		18.5		23	ns

Function Table

Inputs										Outputs			
Clear	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S0		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state). L = Low Level (steady state). X = Don't Care (any input, including transitions).

↑ = Transition from low to high level.

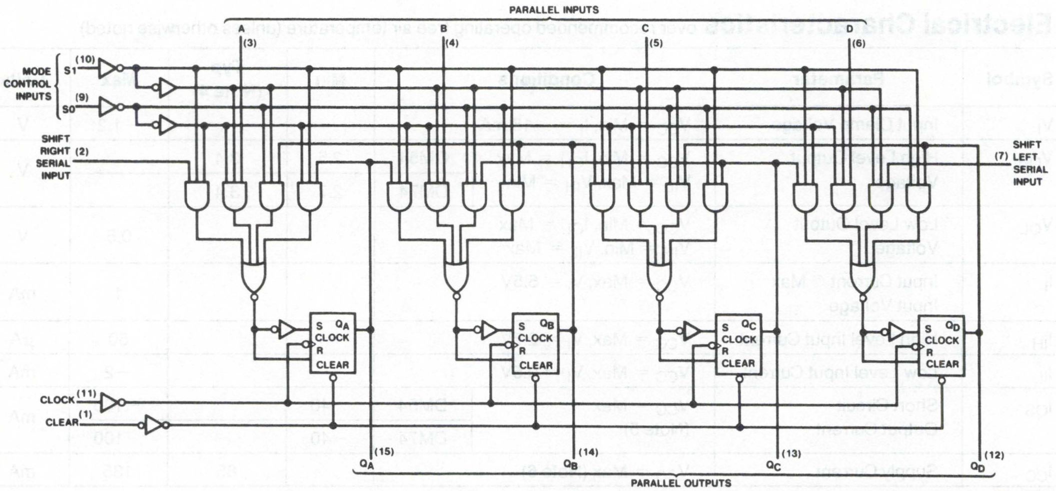
a, b, c, d = The level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C respectively, before the most recent ↑ transition of the clock.

Logic Diagram

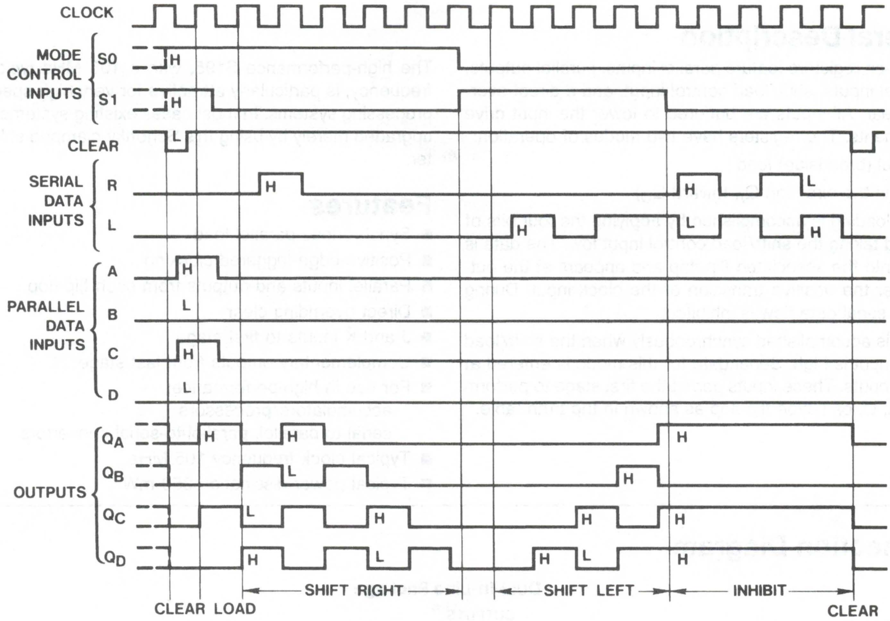
S194


PARALLEL INPUTS
A (3)
B (4)
C (5)
D (6)
MODE CONTROL INPUTS
S1 (10)
S0 (9)
SHIFT RIGHT SERIAL INPUT (2)
SHIFT LEFT SERIAL INPUT (7)
S Q_A CLOCK R CLEAR
S Q_B CLOCK R CLEAR
S Q_C CLOCK R CLEAR
S Q_D CLOCK R CLEAR
CLOCK (11)
CLEAR (1)
Q_A (15)
Q_B (14)
Q_C (13)
Q_D (12)
PARALLEL OUTPUTS

TL/F/6475–2

Timing Diagram

Typical Clear, Load, Right-Shift, Left-Shift, Inhibit, and Clear Sequences


CLOCK
MODE CONTROL INPUTS
S0
S1
H
H
CLEAR
L
SERIAL DATA INPUTS
R
L
H
H
L
H
L
H
PARALLEL DATA INPUTS
A
B
C
D
H
L
H
L
OUTPUTS
Q_A
Q_B
Q_C
Q_D
H
H
L
H
L
H
H
H
H
H
L
H
H
L
H
SHIFT RIGHT
SHIFT LEFT
INHIBIT
CLEAR
LOAD
CLEAR

TL/F/6475–3

National Semiconductor

DM54S195/DM74S195 4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load

Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T-type flip-flop as shown in the truth table.

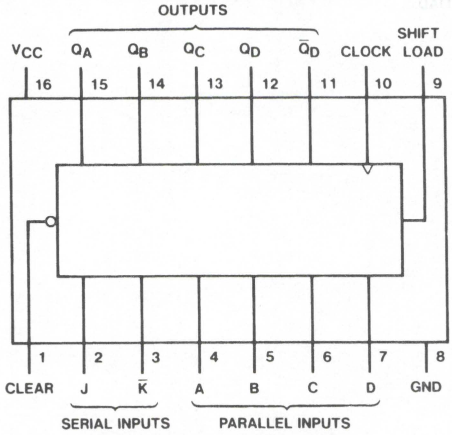
The high-performance S195, with a 105 MHz typical shift frequency, is particularly attractive for very high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- For use in high-performance:
  accumulators/processors
  serial-to-parallel, parallel-to-serial converters
- Typical clock frequency 105 MHz
- Typical power dissipation 350 mW

Connection Diagram

Dual-In-Line Package



TL/F/6476-1

Order Number DM54S195J or DM74S195N
See NS Package Number J16A or N16E

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54S195			DM74S195			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 1)		0	105	70	0	105	70	MHz
f_{CLK}	Clock Frequency (Note 2)		0	90	60	0	90	60	MHz
t_W	Pulse Width (Note 3)	Clock	7			7			ns
		Clear	12			12			
t_{SU}	Setup Time (Note 3)	Shift/Load	11			11			ns
		Data	5			5			
t_H	Data Hold Time (Note 3)		3			3			ns
t_{REL}	Shift/Load Release Time (Note 3)		6			6			ns
	Clear Release Time (Note 3)		9			9			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15\text{ pF}$, $R_L = 280\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 2: $C_L = 50\text{ pF}$, $R_L = 280\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}$, $I_I = -18\text{ mA}$				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OL} = \text{Max}$ $V_{IH} = \text{Min}$, $V_{IL} = \text{Max}$				0.5	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$, $V_I = 5.5V$				1	mA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}$, $V_I = 2.7V$				50	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}$, $V_I = 0.5V$				−2	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 5)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 6)			70	109	mA

Note 4: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all inputs open, SHIFT/LOAD grounded, and 4.5V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, then 4.5V to the CLEAR and then applying a momentary ground then 4.5V to the CLOCK.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		70		60		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		16.5		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		18.5		23	ns

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

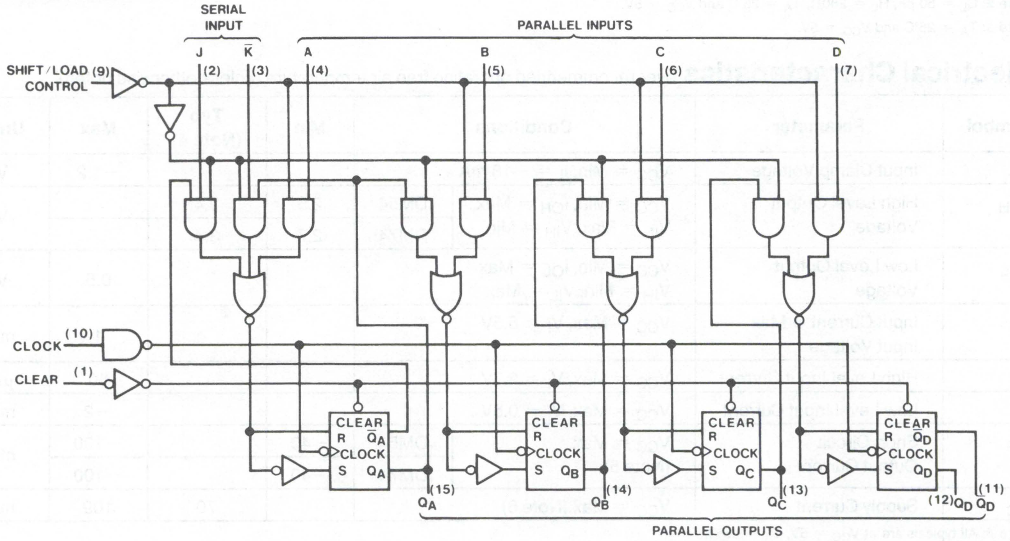
↑ = Transition from low to high level

a, b, c, d = The level of steady state input at A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent transition of the clock.

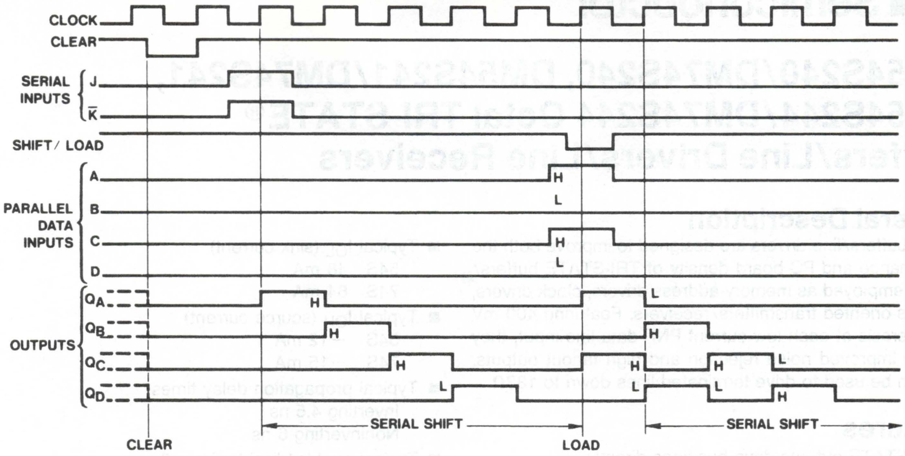
Logic Diagram


SERIAL INPUT
J
K̄
PARALLEL INPUTS
A
B
C
D
(2)
(3)
(4)
(5)
(6)
(7)
SHIFT/LOAD CONTROL (9)
CLOCK (10)
CLEAR (1)
CLEAR
R
CLOCK
S
Q̄A
QA
QB
QC
QD
Q̄D
(15)
(14)
(13)
(12)
(11)
PARALLEL OUTPUTS

TL/F/6476-2

Timing Diagram

Typical Clear, Shift, and Load Sequences


CLOCK
CLEAR
SERIAL INPUTS
J
K̄
SHIFT/ LOAD
PARALLEL DATA INPUTS
A
B
C
D
H
L
H
L
OUTPUTS
QA
QB
QC
QD
H
H
H
L
L
H
H
L
L
H
L
L
H
SERIAL SHIFT
SERIAL SHIFT
CLEAR
LOAD

TL/F/6476-3

National Semiconductor

DM54S240/DM74S240, DM54S241/DM74S241, DM54S244/DM74S244 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

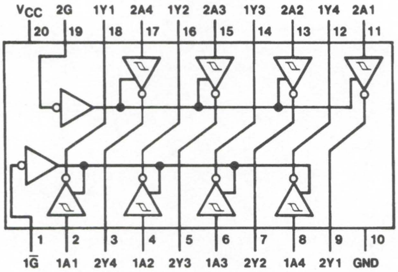
These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs, and can be used to drive terminated lines down to 133Ω.

Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at data inputs improves noise margins
- Typical I_{OL} (sink current)
  - 54S 48 mA
  - 74S 64 mA
- Typical I_{OH} (source current)
  - 54S −12 mA
  - 74S −15 mA
- Typical propagation delay times
  - Inverting 4.5 ns
  - Noninverting 6 ns
- Typical enable/disable times 9 ns
- Typical power dissipation (enabled)
  - Inverting 450 mW
  - Noninverting 538 mW

Connection Diagrams

Dual-In-Line Package

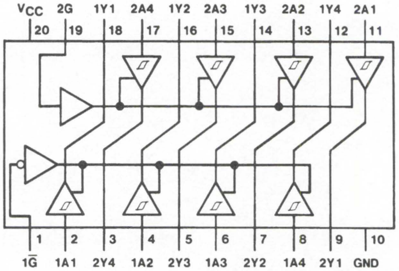


V_{CC}
2G
1Y1
2A4
1Y2
2A3
1Y3
2A2
1Y4
2A1
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
1G̅
1A1
2Y4
1A2
2Y3
1A3
2Y2
1A4
2Y1
GND

TL/F/6478-1

Order Number DM54S240J, DM74S240WM or DM74S240N
See NS Package Number J20A, M20B or N20A

Dual-In-Line Package

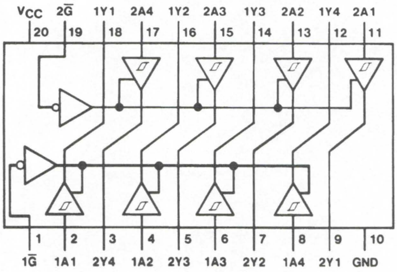


V_{CC}
2G
1Y1
2A4
1Y2
2A3
1Y3
2A2
1Y4
2A1
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
1G̅
1A1
2Y4
1A2
2Y3
1A3
2Y2
1A4
2Y1
GND

TL/F/6478-2

Order Number DM54S241J or DM74S241N
See NS Package Number J20A or N20A

Dual-In-Line Package



V_{CC}
2G̅
1Y1
2A4
1Y2
2A3
1Y3
2A2
1Y4
2A1
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
1G̅
1A1
2Y4
1A2
2Y3
1A3
2Y2
1A4
2Y1
GND

TL/F/6478-3

Order Number DM54S244J, DM74S244WM or DM74S244N
See NS Package Number J20A, M20B or N20A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S			DM74S			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			48			64	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.2	V
H_{ys}	Hysteresis ($V_{T+} - V_{T-}$) (Data Inputs Only)	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −3 mA			2.4	3.4		
		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.5V, I_{OH} = Max			2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = Max	DM54			0.55	V
				DM74			0.55	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max V_{IL} = 0.8V V_{IH} = 2V	V_O = 2.4V				50	µA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.5V				−50	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.7V				50	µA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.5V	Any A			−400	µA
				Any G			−2	mA

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−50		−225	mA
I_{CC}	Supply Current	Outputs High	DM54S240		80	123	mA
			DM74S240		80	135	
			DM54S241, 244		95	147	
			DM74S241, 244		95	160	
		Outputs Low	DM54S240		100	145	
			DM74S240		100	150	
			DM54S241, 244		120	170	
			DM74S241, 244		120	180	
		Outputs Disabled	DM54S240		100	145	
			DM74S240		100	150	
			DM54S241, 244		120	170	
			DM74S241, 244		120	180	

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time and duration should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions		Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF R_L = 90Ω	DM54/74S240	2	7	ns
			DM54/74S241, 244	2	9	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 45 pF R_L = 90Ω	DM54/74S240	2	7	ns
			DM54/74S241, 244	2	9	
t_{PZL}	Output Enable Time to Low Level	C_L = 45 pF R_L = 90Ω	DM54/74S240	3	15	ns
			DM54/74S241, 244	3	15	
t_{PZH}	Output Enable Time to High Level	C_L = 45 pF R_L = 90Ω	DM54/74S240	2	10	ns
			DM54/74S241, 244	3	12	
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF R_L = 90Ω	DM54/74S240	4	15	ns
			DM54/74S241, 244	2	15	
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF R_L = 90Ω	DM54/74S240	2	9	ns
			DM54/74S241, 244	2	9	
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 150 pF R_L = 90Ω	DM54/74S240	3	10	ns
			DM54/74S241, 244	4	12	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 150 pF R_L = 90Ω	DM54/74S240	3	10	ns
			DM54/74S241, 244	4	12	
t_{PZL}	Output Enable Time to Low Level	C_L = 150 pF R_L = 90Ω	DM54/74S240	6	21	ns
			DM54/74S241, 244	6	21	
t_{PZH}	Output Enable Time to High Level	C_L = 150 pF R_L = 90Ω	DM54/74S240	4	12	ns
			DM54/74S241, 244	4	15	

National Semiconductor

DM54S251/DM74S251 TRI-STATE® 1 of 8 Line Data Selector/Multiplexer

General Description

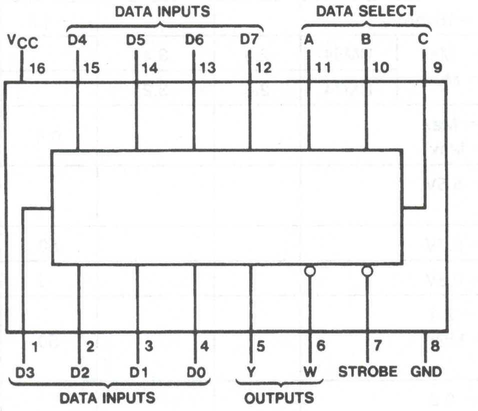
These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

Features

- TRI-STATE version of S151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data
- Max no. of common outputs
  - 54S 39
  - 74S 129
- Typical propagation delay time (D to Y) 8 ns
- Typical power dissipation 275 mW

Connection Diagram



TL/F/6480-1

Order Number DM54S251J or DM74S251N
See NS Package Number J16A or N16E

Function Table

Inputs				Outputs	
Select			Strobe S	Y	W
C	B	A			
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level
X = Don't Care, Z = High Impedance (Off)
D0, D1 . . . D7 = The Level of the respective D input

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S251			DM74S251			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−6.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4 V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5 V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			55	85	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

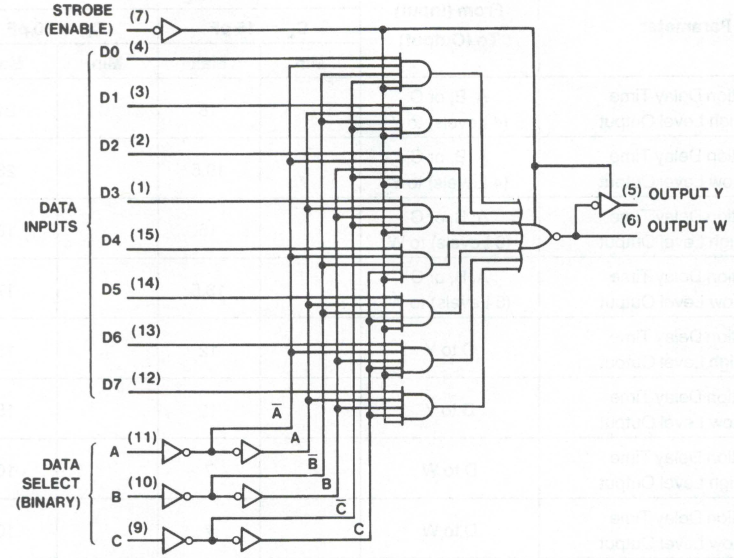
Note 3: I_{CC} is measured with the outputs open and all inputs at 4.5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, or C (4 Levels) to Y		18		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, or C (4 Levels) to Y		19.5		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, or C (3 Levels) to W		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, or C (3 Levels) to W		13.5		17	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to Y		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to Y		12		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to W		7		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to W		7		10	ns
t_{PZH}	Output Enable Time to High Level Output	Strobe to Y				19.5	ns
t_{PZL}	Output Enable Time to Low Level Output	Strobe to Y				21	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	Strobe to Y		8.5			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	Strobe to Y		14			ns
t_{PZH}	Output Enable Time to High Level Output	Strobe to W				19.5	ns
t_{PZL}	Output Enable Time to Low Level Output	Strobe to W				21	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	Strobe to W		8.5			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	Strobe to W		14			ns

Note 1: C_L = 5 pF.

Logic Diagram


STROBE (ENABLE) (7)
D0 (4)
D1 (3)
D2 (2)
D3 (1)
DATA INPUTS
D4 (15)
D5 (14)
D6 (13)
D7 (12)
$\overline{A}$
A (11)
A
$\overline{B}$
DATA SELECT (BINARY)
B (10)
B
$\overline{C}$
C (9)
C
(5) OUTPUT Y
(6) OUTPUT W

TL/F/6480-2

National Semiconductor

DM54S253/DM74S253
Dual TRI-STATE® 1 of 4 Line Data Selectors/Multiplexers

General Description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

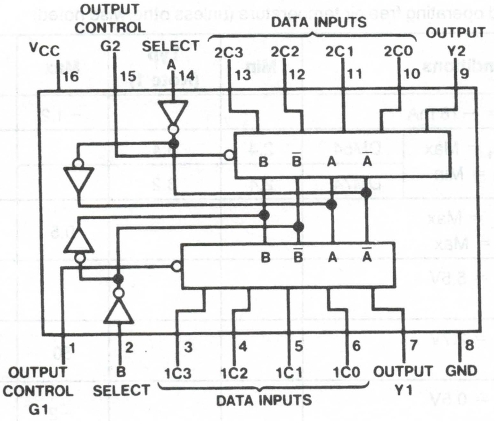
The TRI-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enable output will drive the bus line to a high or low logic level.

Features

- TRI-STATE version of S153 with same pin-out
- Schottky-diode-clamped transistors
- Permits multiplexing from N lines to 1 line
- Performs parallel-T-serial conversion
- Strobe/output control
- High fan-out totem-pole outputs
- Typical propagation delay
  - From data to output 6 ns
  - From select to output 12 ns
- Typical power dissipation 275 mW

Connection Diagram

Dual-In-Line Package



OUTPUT CONTROL G2
SELECT A
DATA INPUTS
OUTPUT Y2
V_{CC}
16
15
14
2C3
13
2C2
12
2C1
11
2C0
10
9
B
$\overline{B}$
A
$\overline{A}$
B
$\overline{B}$
A
$\overline{A}$
1
2
3
4
5
6
7
8
OUTPUT CONTROL G1
B SELECT
1C3
1C2
1C1
1C0
DATA INPUTS
OUTPUT Y1
GND

TL/F/6481–1

Order Number DM54S253J, DM54S253W or DM74S253N
NS Package Number J16A, N16E or W16A

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	**A**	**C0**	**C1**	**C2**	**C3**	**G**	**Y**
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S253			DM74S253			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−6.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			55	70	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

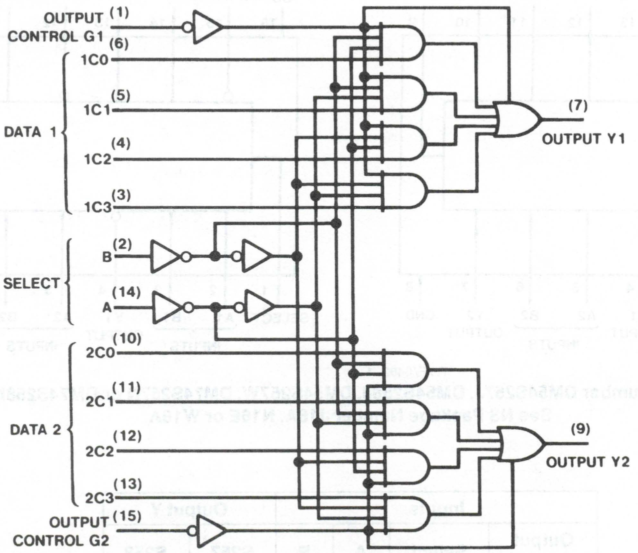
Note 3: I_{CC} is measured with all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			$C_L = 15$ pF		$C_L = 50$ pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		9		12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		9		12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		18		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		18		21	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		16.5		19.5	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		18		21	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	Output Control to Y		9.5			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	Output Control to Y		15			ns

Note 1: $C_L = 5$ pF.

Logic Diagram


OUTPUT CONTROL G1 (1)
(6) 1C0
(5) 1C1
DATA 1
(4) 1C2
(3) 1C3
(2) B
SELECT
(14) A
(10) 2C0
(11) 2C1
DATA 2
(12) 2C2
(13) 2C3
OUTPUT CONTROL G2 (15)
(7) OUTPUT Y1
(9) OUTPUT Y2

TL/F/6481–2

National Semiconductor

DM54S257/DM74S257, DM54S258/DM74S258 TRI-STATE® Quad 1 of 2 Data Selectors/Multiplexers

General Description

These Schottky-clamped high-performance multiplexers feature TRI-STATE outputs that can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times.

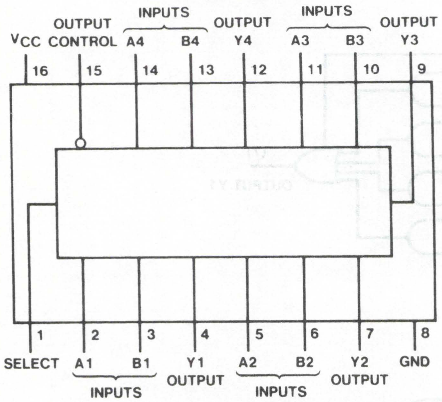
This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Features

- TRI-STATE versions S157, S158, with same pin-outs
- Schottky-clamped for significant improvement in A-C performance
- Provides bus interface from multiple sources in high-performance systems
- Average propagation delay from data input
  S257 4.8 ns
  S258 4 ns
- Typical power dissipation
  S257 320 mW
  S258 280 mW

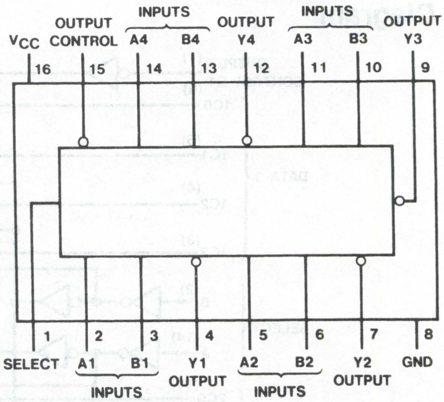
Connection Diagrams

Dual-In-Line Package


VCC
OUTPUT CONTROL
INPUTS
A4
B4
OUTPUT Y4
INPUTS
A3
B3
OUTPUT Y3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
SELECT
A1
B1
INPUTS
Y1 OUTPUT
A2
B2
INPUTS
Y2 OUTPUT
GND

TL/F/6482–1

Dual-In-Line Package


VCC
OUTPUT CONTROL
INPUTS
A4
B4
OUTPUT Y4
INPUTS
A3
B3
OUTPUT Y3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
SELECT
A1
B1
INPUTS
Y1 OUTPUT
A2
B2
INPUTS
Y2 OUTPUT
GND

TL/F/6482–2

Order Number DM54S257J, DM54S258J, DM54S257W, DM74S257N or DM74S258N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs				Output Y	
Output Control	**Select**	**A**	**B**	**S257**	**S258**
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care
Z = High Impedance (off)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S257			DM74S257			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−6.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'S257 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Select			100	μA
			Other			50	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Select			−4	mA
			Other			−2	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			44	68	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 3)			60	93	mA
I_{CCZ}	Supply Current with Outputs Disabled	V_{CC} = Max (Note 3)			64	99	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

'S257 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω C_L = 15 pF Min		C_L = 50 pF Min		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		7.5		11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		6.5		10	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		15		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		15		16	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		19.5		23	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		21		24	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	Output Control to Y		8.5			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	Output Control to Y		14			ns

Note 1: C_L = 5 pF.

Recommended Operating Conditions

Symbol	Parameter	DM54S258			DM74S258			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−6.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'S258 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Select			100	μA
			Other			50	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Select			−4	mA
			Other			−2	

’S258 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			36	56	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 3)			52	81	mA
I_{CCZ}	Supply Current with Outputs Disabled	V_{CC} = Max (Note 3)			56	87	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

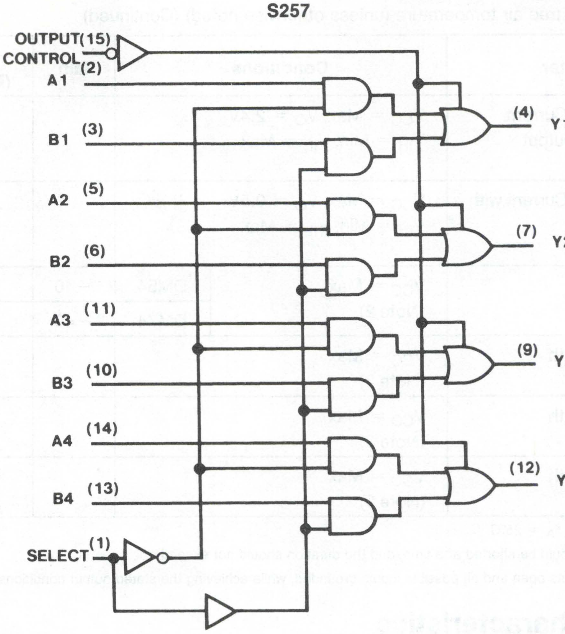
’S258 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

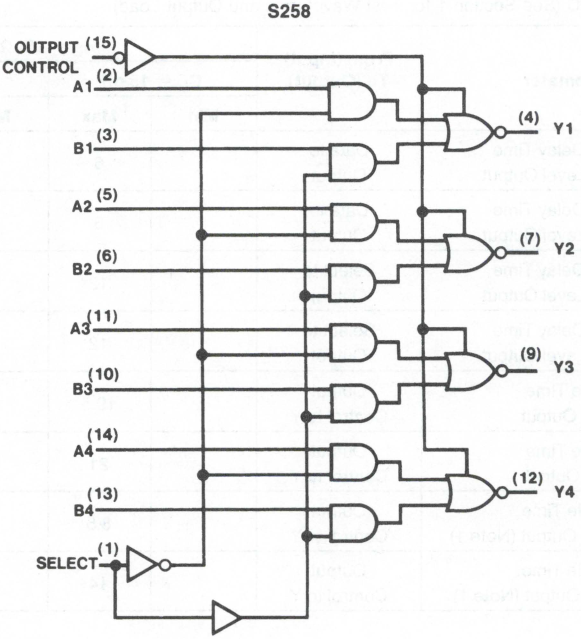
Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		6		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		6		9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		12		15	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		19.5		23	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		21		24	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	Output Control to Y		8.5			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	Output Control to Y		14			ns

Note 1: C_L = 5 pF.

Logic Diagrams


S257
OUTPUT
CONTROL
(15)
A1
(2)
B1
(3)
A2
(5)
B2
(6)
A3
(11)
B3
(10)
A4
(14)
B4
(13)
SELECT
(1)
(4)
Y1
(7)
Y2
(9)
Y3
(12)
Y4

TL/F/6482-3


S258
OUTPUT
CONTROL
(15)
A1
(2)
B1
(3)
A2
(5)
B2
(6)
A3
(11)
B3
(10)
A4
(14)
B4
(13)
SELECT
(1)
(4)
Y1
(7)
Y2
(9)
Y3
(12)
Y4

TL/F/6482-4

National Semiconductor

DM54S280/DM74S280 9-Bit Parity Generators/Checkers

General Description

These universal, nine-bit parity generators/checkers utilize Schottky-clamped TTL high-performance circuitry, and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word-length capability is easily expanded by cascading.

The S280 can be used to upgrade the performance of most systems utilizing the DM74180 parity generator/checker. Although the S280 is implemented without expander inputs, the corresponding function is provided by the availability of all input at pin 4, and no internal connection at pin 3. This permits the S280 to be substituted for the 180 in existing designs to produce an identical function, even if S280's are mixed with existing 180's.

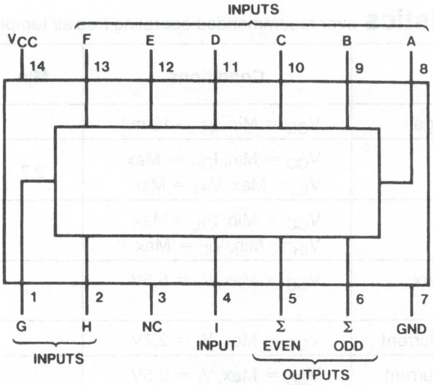
Input buffers are provided so that each input represents only one normal 74S load, and full fan-out to 10 normal Series 74S loads is available from each of the outputs at low logic levels. A fan-out to 20 normal Series 74S loads is provided at high logic levels, to facilitate connection of unused inputs to used inputs.

Features

- Generates either odd or even parity for nine data lines
- Cascadable for N-bits
- Can be used to upgrade existing systems using MSI parity circuits
- Typical data-to-output delay—14 ns

Connection Diagram

Dual-In-Line Package



TL/F/6483–1

Order Number DM54S280J, DM54S280W, DM74S280M or DM74S280N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

Number of Inputs (A Thru I) that are High	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S280			DM74S280			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} Max (Note 3)			67	105	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

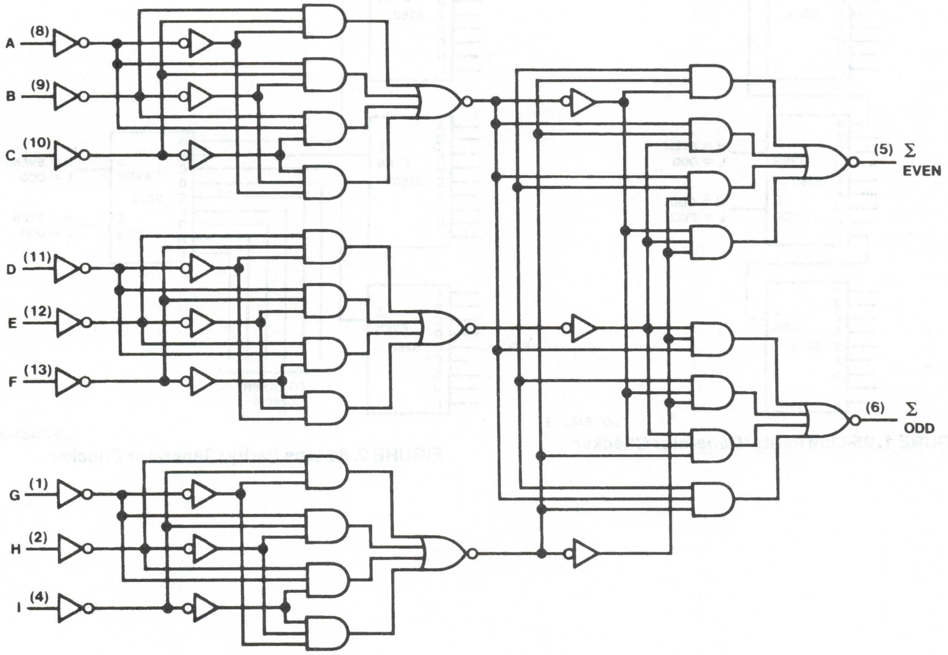
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω C_L = 15 pF		R_L = 280Ω C_L = 50 pF		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Even		21		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Even		18		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Odd		21		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Odd		18		21	ns

Logic Diagram



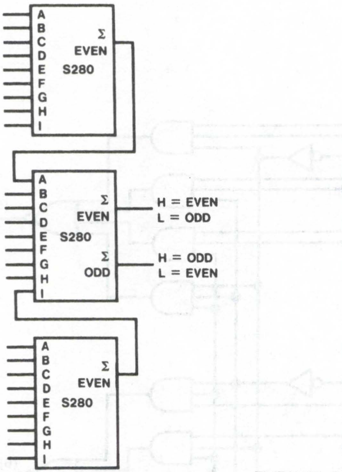
TL/F/6483-2

Typical Applications

Three S280's can be used to implement a 25-line parity generator/checker. This arrangement will provide parity in typically 25 ns. (See *Figure 1*.)

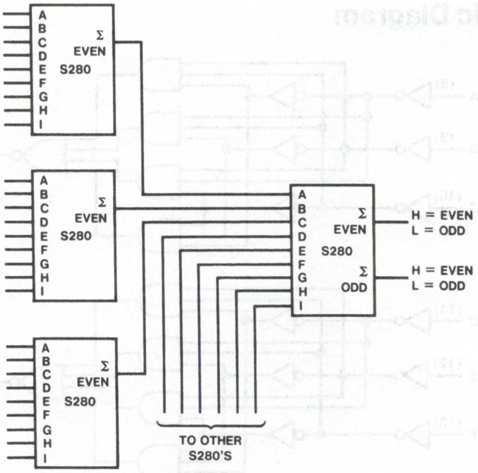
As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input (S86) or 3-input (S135) exclusive-OR gate for 18 or 27-line parity applications.

Longer word lengths can be implemented by cascading S280's. As shown in *Figure 2*, parity can be generated for word lengths up to 81 bits in typically 25 ns.


A
B
C
D
E
F
G
H
I
Σ
EVEN
S280
Σ
ODD
H = EVEN
L = ODD
H = ODD
L = EVEN

TL/F/6483-3

FIGURE 1. 25-Line Parity/Generator Checker


A
B
C
D
E
F
G
H
I
Σ
EVEN
S280
Σ
ODD
H = EVEN
L = ODD
H = EVEN
L = ODD
TO OTHER
S280'S

TL/F/6483-4

FIGURE 2. 81-Line Parity/Generator Checker

National Semiconductor

DM54S283/DM74S283 4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

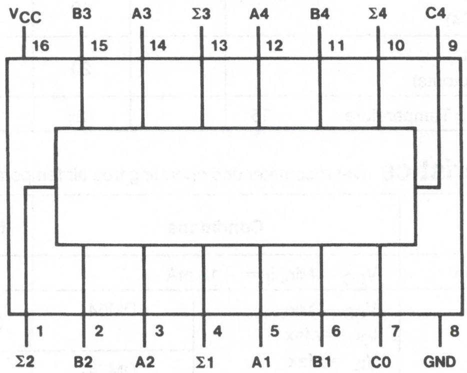
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  Two 8-bit words 15 ns
  Two 16-bit words 30 ns
- Typical power dissipation 510 mW

Connection Diagram

Dual-In-Line Package



TL/F/6484-1

Order Number DM54S283J or DM74S283N
See NS Package Number J16A or N16E

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S283			DM74S283			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current (Output C4)			−0.5			−0.5	mA
	High Level Output Current (Other Outputs)			−1			−1	
I_{OL}	Low Level Output Current (Output C4)			10			10	mA
	Low Level Output Current (Other Outputs)			20			20	
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min I_{OH} = Max V_{IL} = Max V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	C4 Output	−20		−100	mA
			Other Outputs	−40		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			80	120	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			95	160	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, all B inputs low and all other inputs at 4.5V.

Note 4: I_{CC2} is measured with all outputs open and all inputs at 4.5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω, C_L = 15 pF Min	R_L = 280Ω, C_L = 15 pF Max	R_L = 280Ω, C_L = 50 pF Min	R_L = 280Ω, C_L = 50 pF Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to $\Sigma1$ or $\Sigma2$		18		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to $\Sigma1$ or $\Sigma2$		18		20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to $\Sigma3$		18		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to $\Sigma3$		18		20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to $\Sigma4$		18		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to $\Sigma4$		18		20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i, B_i to S_i		18		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i, B_i to S_i		18		20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (Note 1)	C0 to $\Sigma4$		11		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 1)	C0 to $\Sigma4$		11		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (Note 1)	A_i, B_i to C4		12		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 1)	A_i, B_i to C4		12		16	ns

Note 1: R_L = 560Ω.

Function Table

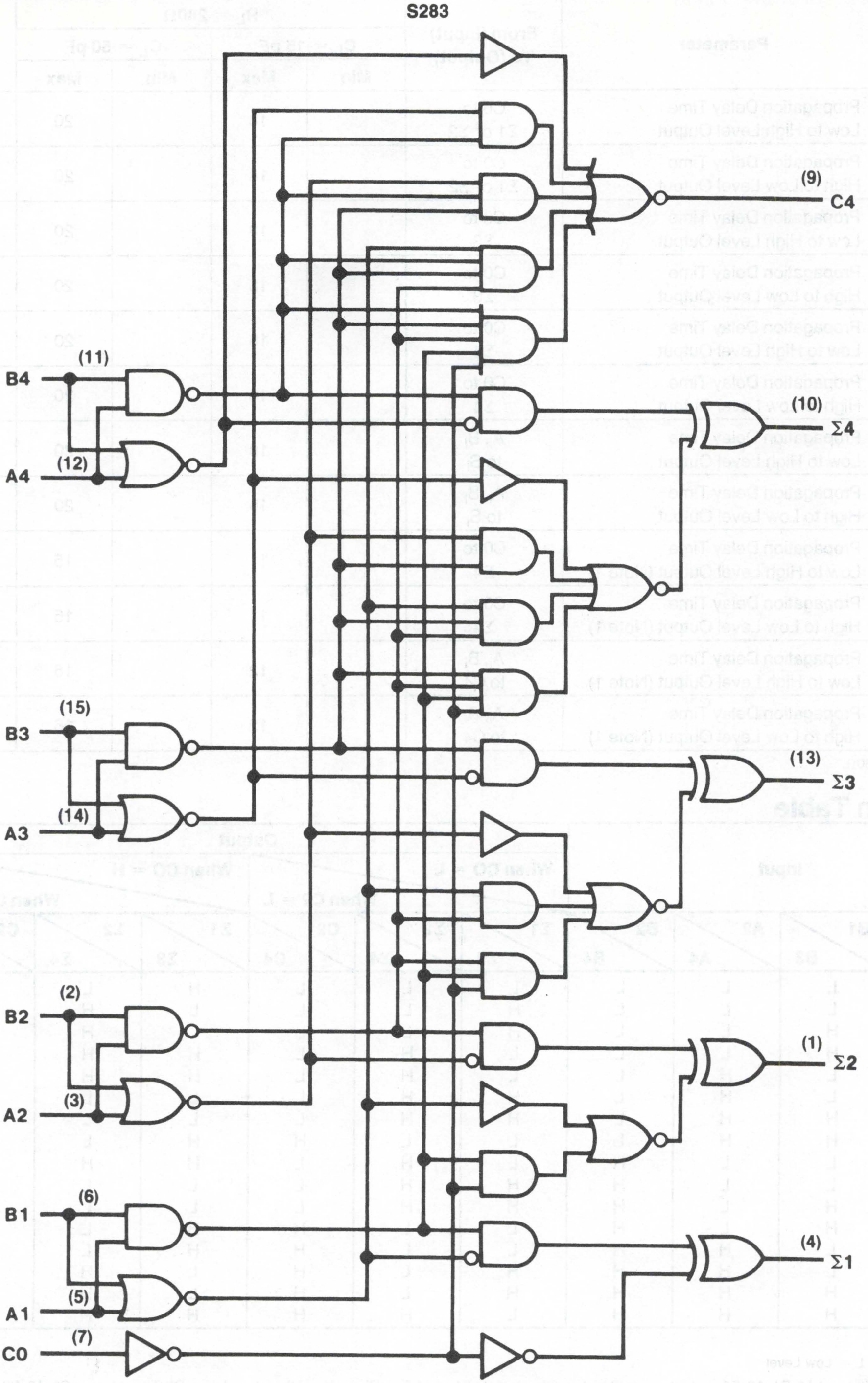
Input				Output: When CO = L / When C2 = L			Output: When CO = H / When C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	$\Sigma1$ / $\Sigma3$	$\Sigma2$ / $\Sigma4$	C2 / C4	$\Sigma1$ / $\Sigma3$	$\Sigma2$ / $\Sigma4$	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = High Level, L = Low Level

TL/F/6484-3

Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs $\Sigma1$ and $\Sigma2$ and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs $\Sigma3$, $\Sigma4$, and C4.

Logic Diagram


S283
(9)
C4
(11)
B4
(12)
A4
(10)
Σ4
(15)
B3
(14)
A3
(13)
Σ3
(2)
B2
(3)
A2
(1)
Σ2
(6)
B1
(5)
A1
(4)
Σ1
(7)
C0

TL/F/6484-2

National Semiconductor

DM74S299
TRI-STATE® 8-Bit Universal Shift/Storage Registers

Description

This Schottky TTL eight-bit universal register features multiplexed inputs/outputs to achieve full eight bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

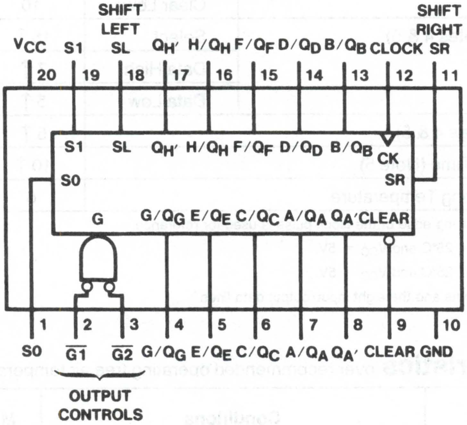
Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the TRI-STATE outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

Features

- Multiplexed inputs/outputs provide improved bit density
- Four modes of operation:
  - Hold (Store) Shift Left
  - Shift Right Load Data
- TRI-STATE outputs drive bus lines directly
- Can be cascaded for N-bit word lengths
- Operates with outputs enabled or at high Z
- Guaranteed shift (clock) frequency 50 MHz
- Typical power dissipation 700 mW

Connection Diagram

Dual-In-Line Package


SHIFT LEFT
SHIFT RIGHT
V_{CC}
S1
SL
$Q_{H'}$
H/Q_H
F/Q_F
D/Q_D
B/Q_B
CLOCK
SR
20
19
18
17
16
15
14
13
12
11
S1
SL
$Q_{H'}$
H/Q_H
F/Q_F
D/Q_D
B/Q_B
CK
S0
SR
G
G/Q_G
E/Q_E
C/Q_C
A/Q_A
$Q_{A'}$
CLEAR
1
2
3
4
5
6
7
8
9
10
S0
$\overline{G1}$
$\overline{G2}$
G/Q_G
E/Q_E
C/Q_C
A/Q_A
$Q_{A'}$
CLEAR
GND
OUTPUT CONTROLS

TL/F/6485–1

Order Number DM74S299N
See NS Package Number N20A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range DM74S	 0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM74S299 Min	DM74S299 Nom	DM74S299 Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current (Q_A thru Q_H)				−6.5	mA
	High Level Output Current ($Q_{A'}$, $Q_{H'}$)				−0.5	
I_{OL}	Low Level Output Current (Q_A thru Q_H)				20	mA
	High Level Output Current ($Q_{A'}$, $Q_{H'}$)				6	
f_{CLK}	Clock Frequency (Note 2)		0	70	50	MHz
f_{CLK}	Clock Frequency (Note 3)		0	60	40	MHz
t_W	Pulse Width (Note 5)	Clock High	10			ns
		Clock Low	10			
		Clear Low	10			
t_{SU}	Setup Time (Notes 4 & 5)	Select	15 ↑			ns
		Data High	7 ↑			
		Data Low	5 ↑			
t_H	Hold Time (Notes 4 & 5)		5 ↑			ns
t_{REL}	Clear Release Time (Note 5)		10 ↑			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: Data includes the two serial inputs and the eight input/output data lines.

Note 5: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	Q_A thru Q_H	2.4	3.2		V
			$Q_{A'}$, $Q_{H'}$	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	A thru H, S0, S1			100	μA
			Any Other			50	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V	Clock, Clear			−2	mA
			S0, S1			−0.5	
			Other			−0.25	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied (Q_A thru Q_H)	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				100	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied (Q_A thru Q_H)	V_{CC} = Max, V_O = 0.5V V_{IH} = Min, V_{IL} = Max				−250	μA
I_{OS}	Short Circuit Output Current (Q_A thru Q_H)	V_{CC} = Max (Note 2)		−40		−100	mA
	Short Circuit Output Current ($Q_{A'}$, $Q_{H'}$)	V_{CC} = Max (Note 2)		−20		−100	
I_{CC}	Supply Current	V_{CC} = Max			140	225	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω (Note 2)				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	(Note 3)	50		40		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output (Note 2)	Clock to $Q_{A'}$ or $Q_{H'}$		20		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 2)	Clock to $Q_{A'}$ or $Q_{H'}$		20		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q_A thru Q_H				21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q_A thru Q_H				21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 2)	Clear to $Q_{A'}$ or $Q_{H'}$		21		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q_A thru Q_H				24	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}1$, $\overline{G}2$ to Q_A thru Q_H				18	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}1$, $\overline{G}2$ to Q_A thru Q_H				18	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	$\overline{G}1$, $\overline{G}2$ to Q_A thru Q_H		12			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	$\overline{G}1$, $\overline{G}2$ to Q_A thru Q_H		12			ns

Note 1: C_L = 5 pF.

Note 2: R_L = 1KΩ for delays measured to $Q_{A'}$ and $Q_{H'}$.

Note 3: For testing f_{MAX} all outputs are loaded simultaneously.

Function Table

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected

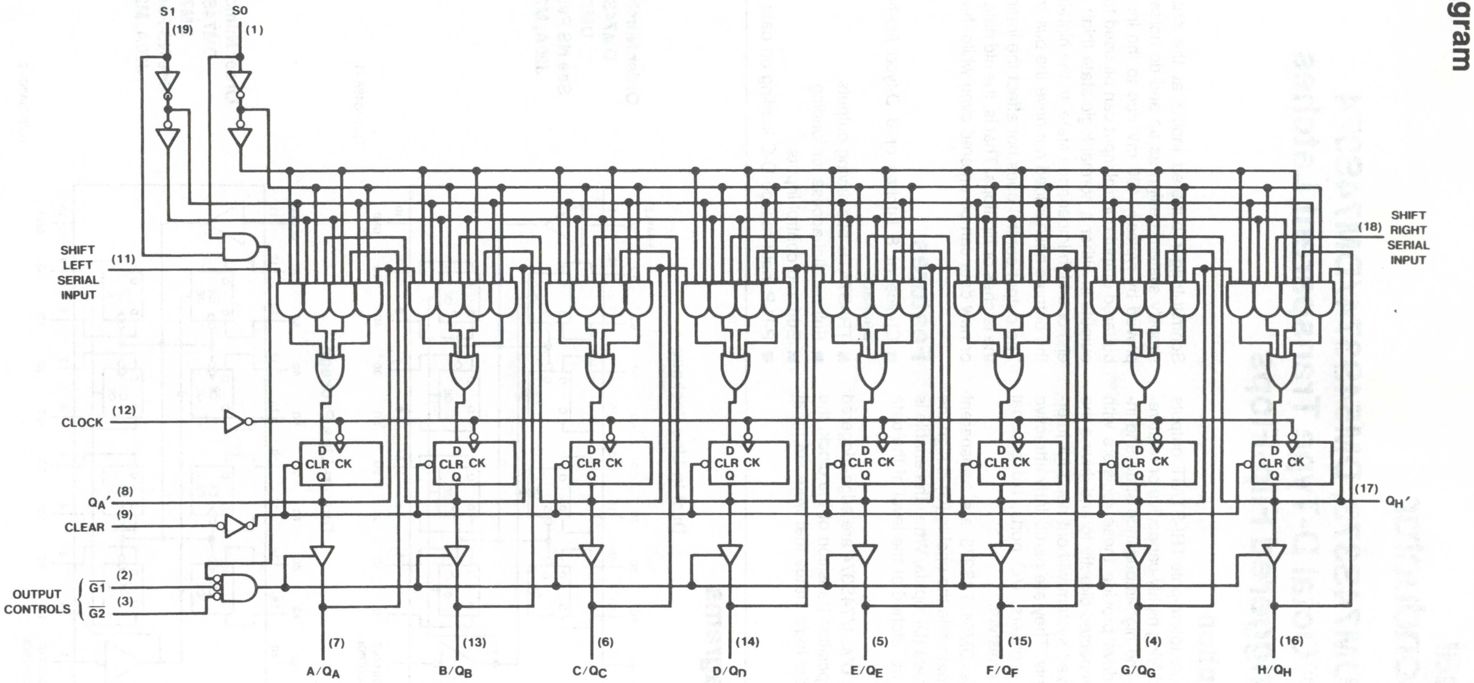
a...h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

Q_{A0}...Q_{H0} = The output logic level of Q_X before the indicated input conditions were established.

H = high level, L = low logic level, X = either low or high logic level

Q_{An}...Q_{Hn} = The output logic level before the active transition (↑) of the clock input.

Logic Diagram


S1
(19)
S0
(1)
SHIFT LEFT SERIAL INPUT
(11)
SHIFT RIGHT SERIAL INPUT
(18)
CLOCK
(12)
D
CLR
CK
Q
Q_A'
(8)
CLEAR
(9)
(17)
Q_H'
OUTPUT CONTROLS
(2)
$\overline{G1}$
(3)
$\overline{G2}$
(7)
A/Q_A
(13)
B/Q_B
(6)
C/Q_C
(14)
D/Q_D
(5)
E/Q_E
(15)
F/Q_F
(4)
G/Q_G
(16)
H/Q_H

TL/F/6485-2

National Semiconductor

DM54S373/DM74S373, DM54S374/DM74S374 TRI-STATE® Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the DM54/74S373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

The eight flip-flops of the DM54/74S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

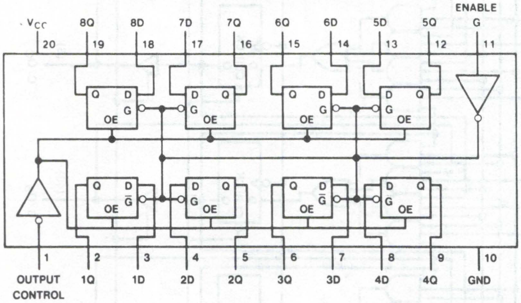
The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Choice of 8 latches or 8 D-type flip-flops in a single package
- TRI-STATE bus-driving outputs
- Full parallel-access for loading
- Buffered control inputs
- P-N-P input reduce D-C loading on data lines

Connection Diagrams

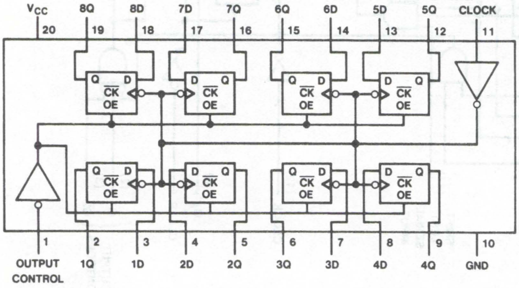
Dual-In-Line Package



TL/F/6486-1

Order Number DM54S373J, DM74S373WM or DM74S373N
See NS Package Number J20A, M20B or N20A

Dual-In-Line Package



TL/F/6486-2

Order Number DM54S374J, DM74S374WM or DM74S374N
See NS Package Number J20A, M20B or N20A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Function Tables

DM54/74S373 Truth Table

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

DM54/74S374 Truth Table

Output Control	Clock	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

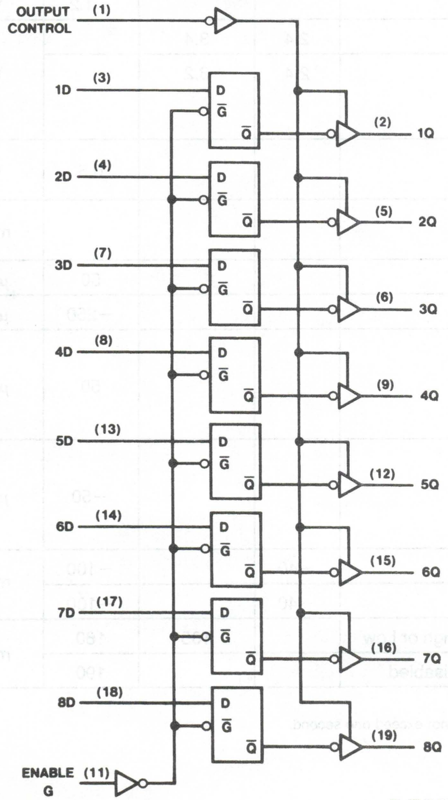
H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care

↑ = Transition from low-to-high level, Z = High Impedance State

Q_0 = The level of the output before steady-state input conditions were established.

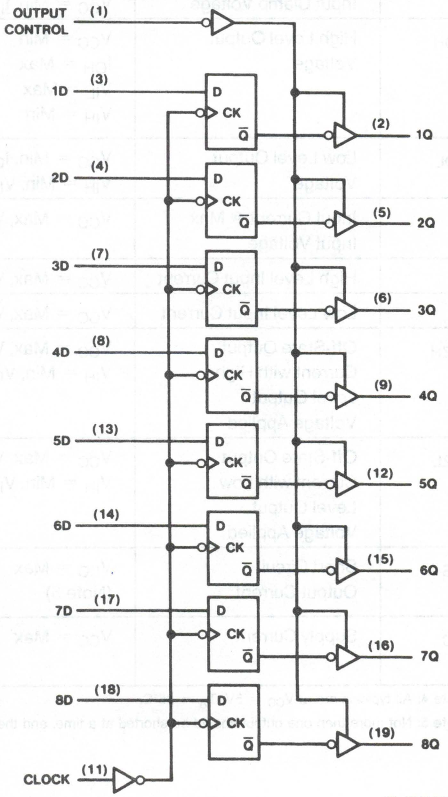
Logic Diagrams

DM54/74S373 Transparent Latches


OUTPUT CONTROL (1)
1D (3)
2D (4)
3D (7)
4D (8)
5D (13)
6D (14)
7D (17)
8D (18)
D
G
Q
(2) 1Q
(5) 2Q
(6) 3Q
(9) 4Q
(12) 5Q
(15) 6Q
(16) 7Q
(19) 8Q
ENABLE G (11)

TL/F/6486-3

DM54/74S374 Positive-Edge-Triggered Flip-Flops


OUTPUT CONTROL (1)
1D (3)
2D (4)
3D (7)
4D (8)
5D (13)
6D (14)
7D (17)
8D (18)
D
CK
Q
(2) 1Q
(5) 2Q
(6) 3Q
(9) 4Q
(12) 5Q
(15) 6Q
(16) 7Q
(19) 8Q
CLOCK (11)

TL/F/6486-4

'S373 Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM54S373			DM74S373			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−6.5	mA
I_{OL}	Low Level Output Current				20			20	mA
t_W	Pulse Width (Note 2)	Enable High	6			6			ns
		Enable Low	7.3			7.3			
t_{SU}	Data Setup Time (Notes 1 and 3)		0 ↓			0 ↓			ns
t_H	Data Hold Time (Notes 1 and 3)		10 ↓			10 ↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

'S373 Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min I_{OH} = Max V_{IL} = Max V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−250	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max	Outputs High or Low		105	160	mA
			Outputs Disabled			190	

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

'S373 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω C_L = 15 pF Min	 Max	 C_L = 50 pF Min	 Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Any Q		12		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Any Q		12		16	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Any Q		14		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Any Q		18		21	ns
t_{PZH}	Enable Time to High Level Output	Output Control to Any Q		15		17	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Any Q		18		23	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	Output Control to Any Q		9			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	Output Control to Any Q		12			ns

Note 1: C_L = 5 pF

'S374 Recommended Operating Conditions

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM54S374 Min	 Nom	 Max	DM74S374 Min	 Nom	 Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−6.5	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	100	75	0	100	75	MHz
f_{CLK}	Clock Frequency (Note 3)		0	100	75	0	100	75	MHz
t_W	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	7.3			7.3			
	Pulse Width (Note 3)	Clock High	15			15			
		Clock Low	15			15			
t_{SU}	Data Setup Time (Notes 1 and 4)		5 ↑			5 ↑			ns
t_H	Data Hold Time (Notes 1 and 4)		2 ↑			2 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

'S374 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min I_{OH} = Max V_{IL} = Max V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_H	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−250	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max	Outputs High			110	mA
			Outputs Low		90	140	
			Outputs Disabled			160	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

'S374 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency			75		75	MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		15		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		17		20	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Any Q		15		17	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Any Q		18		23	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)	Output Control to Any Q		9			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)	Output Control to Any Q		12			ns

Note 1: C_L = 5 pF

National Semiconductor

DM74S381 Arithmetic Logic Unit/Function Generator

General Description

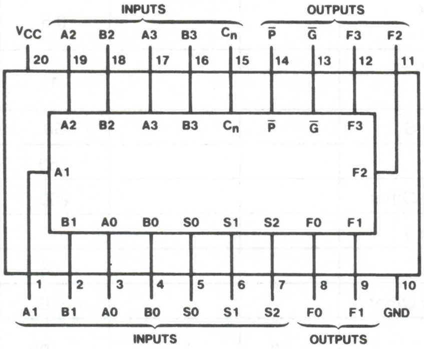
The 'S381 is a Schottky TTL arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. These operations are selected by the three function-select lines (S0, S1, S2). A full carry look-ahead circuit is provided for fast, simultaneous carry generation by means of two cascade outputs ($\overline{P}$ and $\overline{G}$) for the four bits in the package. The method of cascading 54S182/74S182 look-ahead carry generators with these ALU's to provide multi-level full carry look-ahead is illustated under typical applications data for the 'S182. The typical addition times shown illustrate the short delay time required for addition of longer words when full look-ahead is employed. The exclusive-OR, AND, or OR function of two Boolean variables is provided without the use of external circuitry. Also, the outputs can be either cleared (low) or preset (high) as desired.

Features

- A fully parallel 4-Bit ALU in 20-pin package for 0.300-inch row spacing
- Ideally suited for high-density economical processors
- Parallel inputs and outputs and full look-ahead provide system flexibility
- Arithmetic and logic operations selected specifically to simplify system implementation:
  - A minus B
  - B minus A
  - A plus B
  - and five other functions
- Schottky-clamped for high performance
  - 16-bit add time . . . 26 ns typ using look-ahead
  - 32-bit add time . . . 34 ns typ using look-ahead

Connection Diagram

Dual-In-Line Package



TL/F/6487–1

Order Number DM74S381N
See NS Package Number N20A

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	17, 19, 1, 3	Word A Inputs
B3, B2, B1, B0	16, 18, 2, 4	Word B Inputs
S2, S1, S0	7, 6, 5	Function-Select Inputs
C_n	15	Carry Input for Addition, Inverted Carry Input for Subtraction
F3, F2, F1, F0	12, 11, 9, 8	Function Outputs
$\overline{P}$	14	Inverted Carry Propagate Output
$\overline{G}$	13	Inverted Carry Generated Output
V_{CC}	20	Supply Voltage
GND	10	Ground

Function Table

Selection			Arithmetic/Logic Operation
S2	S1	S0	
L	L	L	CLEAR
L	L	H	B MINUS A
L	H	L	A MINUS B
L	H	H	A PLUS B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	PRESET

H = high level, L = low level

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−1	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Any S			50	μA
			Cn			250	
			Any Other			200	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V	Any S			−2	mA
			Cn			−8	
			Any Other			−6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			105	160	mA

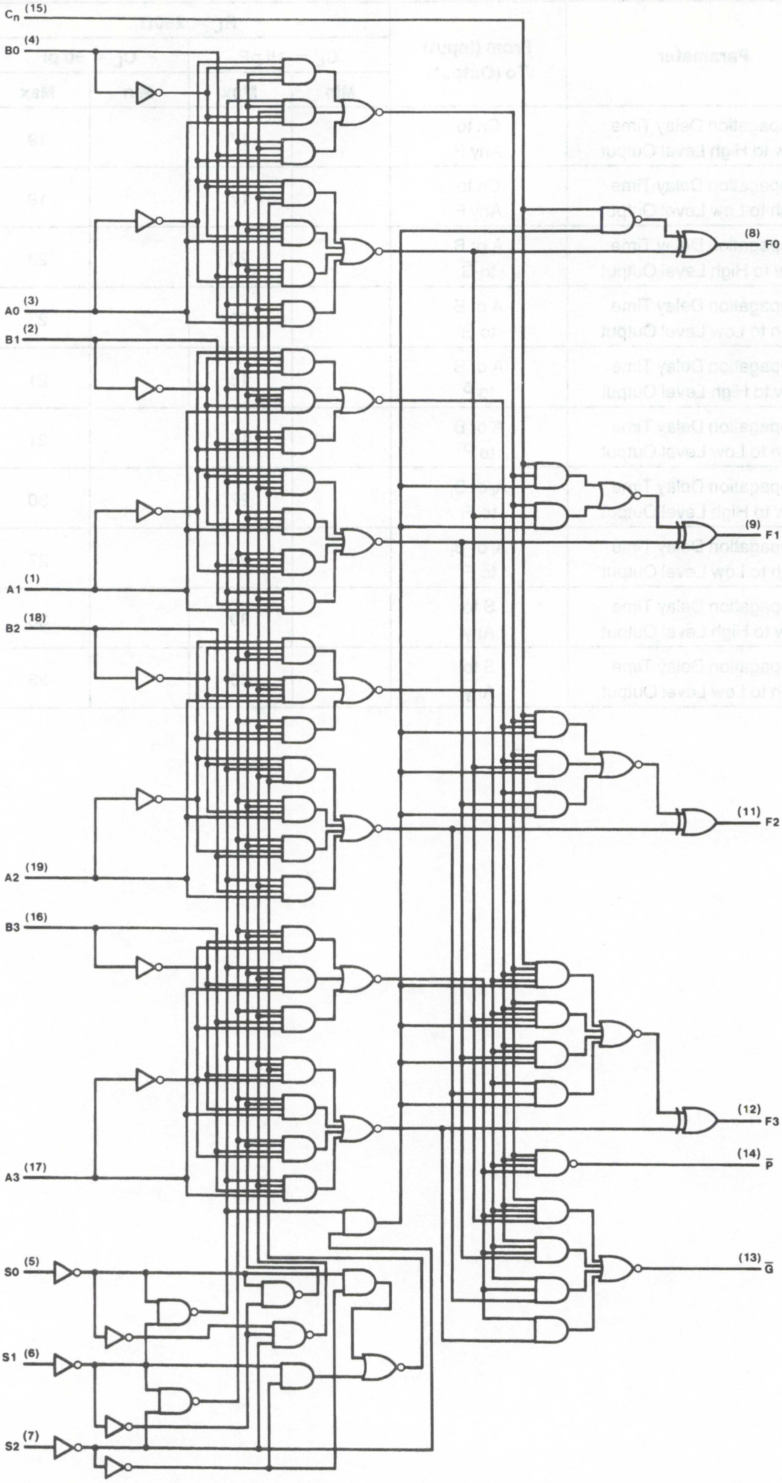
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			$C_L = 15$ pF		$C_L = 50$ pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Cn to Any F		17		19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Cn to Any F		17		19	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to $\overline{G}$		20		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to $\overline{G}$		20		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to $\overline{P}$		18		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to $\overline{P}$		18		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i or B_i to F_i		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i or B_i to F_i		25		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	S to Any		30		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	S to Any		30		33	ns

Logic Diagram


C$_n$ (15)
B0 (4)
A0 (3)
B1 (2)
A1 (1)
B2 (18)
A2 (19)
B3 (16)
A3 (17)
S0 (5)
S1 (6)
S2 (7)
(8) F0
(9) F1
(11) F2
(12) F3
(14) $\overline{P}$
(13) $\overline{G}$

TL/F/6487-2

National Semiconductor

DM93S00
4-Bit Universal Shift Register

General Description

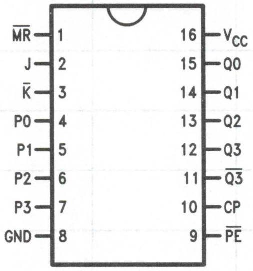
This device is 4-bit universal shift register. As a high speed multifunctional sequential logic block, it is useful in a wide variety of register and counter applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers.

Features

- Asynchronous master reset
- J, $\overline{K}$ inputs to first stage

Connection Diagram

Dual-In-Line Package

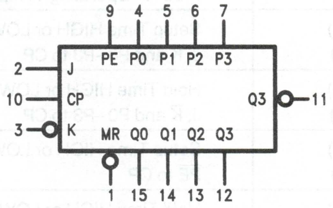


MR̅ 1
J 2
K̅ 3
P0 4
P1 5
P2 6
P3 7
GND 8
16 VCC
15 Q0
14 Q1
13 Q2
12 Q3
11 Q̅3
10 CP
9 P̅E̅

TL/F/10164–1

Order Number DM93S00N
See NS Package Number N16E

Logic Symbol



9
4
5
6
7
PE
P0
P1
P2
P3
2
J
10
CP
Q3
11
3
K
MR
Q0
Q1
Q2
Q3
1
15
14
13
12

TL/F/10164–2

V_{CC} = Pin 16
GND = Pin 8

Truth Table

Operating Mode	Inputs ($\overline{MR}$ = H)							Outputs @ tn+1				
	$\overline{PE}$	J	$\overline{K}$	P0	P1	P2	P3	Q0	Q1	Q2	Q3	$\overline{Q3}$
Shift Mode	H	L	L	X	X	X	X	L	Q0	Q1	Q2	$\overline{Q2}$
	H	L	H	X	X	X	X	Q0	Q0	Q1	Q2	$\overline{Q2}$
	H	H	L	X	X	X	X	$\overline{Q0}$	Q0	Q1	Q2	$\overline{Q2}$
	H	H	H	X	X	X	X	H	Q0	Q1	Q2	$\overline{Q2}$
Parallel Entry Mode	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

*tn+1 = State after next LOW-to-HIGH clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM93S00			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−1	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW, J, $\overline{K}$ and P0–P3 to CP	6.0 6.0			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW, J, $\overline{K}$ and P0–P3 to CP	0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW, $\overline{PE}$ to CP	8.0 8.0			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW, $\overline{PE}$ to CP	0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	7.0 7.0			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	12			ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2.0	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	20		80	mA
I_{CC}	Supply Current	V_{CC} = Max			120	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω C_L = 15 pF		Units
		Min	**Max**	
f_{max}	Maximum Shift Frequency	70		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Qn		8.5 12	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Qn		23	ns

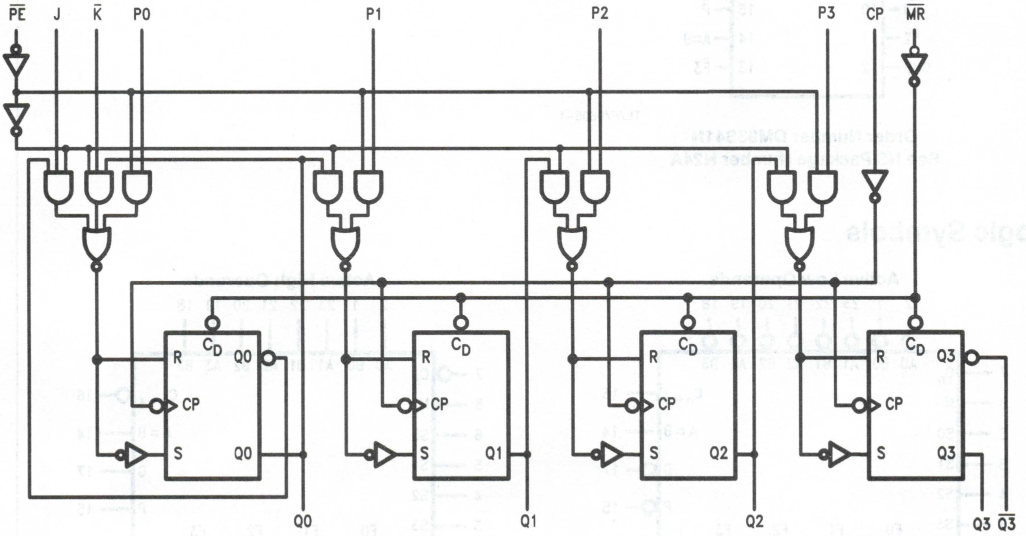
Functional Description

The Logic Diagrams and Truth Table indicate the functional characteristics of the DM93S00 4-bit shift register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers.

The DM93S00 has two primary modes of operation, shift right (Q0 → Q1) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ input is HIGH, serial data enters the first flip-flop Q0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction Q0 → Q1 → Q2 → Q3 following each LOW-to-HIGH clock transition. The J$\overline{K}$ inputs provide the flexibility of the JK type input for special applications, and the simple D-type input for general applications by tying the two pins together. When the $\overline{PE}$ input is LOW, the DM93S00 appears as four common clocked D flip-flops. The data on the parallel inputs P0–P3 is transferred to the respective Q0–Q3 outputs following the LOW-to-HIGH clock transition. Shift left operation (Q3 → Q2) can be achieved by tying the Qn outputs to the Pn−1 inputs and holding the $\overline{PE}$ input LOW.

All serial and parallel data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. Since the DM93S00 utilizes edge triggering, there is no restriction on the activity of the J, $\overline{K}$, Pn and $\overline{PE}$ inputs for logic operation—except for the setup and release time requirements. A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

Logic Diagram



TL/F/10164-3

National Semiconductor

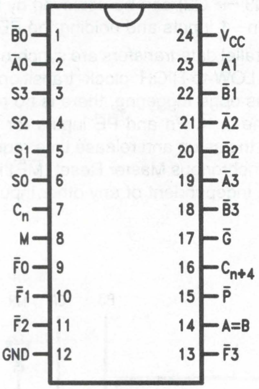
DM93S41
4-Bit Arithmetic Logic Unit

General Description

The DM93S41 4-bit arithmetic logic units can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations; the Add and Subtract modes are the most important. The DM93S41 is a pin replacement for the 54/74181.

Connection Diagram

Dual-In-Line Package


B̄0 1
Ā0 2
S3 3
S2 4
S1 5
S0 6
Cn 7
M 8
F̄0 9
F̄1 10
F̄2 11
GND 12
24 VCC
23 Ā1
22 B̄1
21 Ā2
20 B̄2
19 Ā3
18 B̄3
17 Ḡ
16 Cn+4
15 P̄
14 A=B
13 F̄3

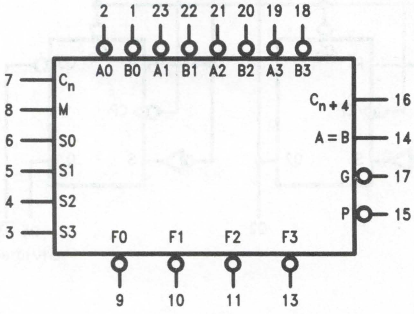
TL/F/9805-1

Order Number DM93S41N
See NS Package Number N24A

Pin Name	Description
Ā0–Ā3, B̄0–B̄3	Operand Inputs (Active LOW)
S0–S3	Function Select Inputs
M	Mode Control Input
Cu	Carry Input
F̄0–F̄3	Function Outputs (Active LOW)
A = B	Comparator Output
Ḡ	Carry Generate Output (Active LOW)
P̄	Carry Propagate Output (Active LOW)
C_{n+4}	Carry Output

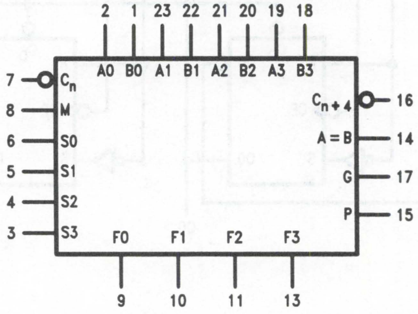
Logic Symbols

Active Low Operands


2
1
23
22
21
20
19
18
A0
B0
A1
B1
A2
B2
A3
B3
7 Cn
8 M
6 S0
5 S1
4 S2
3 S3
Cn+4 16
A=B 14
G 17
P 15
F0
F1
F2
F3
9
10
11
13

TL/F/9805-2

Active High Operands


2
1
23
22
21
20
19
18
A0
B0
A1
B1
A2
B2
A3
B3
7 Cn
8 M
6 S0
5 S1
4 S2
3 S3
Cn+4 16
A=B 14
G 17
P 15
F0
F1
F2
F3
9
10
11
13

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM93S41			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−1	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−40		−100	mA
I_{CCL}	Supply Current	V_{CC} = Max M, S0–S3 = 4.5V All Other Inputs = 0V			150	mA
I_{CCH}	Supply Current	V_{CC} = Max C_n, $\overline{B}0$–$\overline{B}3$ = GND All Other Inputs = 4.5V			140	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	Conditions	CL = 15 pF R_L = 280Ω		Units
			Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}	M = Gnd		12 12	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to $\overline{F}$	M = Gnd		12 12	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	M, S1, S2 = Gnd S0, S3 = 4.5V		14 14	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	M, S0, S3 = Gnd S1, S2 = 4.5V		15 15	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	M, S1, S2 = Gnd S0, S3 = 4.5V		14 14	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	M, S0, S3 = Gnd S1, S2 = 4.5V		15 15	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	M, S1, S3 = Gnd S0, S3 = 4.5V		20 20	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	M, S0, S3 = Gnd S1, S2 = 4.5V		21 21	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_{i+1}$	M, S1, S2 = Gnd S0, S3 = 4.5V		24 24	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_{i+1}$	M, S0, S3 = Gnd S1, S2 = 4.5V		25 25	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}$	M = 4.5V		20 20	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+1}	M, S1, S2 = Gnd S0, S3 = 4.5V		18.5 18.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+1}	M, S0, S3 = Gnd S1, S2 = 4.5V		23 23	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to A = B	M, S0, S3 = Gnd S1, S2 = 4.5V R_L = 400Ω to 5.0V		23 23	ns

Functional Description

The DM93S41 is a 4-bit high speed parallel arithmetic logic unit (ALU). Controlled by the four Function Select inputs (S0–S3) and the Mode Control input (M), it can perform all the 16 possible operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table below lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the DM93S41 can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For super high speed operation the Schottky DM93S41 should be used in conjunction with the '42 carry lookahead circuit.

The A = B output from the DM93S41 goes HIGH when all four $\overline{F}_n$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with the other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated the '41 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

Function Table

Mode Select Inputs				Active Low Inputs & Outputs		Active High Inputs & Outputs	
				Logic	Arithmetic**	Logic	Arithmetic**
S3	S2	S1	S0	(M = H)	(M = L) (C_n = L)	(M = H)	(M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A} + \overline{B}$	A + B
L	L	H	L	$\overline{A} + \overline{B}$	$A\overline{B}$ minus 1	$\overline{A}B$	$A + \overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A} + \overline{B}$	A plus $(A + \overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A + \overline{B})$	$\overline{B}$	(A + B) plus $A\overline{B}$
L	H	H	L	$\overline{A} \oplus \overline{B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A + \overline{B}$	$A + \overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{A}B$	A plus (A + B)	$\overline{A} + B$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$A \oplus B$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)	B	$(A + \overline{B})$ plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	$A\overline{B}$	AB plus A	$A + \overline{B}$	(A + B) plus A
H	H	H	L	AB	$A\overline{B}$ minus A	A + B	$(A + \overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

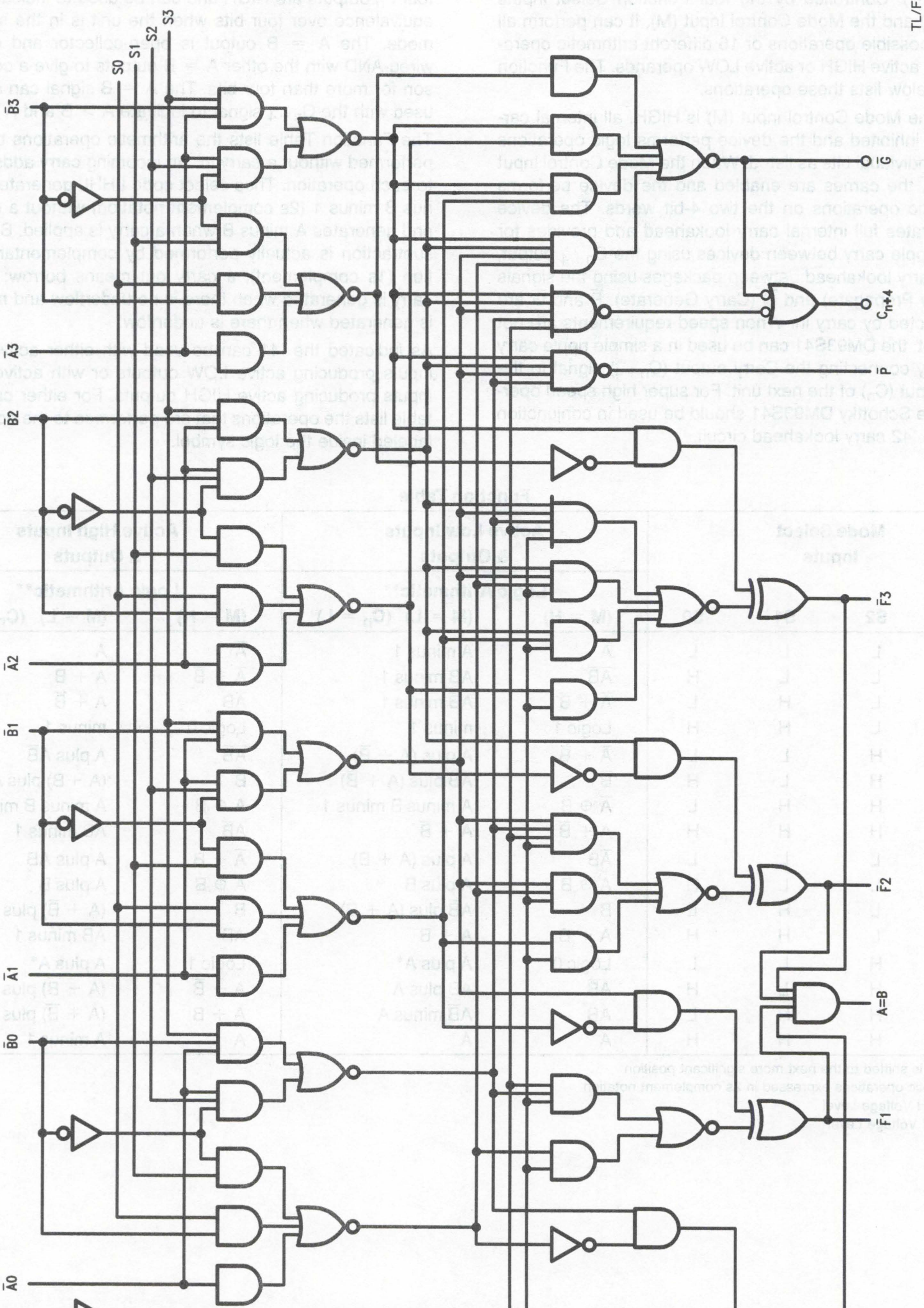
*Each bit is shifted to the next more significant position

**Arithmetic operations expressed in 2s complement notation

H = HIGH Voltage Level

L = LOW Voltage Level

Logic Diagram


S0
S1
S2
S3
B̄3
Ā3
B̄2
Ā2
B̄1
Ā1
B̄0
Ā0
M
Cn
G
Cn+4
P
F3
F2
A=B
F1
F0

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SUM MODE TEST TABLE I. Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Input		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ to $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ to $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II. Function Inputs: S1 = S2 = 4.5V,S0 = S3 = M = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$

DIFF MODE TEST TABLE II. Function Inputs: S1 = S2 = 4.5V,S0 = S3 = M = 0V (Continued)

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	$C_n + 4$

LOGIC MODE TEST TABLE III. Function Inputs: S1 = S2 = M = 4.5V, S0 = S3 = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$

National Semiconductor

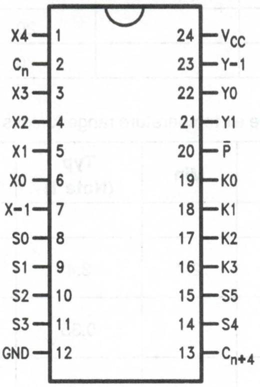
DM93S43
4-Bit by 2-Bit Twos Complement Multiplier

General Description

The DM93S43 is a high-speed twos complement multiplier. The device is a 4-bit by 2-bit building block that can be connected in an iterative array to perform multiplication of two binary numbers of variable lengths. The device can generate the twos complement product, without correction, of two binary numbers presented in twos complement notation.

Connection Diagram

Dual-In-Line Package

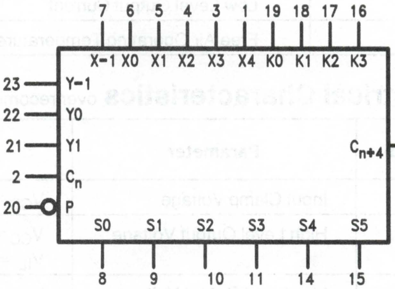


X4 1
Cn 2
X3 3
X2 4
X1 5
X0 6
X-1 7
S0 8
S1 9
S2 10
S3 11
GND 12
24 VCC
23 Y-1
22 Y0
21 Y1
20 P̅
19 K0
18 K1
17 K2
16 K3
15 S5
14 S4
13 Cn+4

TL/F/9806-1

Order Number DM93S43N
See NS Package Number N24A

Logic Symbol



7 6 5 4 3 1 19 18 17 16
X-1 X0 X1 X2 X3 X4 K0 K1 K2 K3
23 Y-1
22 Y0
21 Y1
2 Cn
20 P
Cn+4 13
S0 S1 S2 S3 S4 S5
8 9 10 11 14 15

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V_{CC} = Pin 24
GND = Pin 12

Pin Name	Description
X-1, X3, X4, X0, X1, X2	Multiplicand Inputs
Y0, Y-1, Y1	Multiplier Inputs
C_n	Carry Input
K0–K3	Constant Inputs
$\overline{P}$	Polarity Control Input (Active Low for High Operands)
S0–S5	Product Outputs
C_{n+4}	Carry Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range DM93S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM93S43			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−1	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			149	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}		9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to $S_0 - S_3$		13 11	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to S_4, S_5		16 15	ns

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations) (Continued)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay kn to C_{n+4}		12 13	ns
t_{PLH} t_{PHL}	Propagation Delay kn to S0 − S3		14 12	ns
t_{PLH} t_{PHL}	Propagation Delay kn to S4, S5		19 17	ns
t_{PLH} t_{PHL}	Propagation Delay xn to C_{n+4}		15 24	ns
t_{PLH} t_{PHL}	Propagation Delay xn to S0 − S3		25 25	ns
t_{PLH} t_{PHL}	Propagation Delay xn to S4, S5		30 21	ns
t_{PLH} t_{PHL}	Propagation Delay yn to C_{n+4}		25 27	ns
t_{PLH} t_{PHL}	Propagation Delay yn to S0 − S3		28 27	ns
t_{PLH} t_{PHL}	Propagation Delay yn to S4, S5		32 30	ns

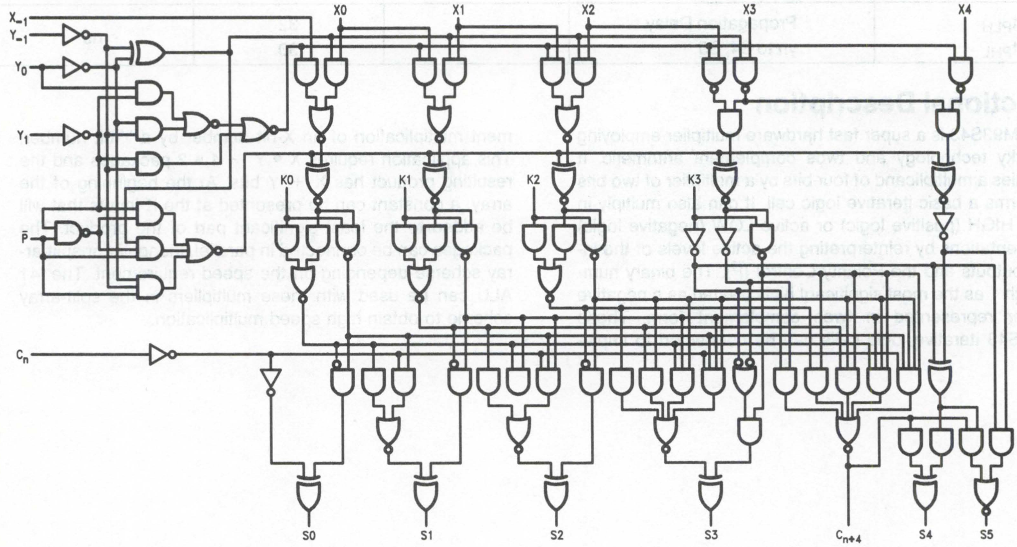
Functional Description

The DM93S43 is a super fast hardware multiplier employing Schottky technology and twos complement arithmetic. It multiplies a multiplicand of four bits by a multiplier of two bits and forms a basic iterative logic cell. It can also multiply in active HIGH (positive logic) or active LOW (negative logic) representations by reinterpreting the active levels of the inputs, outputs and the Polarity Control ($\overline{P}$). The binary number with 1 as the most significant bit is treated as a negative number represented in twos complement form. These DM93S43 iterative logic cells can be connected to implement multiplication of an X-bit number by a Y-bit number. This application requires X • Y ÷ 4 • 2 packages and the resulting product has X + Y bits. At the beginning of the array, a constant can be presented at the K inputs that will be added to the least significant part of the product. The packages can be connected in parallel, triangular or split-array scheme depending on the speed requirement. The '41 ALU can be used with these multipliers in the split-array scheme to obtain high speed multiplication.

TABLE I. Switching Test Conditions

Input	Outputs	Inputs at 0V (Remaining Inputs at 4.5 V)
C_n	C_{n+4}, S0 − S3, S4, S5	$\overline{P}$, y−1, y1 All x
k0	C_{n+4}, S0 − S3, S4, S5	$\overline{P}$, y−1, y1 All x
k1	C_{n+4}, S1 − S3, S4, S5	$\overline{P}$, y−1, y1 All x
k2	C_{n+4}, S2, S3, S4, S5	$\overline{P}$, y−1, y1 All x
k3	S3	$\overline{P}$, y−1, y1 All x
k3	S4, S5	$\overline{P}$, y−1, y1 All x, C_n
x−1	C_{n+4}, S0 − S3, S4, S5	$\overline{P}$, y−1, All k
x0	C_{n+4}, S0 − S3, S4, S5	$\overline{P}$, y−1, y1, All k
x1	C_{n+4}, S1 − S3, S4, S5	$\overline{P}$, y−1, y1, All k
x2	C_{n+4}, S2, S3, S4, S5	$\overline{P}$, y−1, y1, All k
x3, x4	S3	$\overline{P}$, y−1, y1, All k
x3, x4	S4, S5	$\overline{P}$, y−1, y1, All k, C_n
x3, x4	S4, S5	$\overline{P}$, y−1, All k, C_n
y−1	C_{n+4}, S0 − S3, S4, S5	$\overline{P}$, x1, x2, x3, x4, All k
y0	C_{n+4}, S0 − S3, S4, S5	$\overline{P}$, x1, x2, x3, x4, All k
y1	C_{n+4}, S0 − S3, S4, S5	x0, x1, x2, x3, x4, All k

Logic Diagram



TL/F/9806-3

National Semiconductor

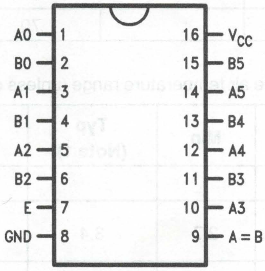
DM93S46
High-Speed 6-Bit Identity Comparator

General Description

The DM93S46 is a very high speed 6-bit identity comparator. The device compares two words of up to six bits and indicates identity in less than 12 ns. It is easily expandable to any word length by using either serial or parallel expansion techniques. When the Enable input (E) is LOW, it forces the output LOW.

Connection Diagram

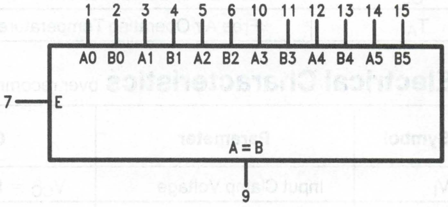
Dual-In-Line Package


A0 1
B0 2
A1 3
B1 4
A2 5
B2 6
E 7
GND 8
16 VCC
15 B5
14 A5
13 B4
12 A4
11 B3
10 A3
9 A=B

TL/F/9807–1

Order Number DM93S46N
See NS Package Number N16E

Logic Symbol


1 2 3 4 5 6 10 11 12 13 14 15
A0 B0 A1 B1 A2 B2 A3 B3 A4 B4 A5 B5
7 E
A=B
9

TL/F/9807–2

V_{CC} = Pin 16
GND = Pin 18

Pin Name	Description
A0–A5	Word A Inputs
B0–B5	Word B Inputs
E	Enable Input (Active High)
A=B	A Equal to B Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range DM93S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM93S46 Min	DM93S46 Nom	DM93S46 Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−1	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−20	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			70	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	Conditions	CL = 15 pF Min	CL = 15 pF Max	Units
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to A = B	E = 4.5V, Other Inputs = 4.5V, Test Each Input Individually	3.0 3.0	17 17	ns
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to A = B	E = 4.5V, Other Inputs = Gnd, Test Each Input Individually	3.0 3.0	14 15	ns
t_{PLH} t_{PHL}	Propagation Delay E to A = B	$A_n = B_n$	2.0 2.0	10 10	ns

Functional Description

The DM93S46 is a very high speed 6-bit identity comparator. The A = B output is HIGH when the Enable (E) is HIGH and the two 6-bit words are equal. Equality is determined by Exclusive-NOR circuits which individually compare the equivalent bits from each word. When any two of the equivalent bits from each word have different logic levels, the A = B output is LOW.

$$(A = B) = (\overline{A0 \oplus B0}) \bullet (\overline{A1 \oplus B1}) \bullet (\overline{A2 \oplus B2}) \bullet (\overline{A3 \oplus B3}) \bullet (\overline{A4 \oplus B4}) \bullet (\overline{A5 \oplus B5}) \bullet E$$

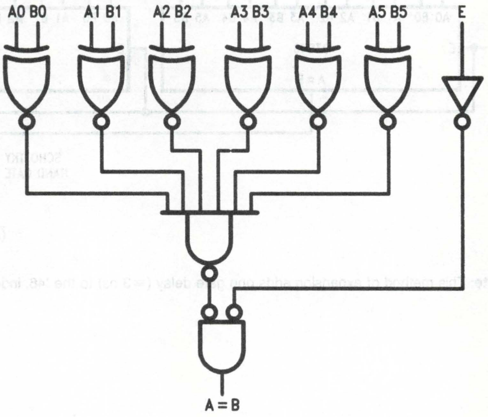
An active HIGH Enable (E) provides a means of fast ripple expansion. By connecting the A = B output of the first stage of the comparator to the enable of the next stage, the comparator can be expanded in 6-bit increments at an additional 4.5 ns per stage. An even faster expansion technique is achieved by connecting the A = B outputs to a Schottky NAND gate. This method compares two words of up to 78 bits each in 15 ns (typical) using the '133 13-input Schottky NAND gate.

Truth Table

Inputs		Output
E	**A_n, B_n**	**A = B**
L	$A_n = B_n$	L
L	$A_n \neq B_n$	L
H	$A_n \neq B_n$	L
H	$A_n = B_n$	H

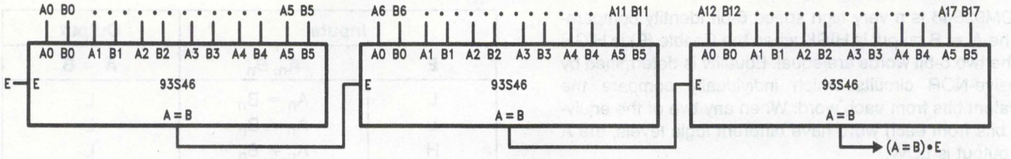
H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram



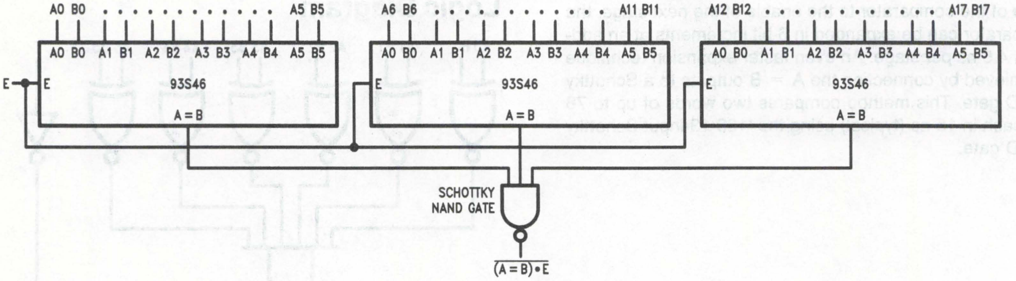
TL/F/9807-5

Ripple Expansion


A0 B0 . . . . A5 B5
A6 B6 . . . . A11 B11
A12 B12 . . . . A17 B17
A0 B0 A1 B1 A2 B2 A3 B3 A4 B4 A5 B5
E
93S46
A = B
(A = B)•E

TL/F/9807-3

Note: This simple method of expansion adds 4.5 ns for each additional '46 used.


A0 B0 . . . . A5 B5
A6 B6 . . . . A11 B11
A12 B12 . . . . A17 B17
A0 B0 A1 B1 A2 B2 A3 B3 A4 B4 A5 B5
E
93S46
A = B
SCHOTTKY NAND GATE
$\overline{(A = B) \cdot E}$

TL/F/9807-4

Note: This method of expansion adds one gate delay (≅3 ns) to the '46, independent of the word length that is compared.

National Semiconductor

DM93S47
High Speed 6-Bit Identity Comparator

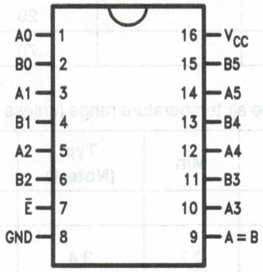
General Description

The DM93S47 is a very high speed 6-bit identity comparator. The device features an open-collector output for wired-OR expansion and active LOW enable. The DM93S47 is fabricated with the Schottky barrier diode process for high speed, and is completely compatible with all TTL families.

This device is recommended for applications where wired-OR expansion is desired and the speed of an active pull-up is not required. The DM93S47 is a pin-for-pin replacement for the DM7160/8160.

Connection Diagram

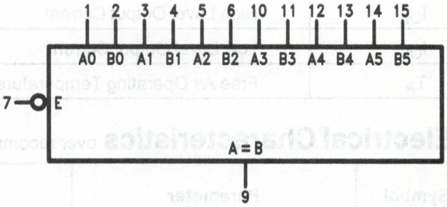
Dual-In-Line Package


A0 1
B0 2
A1 3
B1 4
A2 5
B2 6
$\overline{E}$ 7
GND 8
16 V_{CC}
15 B5
14 A5
13 B4
12 A4
11 B3
10 A3
9 A = B

TL/F/9808-1

Order Number DM93S47N
See NS Package Number N16E

Logic Symbol


1 2 3 4 5 6 10 11 12 13 14 15
A0 B0 A1 B1 A2 B2 A3 B3 A4 B4 A5 B5
7
E
A = B
9

V_{CC} = Pin 16
GND = Pin 8

TL/F/9808-2

Truth Table

Inputs		Output
$\overline{E}$	A_n, B_n	A = B
L	$A_n = B_n$	H
L	$A_n \neq B_n$	L
H	$A_n \neq B_n$	H
H	$A_n = B_n$	H

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range (DM93S)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM93S47			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Current	2			V
V_{IL}	Low Level Input Current			0.8	V
I_{OH}	High Level Output Current			−1	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2.0	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			65	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for Waveforms and Load Configurations)

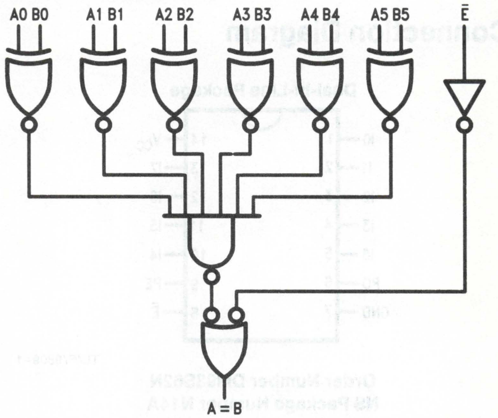
Symbol	Parameter	Conditions	$C_L = 15$ pF, $R_L = 280\Omega$ Min	$C_L = 15$ pF, $R_L = 280\Omega$ Max	Units
t_{PLH}	Propagation Delay	$\overline{E}$ = GND, Other Inputs = 4.5V,	5.0	17	ns
t_{PHL}	A_n or B_n to A = B	Test Each Input Individually	5.0	17	
t_{PLH}	Propagation Delay	$\overline{E}$ = GND, Other Inputs = GND,	4.0	14	ns
t_{PHL}	A_n or B_n to A = B	Test Each Input Individually	4.0	15	
t_{PLH}	Propagation Delay	$A_n \neq B_n$	3.0	10	ns
t_{PHL}	$\overline{E}$ to A = B		3.0	10	

Functional Description

The DM93S47 is a very high speed 6-bit identity comparator. When enabled ($\overline{E}$ input LOW), the A = B output is HIGH if the two 6-bit words are equal. When disabled ($\overline{E}$ input HIGH), the A = B output is forced HIGH. Equality is determined by Exclusive-NOR circuits which individually compare the equivalent bits from each word. Since the A = B output state is determined by the equality of each pair of inputs, the equivalent A_n and B_n pins can be interchanged to facilitate board layout or wiring. The active LOW Enable ($\overline{E}$) can be used as a high speed strobe. When the Enable is HIGH, the A = B output is forced HIGH. This allows devices tied to a common wired-OR (actually wired-AND) node to be strobed individually or in groups. Only the enabled devices will determine the state of the output node.

$$(A = B) = \overline{E} + \overline{(A0 \oplus B0)} \bullet \overline{(A1 \oplus B1)} \bullet \overline{(A2 \oplus B2)} \bullet \overline{(A3 \oplus B3)} \bullet \overline{(A4 \oplus B4)} \bullet \overline{(A5 \oplus B5)}$$

Logic Diagram



TL/F/9808–3

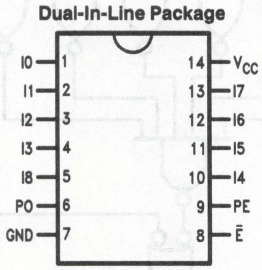
National Semiconductor

DM93S62
9-Input Parity Checker/Generator

General Description

The DM93S62 is a very high speed 9-input parity checker/generator for use in error detection and error correction applications. The DM93S62 provides odd and even parity for up to nine data bits. The even parity output (PE) is HIGH if an even number of inputs are HIGH and $\overline{E}$ is LOW. The odd parity output (PO) will be HIGH if an odd number of inputs are HIGH and $\overline{E}$ is LOW. A HIGH level on the Enable ($\overline{E}$) input forces both outputs LOW.

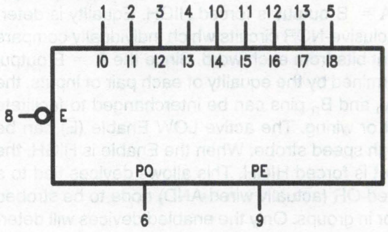
Connection Diagram


Dual-In-Line Package
I0 1
I1 2
I2 3
I3 4
I8 5
PO 6
GND 7
14 VCC
13 I7
12 I6
11 I5
10 I4
9 PE
8 Ē

TL/F/9809-1

Order Number DM93S62N
NS Package Number N14A

Logic Symbol


1 2 3 4 10 11 12 13 5
I0 I1 I2 I3 I4 I5 I6 I7 I8
8 E
PO PE
6 9

TL/F/9809-2

V_{CC} = Pin 14
GND = Pin 7

Pin Name	Description
I0–I8	Data Inputs
$\overline{E}$	Output Enable (Active Low)
PO	Odd Parity Output
PE	Even Parity Output

Truth Table ($\overline{E}$ = LOW)

Number of Inputs I0–I8 that are HIGH	Outputs	
	PO	PE
1, 3, 5, 7, 9	H	L
0, 2, 4, 6, 8	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM93S62			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−1	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V, I0–I8			−1.6	mA
		V_{CC} = Max, V_I = 0.5V, $\overline{E}$ Only			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			65	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH}	Propagation Delay I0–I7 to PE		26	ns
t_{PHL}			22	
t_{PLH}	Propagation Delay I8 to PE		12	ns
t_{PHL}			9.0	
t_{PLH}	Propagation Delay I0–I7 to PO		26	ns
t_{PHL}			26	
t_{PLH}	Propagation Delay I8 to PO		13	ns
t_{PHL}			13	
t_{PLH}	Propagation Delay $\overline{E}$ to PE		7.0	ns
t_{PHL}			7.0	
t_{PLH}	Propagation Delay $\overline{E}$ to PO		7.0	ns
t_{PHL}			7.0	

Functional Description

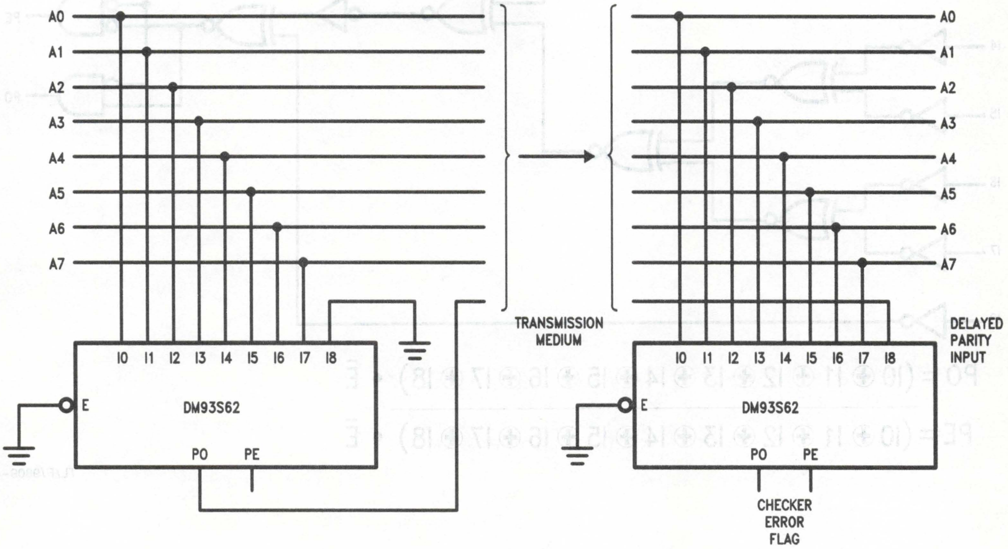
The DM93S62 is a very high speed 9-input parity checker or generator. It is intended primarily for error detection in systems which transmit data in 8-bit bytes, but it can be expanded to any number of data inputs. Both even and odd parity outputs are available to allow maximum flexibility for both parity generation and parity checking. When the device is enabled ($\overline{E}$ = LOW), the Even Parity output (PE) is HIGH when an even number of inputs is HIGH, and the Odd Parity output (PO) is HIGH when an odd number of inputs is HIGH. The active LOW Enable ($\overline{E}$) controls the state of both outputs; when the Enable ($\overline{E}$) is HIGH, both outputs will be LOW. The Enable may be used to strobe the outputs at very high speeds to synchronize or inhibit the parity data.

The DM93S62 has been designed with two sections using Exclusive-NOR comparison techniques. Eight data inputs I0–I7 represent one section which will generate a parity bit in 16 ns to 20 ns. The ninth input (I8) bypasses three levels of logic and switches the outputs in 6.0 ns to 9.0 ns. This feature may be used to compensate for delayed arrival of the parity bit, allowing faster system cycle times *(Figure a)*. The fast I8 input is also useful when more than nine bits are to be checked. The output of one DM93S62 drives the I8 input of a second DM93S62, providing a 17-bit parity check in 29 ns (typ).

When some inputs of the DM93S62 are not used, such as for words of less than nine bits or when using parallel expansion techniques, there is an optimum delay scheme for termination of the unused inputs (see Table II). In essence, if one of the inputs of any Exclusive-NOR stays HIGH, the delay from the other input to the output is minimized.

TABLE II. Termination Recommendations for Less than Nine Bits

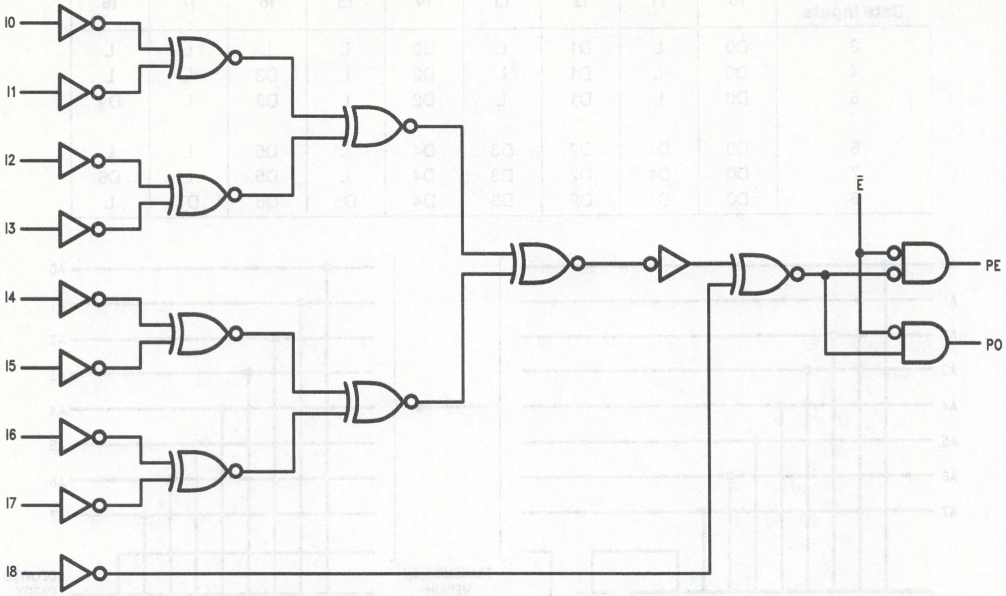
Number of Data Inputs	I0	I1	I2	I3	I4	I5	I6	I7	I8
3	D0	L	D1	L	D2	L	L	L	L
4	D0	L	D1	L	D2	L	D3	L	L
5	D0	L	D1	L	D2	L	D3	L	D4
6	D0	D1	D2	D3	D4	L	D5	L	L
7	D0	D1	D2	D3	D4	L	D5	L	D6
8	D0	D1	D2	D3	D4	D5	D6	D7	L


A0
A1
A2
A3
A4
A5
A6
A7
I0 I1 I2 I3 I4 I5 I6 I7 I8
E
DM93S62
PO
PE
TRANSMISSION
MEDIUM
A0
A1
A2
A3
A4
A5
A6
A7
DELAYED
PARITY
INPUT
I0 I1 I2 I3 I4 I5 I6 I7 I8
E
DM93S62
PO
PE
CHECKER
ERROR
FLAG

TL/F/9809-3

FIGURE a. Fast Input I8 allows Higher System Speed

Logic Diagram


I0
I1
I2
I3
I4
I5
I6
I7
I8
Ē
PE
PO

$$PO = (I0 \oplus I1 \oplus I2 \oplus I3 \oplus I4 \oplus I5 \oplus I6 \oplus I7 \oplus I8) \bullet \bar{E}$$

$$PE = \overline{(I0 \oplus I1 \oplus I2 \oplus I3 \oplus I4 \oplus I5 \oplus I6 \oplus I7 \oplus I8)} \bullet \bar{E}$$

TL/F/9809-4

National Semiconductor

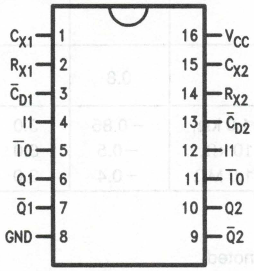
DM96S02 Dual Retriggerable Resettable Monostable Multivibrator

General Description

The DM96S02 is a dual retriggerable and resettable monostable multivibrator. This one-shot provides exceptionally wide delay range, pulse width stability, predictable accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. Resistor values up to 2.0 MΩ for the DM96S02 reduce required capacitor values. Hysteresis is provided on the positive trigger input of the DM96S02 for increased noise immunity.

Connection Diagram

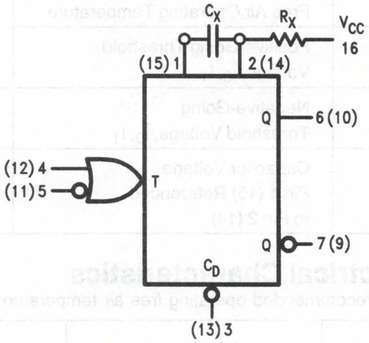
Dual-In-Line Package


C_{X1} 1
R_{X1} 2
$\overline{C}_{D1}$ 3
I1 4
$\overline{I0}$ 5
Q1 6
$\overline{Q}1$ 7
GND 8
16 V_{CC}
15 C_{X2}
14 R_{X2}
13 $\overline{C}_{D2}$
12 I1
11 $\overline{I0}$
10 Q2
9 $\overline{Q}2$

TL/F/9810-1

Order Number DM96S02N
See NS Package Number N16E

Logic Symbol


C_X
R_X
V_{CC}
16
(15) 1
2 (14)
Q
6 (10)
(12) 4
(11) 5
T
$\overline{Q}$
7 (9)
C_D
(13) 3

TL/F/9810-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{I0}$	Trigger Input (Active Falling Edge)
I1	Schmitt Trigger Input (Active Rising-Edge)
$\overline{C}_D$	Direct Clear Input (Active LOW)
Q1-2	True Pulse Output
$\overline{Q}$1-2	Complementary Pulse Output
$C_{X\,1,\,2}$	External Capacitor Connection
$R_{X\,1,\,2}$	External Resistor Connection

Triggering Truth Table

Pin Number			Operation
5(11)	4(12)	3(13)	
H → L	L	H	Trigger
H	L → H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level ≥ V_{IH}
L = LOW Voltage Level ≤ V_{IL}
X = Immaterial (either H or L)
H → L = HIGH to LOW Voltage Level transition
L → H = LOW to HIGH Voltage Level transition

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Conditions		Min	Nom	Max	Units
V_{CC}	Supply Voltage			4.75	5	5.25	V
V_{IH}	High Level Input Voltage			2	V		
V_{IL}	Low Level Input Voltage					0.8	V
I_{OH}	High Level Output Current					−1	mA
I_{OL}	Low Level Output Current					20	mA
T_A	Free Air Operating Temperature			0		70	°C
V_{T+}	Positive-Going Threshold Voltage, $\bar{I}_0$, I_1	$V_{CC} = 5.0V$				2.0	V
V_{T-}	Negative-Going Threshold Voltage, $\bar{I}_0$, I_1	$V_{CC} = 5.0V$		0.8			V
V_{CX}	Capacitor Voltage Pin 1 (15) Referenced to Pin 2 (14)	$V_{CC} = 4.75V$ to 5.25V	$R_X = 1.0\ k\Omega$, $R_X \geq 10\ k\Omega$, $R_X > 1.0\ M\Omega$	−0.85 −0.5 −0.4	3.0 3.0 3.0		V

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = $ Min, $I_I = -18$ mA			−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = $ Min, $I_{OH} = -1.0$ mA, V_{IL} Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	$V_{CC} = $ Min, $I_{OL} = $ Max, $V_{IH} = $ Min		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = $ Max, $V_I = 5.5V$			1	mA
I_{IH}	High Level Input Current	$V_{CC} = $ Max, $V_I = 2.7V$			20	μA
I_{IL}	Low Level Input Current	$V_{CC} = $ Max, $V_I = 0.4V$			−1.0	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = $ Max (Note 2)	−40		−100	mA
I_{CC}	Supply Current	$V_{CC} = $ Max			75	mA

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

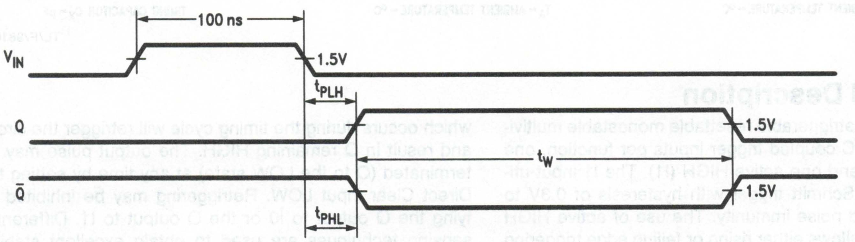
Symbol	Parameter	Conditions	C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay $\overline{I}0$ to Q	*Figure a*		15	ns
t_{PHL}	Propagation Delay $\overline{I}0$ to $\overline{Q}$			19	ns
t_{PLH}	Propagation Delay I1 to Q			19	ns
t_{PHL}	Propagation Delay I1 to $\overline{Q}$			20	ns
t_{PHL}	Propagation Delay $\overline{C}_D$ to Q			20	ns
t_{PLH}	Propagation Delay $\overline{C}_D$ to $\overline{Q}$			14	ns
$t_w(L)$	$\overline{I}0$ Pulse Width LOW		8.0		ns
$t_w(H)$	I1 Pulse Width HIGH		12		ns
$t_w(L)$	$\overline{C}_D$ Pulse Width LOW		7.0		ns
$t_w(H)$	Minimum Q Pulse Width HIGH	R_X = 1.0 kΩ, C_X = 10 pF Including Jig and Stray	30	45	ns
t_w	Q Pulse Width	R_X = 10 kΩ, C_X = 1000 pF	5.2	5.8	µs
R_X	Timing Resistor Range*	T_A = −55°C to +125°C V_{CC} = 4.5V to 5.5V	1.0	2000	kΩ
$t\Delta_t$	Change in Q Pulse Width over Temperature	R_X = 10 kΩ, C_X = 1000 pF		1.0	%
$t\Delta_V$	Change in Q Pulse Width over V_{CC} Range	T_A = 25°C, V_{CC} = 4.75V to 5.25V, R_X = 10 kΩ, C_X = 1000 pF T_A = 25°C, V_{CC} = 4.5V to 5.5V, R_X = 10 kΩ, C_X = 1000 pF		1.0	%

*Applies only over commercial V_{CC} and T_A range for DM96S02.

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Waveforms



INPUT PULSE
f ≅ 100 kHz
Amp ≅ 3.0V
Width ≅ 100 ns
t_r = t_f ≤ 5 ns

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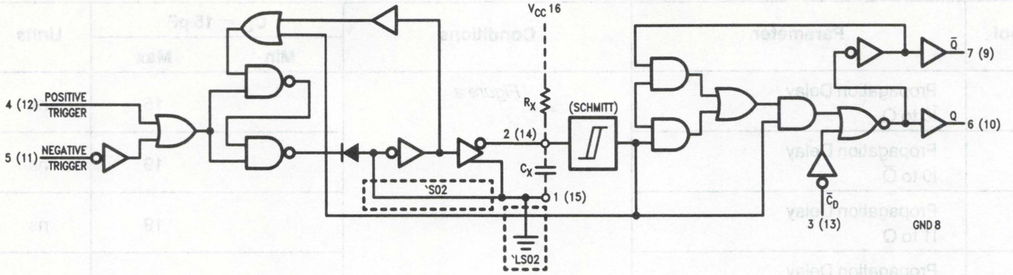
Figure a.

Logic Diagram



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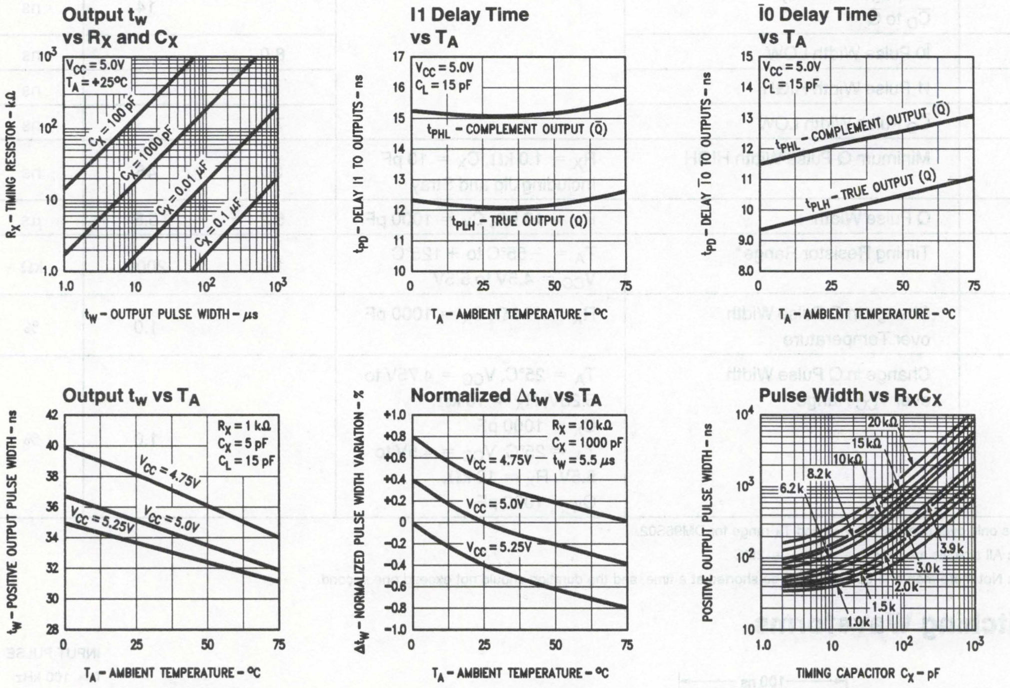
Typical Performance Characteristics



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Functional Description

The 96S02 dual retriggerable resettable monostable multivibrator has two DC coupled trigger inputs per function, one active LOW (Ī0) and one active HIGH (I1). The I1 input utilizes an internal Schmitt trigger with hysteresis of 0.3V to provide increased noise immunity. The use of active HIGH and LOW inputs allows either rising or falling edge triggering and optional non-retriggerable operation. The inputs are DC coupled making triggering independent of input transition times. When input conditions for triggering are met the Q output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger which occurs during the timing cycle will retrigger the circuit and result in Q remaining HIGH. The output pulse may be terminated (Q to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the Q̄ output to Ī0 or the Q output to I1. Differential sensing techniques are used to obtain excellent stability over temperature and power supply variations and a feedback Darlington capacitor discharge circuit minimizes pulse width variation from unit to unit. Schottky TTL output stages provide high switching speeds and output compatibility with all TTL logic families.

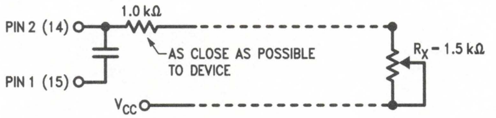
Operation Notes

TIMING

1. An external resistor (R_X) and an external capacitor (C_X) are required as shown in the Logic Diagram. The value of R_X may vary from 1.0 kΩ to 2.0 MΩ (DM96S02).
2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to V_{CC}/R_X the timing equations may not represent the pulse width obtained.
3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 1(15), the (−) terminal to pin 2(14) and R_X. Pin 1(15) will remain positive with respect to pin 2(14) during the timing cycle. However, during quiescent (non-triggered) conditions, pin 1(15) may go negative with respect to pin 2(14) depending on values of R_X and V_{CC}. For values of $R_X \geq 10$ kΩ the maximum amount of capacitor reverse polarity, pin 1(15) negative with respect to pin 2(14) is 500 mV. Most tantalum electrolytic capacitors are rated for safe reverse bias operation up to 5% of their working forward voltage rating; therefore, capacitors having a rating of 10 WVdc or higher should be used with the DM96S02 when $R_X \geq$ 10 kΩ.
4. The output pulse width t_w for $R_X \geq 10$ kΩ and $C_X \geq$ 1000 pF is determined as follows:

   $t_w = 0.55\ R_X C_X$

   Where R_X is in kΩ, C_X is in pF, t is in ns *or* RT_X is in kΩ, C_X is in μF, t is in ms.
5. The output pulse width for $R_X < 10$ kΩ or $C_X < 1000$ pF should be determined from pulse width versus C_X or R_X graphs.
6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



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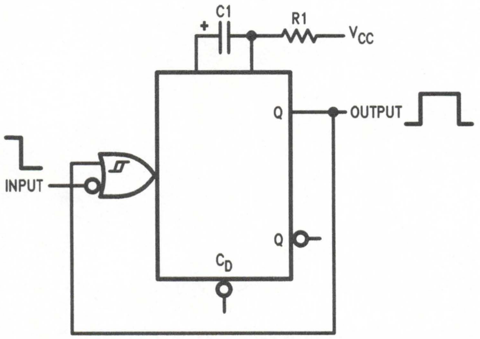
7. Under any operating condition, C_X and R_X (Min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. V_{CC} and ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and ground leads do not cause interaction between one shots. Use of a 0.01 μF to 0.1 μF bypass capacitor between V_{CC} and ground located near the circuit is recommended.

TRIGGERING

1. The minimum negative pulse width into $\overline{\text{I}}$0 is 8.0 ns; the minimum positive pulse width into I1 is 12 ns.
2. Input signals to the DM96S02 exhibiting slow or noisy transitions should use the positive trigger input I1 which contains a Schmitt trigger. Input signals to the 96LS02 exhibiting slow or noisy transitions can use either trigger as both are Schmitt triggers.
3. When non-retriggerable operation is required, i.e., when input triggers are to be ignored during quasi-stable state, input latching is used to inhibit retriggering.
4. An overriding active LOW level direct clear is provided on each multivibrator. By applying a LOW to the clear, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW. A LOW-to-HIGH transition on $\overline{C}_D$ will not trigger the DM96S02. If the $\overline{C}_D$ input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.



NEGATIVE EDGE TRIGGER

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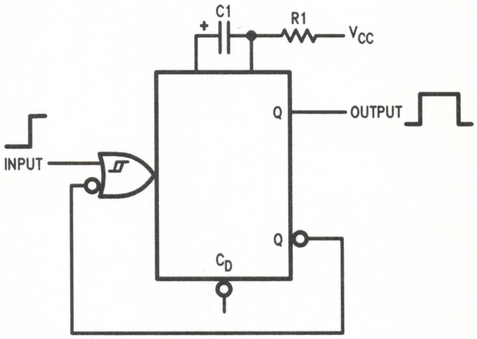

POSITIVE EDGE TRIGGER

TL/F/9810–6

Section 4
TTL

Section 4—TTL

TTL—Commercial Products

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DM7401 Quad 2-Input NAND Gate with Open-Collector Outputs 4-5
DM7402 Quad 2-Input NOR Gate 4-7
DM7403 Quad 2-Input NAND Gate with Open-Collector Outputs 4-9
DM7404 Hex Inverter 4-11
DM7405 Hex Inverter with Open-Collector Outputs 4-13
DM7406 Hex Inverting Buffer/Driver with High-Voltage Open-Collector Outputs 4-15
DM7407 Hex Buffer/Driver with High-Voltage Open-Collector Outputs 4-17
DM7408 Quad 2-Input AND Gate 4-19
DM7409 Quad 2-Input AND Gate with Open-Collector Outputs 4-21
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DM7417 Hex Buffer/Driver with High-Voltage Open-Collector Outputs 4-32
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DM7426 Quad 2-Input NAND Buffer with High-Voltage Open-Collector Outputs 4-38
DM7427 Triple 3-Input NOR Gate 4-40
DM7430 8-Input NAND Gate 4-42
DM7432 Quad 2-Input OR Gate 4-44
DM7437 Quad 2-Input NAND Buffer 4-46
DM7438 Quad 2-Input NAND Buffer with Open-Collector Output 4-48
DM7439 Quad 2-Input NAND Buffer with Open-Collector Output 4-50
DM7440 Dual 4-Input NAND Buffer 4-52
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DM7445 BCD to Decimal Decoder/Driver 4-58
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DM7497 Synchronous Modulo 64 Bit Rate Multiplier 4-104
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Section 4—TTL (Continued)

TTL—Commercial Products (Continued)

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DM74170 4-by-4 Register File with Open-Collector Outputs 4-177
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DM9322 Quad 1-of-2 Line Data Selector/Multiplexer 4-294
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DM9370 7-Segment Decoder/Driver/Latch with Open-Collector Outputs 4-322
DM9374 7-Segment Decoder/Driver/Latch with Constant Current Sink Outputs 4-327
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DM9601 Retriggerable Monostable Multivibrator (One-Shot) with Complementary Outputs 4-337
DM9602 Dual Retriggerable Monostable Multivibrator (One-Shot) with Complementary Outputs 4-341
DM96101 Quad 2-Input Positive NAND Buffer with Open-Collector Outputs 4-346

TTL—Mil/Aero Products

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DM5401 Quad 2-Input NAND Gate with Open-Collector Outputs 4-5

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TTL—Mil/Aero Products (Continued)

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DM5445 BCD to Decimal Decoder/Driver 4-58
DM5447A BCD to 7-Segment Decoder/Driver with Open-Collector Outputs 4-61
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5474/DM5474 Dual Positive-Edge-Triggered D Flip-Flop with Preset, Clear and Complementary Outputs 4-75
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DM54181 Arithmetic Logic Unit/Function Generator 4-193
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National Semiconductor

5400/DM5400/DM7400 Quad 2-Input NAND Gates

General Description

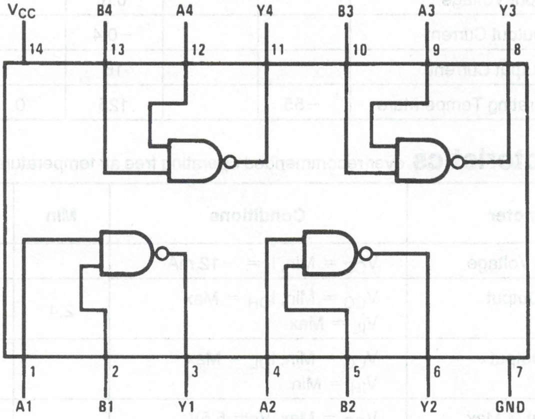
This device contains four independent gates each of which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (5400) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6613-1

Order Number 5400DMQB, 5400FMQB, DM5400J, DM5400W or DM7400N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5400			DM7400			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2) DM54	−20		−55	mA
		DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		4	8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		12	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5401/DM7401 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

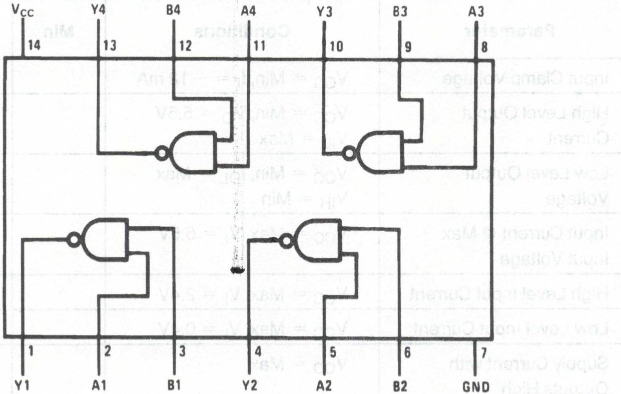
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6614–1

Order Number DM5401J, DM5401W or DM7401N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5401			DM7401			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		4	8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		12	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 4 kΩ (t_{PLH}) R_L = 400Ω (t_{PHL})		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

5402/DM5402/DM7402 Quad 2-Input NOR Gates

General Description

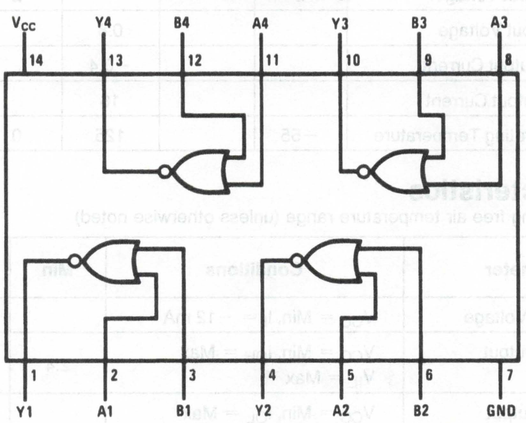
This device contains four independent gates each of which performs the logic NOR function.

Features

- Alternate Military/Areospace device (5402) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6492-1

Order Number 5402DMQB, 5402FMQB, DM5402J, DM5402W or DM7402N
See NS Package Number J14A, N14A or W14B

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5402			DM7402			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			8	16	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			14	27	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5403/DM7403 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

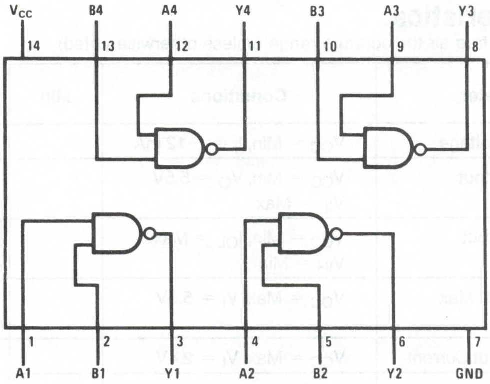
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6493-1

Order Number DM5403J or DM7403N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5403			DM7403			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		4	8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		12	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 4 kΩ (t_{PLH}) R_L = 400Ω (t_{PHL})		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

5404/DM5404/DM7404 Hex Inverting Gates

General Description

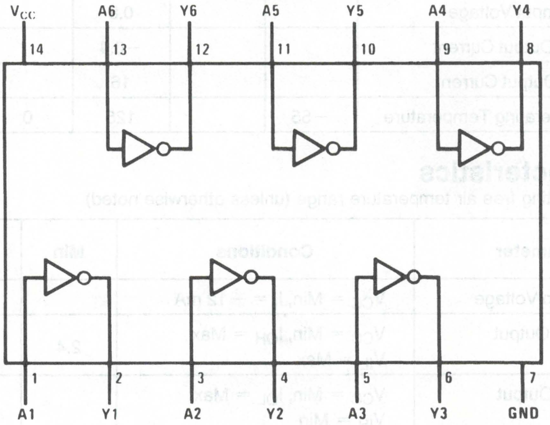
This device contains six independent gates each of which performs the logic INVERT function.

Features

- Alternate Military/Aerospace device (5404) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6494–1

Order Number 5404DMQB, 5404FMQB, DM5404J, DM5404W, DM7404M or DM7404N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

$$Y = \overline{A}$$

Inputs	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5404			DM7404			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			6	12	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			18	33	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5405/DM7405 Hex Inverters with Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

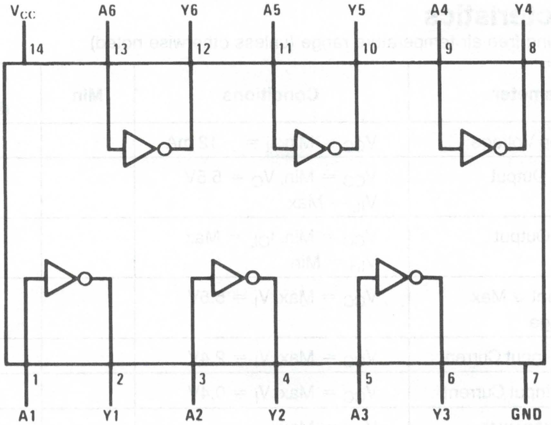
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6495–1

Order Number DM5405J, DM5405W or DM7405N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5405			DM7405			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		6	12	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		18	33	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 4 kΩ (t_{PLH}) R_L = 400Ω (t_{PHL})		55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM5406/DM7406 Hex Inverting Buffers with High Voltage Open-Collector Outputs

General Description

This device contains six independent buffers each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(\mathrm{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(\mathrm{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

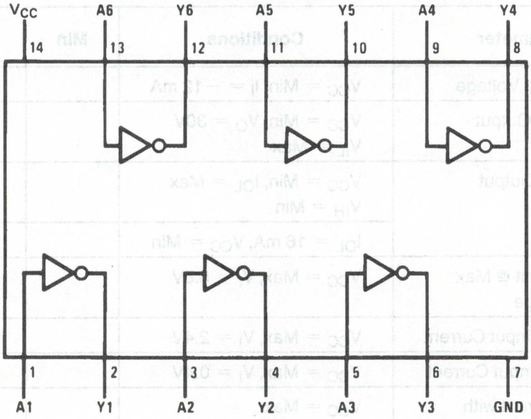
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6496–1

Order Number DM5406J, DM5406W, DM7406M or DM7406N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	30V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5406			DM7406			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			30			30	V
I_{OL}	Low Level Output Current			30			40	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 30V V_{IL} = Max			250	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.7	V
		I_{OL} = 16 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		30	48	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		27	51	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 110Ω		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			23	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

DM5407/DM7407 Hex Buffers with High Voltage Open-Collector Outputs

General Description

This device contains six independent gates each of which performs a buffer function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

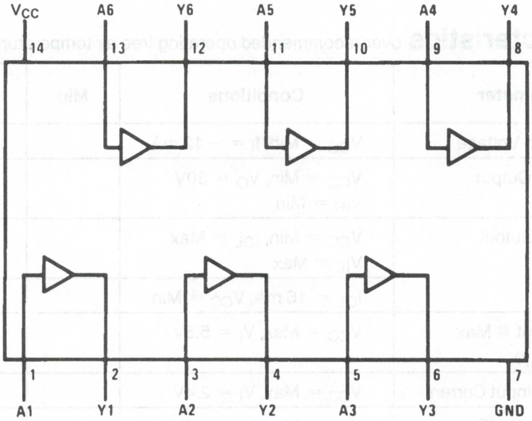
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6497-1

Order Number DM5407J, DM5407W, DM7407M or DM7407N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

Y = A

Input	Output
A	Y
L	L
H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	30V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5407			DM7407			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			30			30	V
I_{OL}	Low Level Output Current			30			40	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 30V V_{IH} = Min			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max			0.7	V
		I_{OL} = 16 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		29	41	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		21	30	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 110Ω		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

5408/DM5408/DM7408
Quad 2-Input AND Gates

General Description

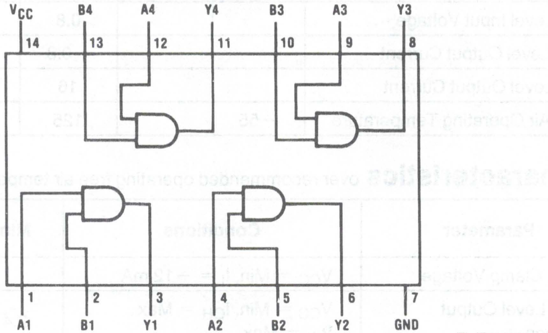
This device contains four independent gates each of which performs the logic AND function.

Features

- ■ Alternate Military/Aerospace device (5408) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6498–1

Order Number 5408DMQB, 5408FMQB, DM5408J, DM5408W or DM7408N
See NS Package Number J14A, N14A or W14B

Function Table

Y = AB

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5408			DM7408			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			11	21	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			20	33	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			19	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

5409/DM7409 Quad 2-Input AND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

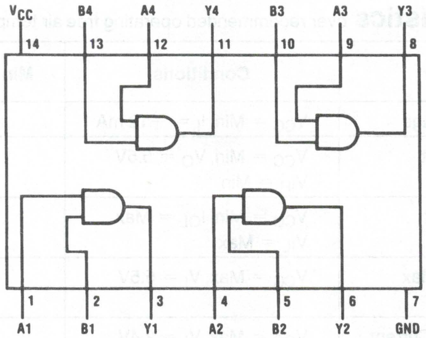
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6499-1

Order Number 5409DMQB, 5409FMQB or DM7409N
See NS Package Number J14A, N14A or W14B

Function Table

Y = AB

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	5409			DM7409			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IH} = Min			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		11	21	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		20	33	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			24	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

5410/DM5410/DM7410 Triple 3-Input NAND Gates

General Description

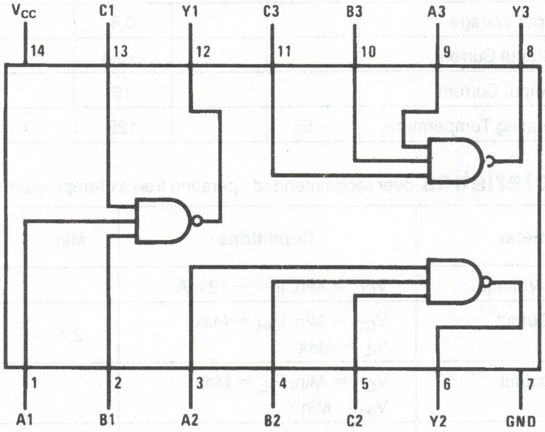
This device contains three independent gates each of which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (5410) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6500-1

Order Number 5410DMQB, 5410FMQB, DM5410J, DM5410W or DM7410N
See NS Package Number J14A, N14A or W14B

Function Table

$$Y = \overline{ABC}$$

Inputs			Output
A	**B**	**C**	**Y**
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5410			DM7410			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			3	6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			9	16.5	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

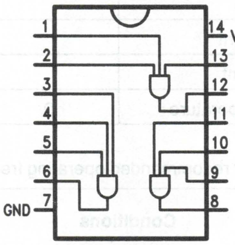
DM7411
Triple 3-Input AND Gate

General Description

This device contains three independent gates with three data inputs each which perform the logic AND function.

Connection Diagram

Dual-In-Line Package



TL/F/9774–1

Order Number DM7411N
NS Package Number N14A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range (DM74)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operations.*

Recommended Operating Conditions

Symbol	Parameter	DM7411			Units
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−18		−57	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			15	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			24	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF, R_L = 400Ω		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			19	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

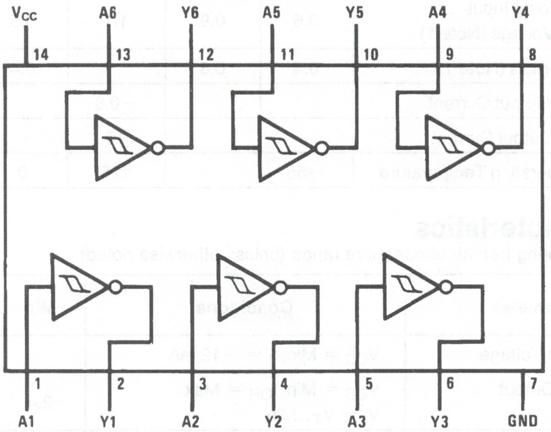
DM5414/DM7414 Hex Inverter with Schmitt Trigger Inputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Connection Diagram

Dual-In-Line Package



TL/F/6503–1

Order Number DM5414J, DM5414W or DM7414N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5414			DM7414			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.5	1.7	2	1.5	1.7	2	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.6	0.9	1.1	0.6	0.9	1.1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_I = V_{T-}Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_I = V_{T+}Max			0.2	0.4	V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}			−0.43		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}			−0.56		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−18		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			22	36	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			39	60	mA

Note 1: V_{CC} = 5V

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			22	ns

National Semiconductor

DM5416/DM7416 Hex Inverting Buffers with High Voltage Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(\mathrm{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(\mathrm{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

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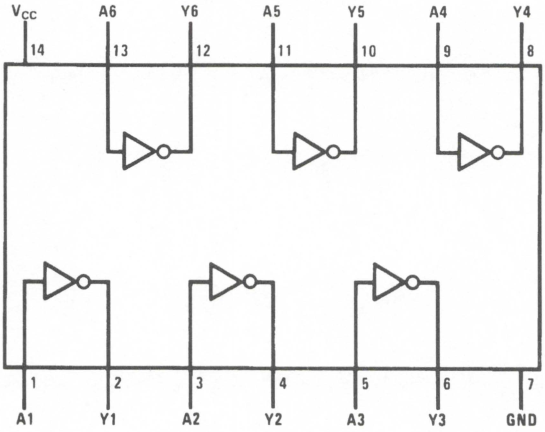
Connection Diagram

Dual-In-Line Package



TL/F/6504-1

Order Number DM5416J, DM5416W or DM7416N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	15V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5416			DM7416			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			30			40	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 15V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.7	V
		I_{OL} = 16 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		30	48	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		27	51	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 110Ω		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			23	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM5417/DM7417 Hex Buffers with High Voltage Open-Collector Outputs

General Description

This device contains six independent gates each of which performs a buffer function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

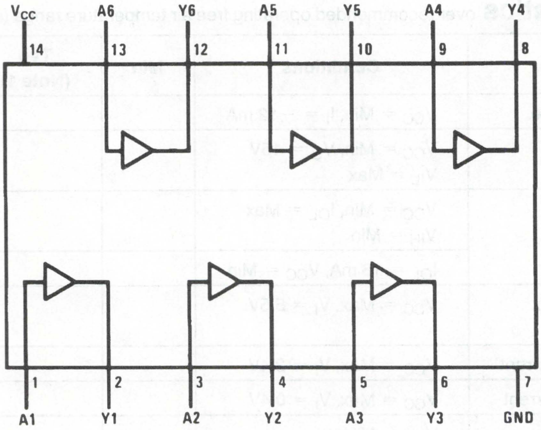
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6505-1

Order Number DM5417J, DM5417W or DM7417N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = A$

Input	Output
A	**Y**
L	L
H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	15V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5417			DM7417			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			30			40	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 15V V_{IH} = Min			250	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max			0.7	V
		I_{OL} = 16 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		29	41	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		21	30	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 110Ω		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor

5420/DM5420/DM7420 Dual 4-Input NAND Gates

General Description

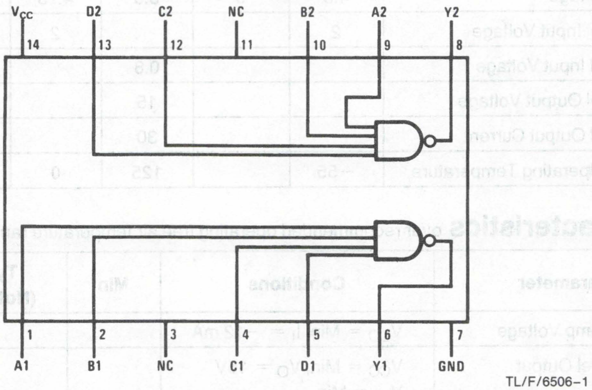
This device contains two independent gates each of which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (5420) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 5420DMQB, 5420FMQB, DM5420J, DM5420W or DM7420N
See NS Package Number J14A, N14A or W14B

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	**B**	**C**	**D**	**Y**
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5402			DM7402			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			2	4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			6	11	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

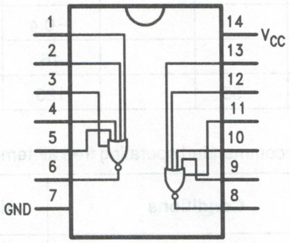
5425/DM7425
Dual 4-Input NOR Gate (with Strobe)

General Description

This device contains two, 4-input gates that perform the logic NOR function. The output of each NOR gate is gated (strobed) by pin 3 and pin 11 by positive true logic i.e., logic "1" equals output on.

Connection Diagram

Dual-In-Line Package



TL/F/9775–1

Order Number 5425DMQB, 5425FMQB, DM7425J or DM7425N
See NS Package Number J14A, N14A and W14B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	5425			DM7425			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Strobe			160	µA
			Inputs			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Strobe			−6.4	mA
			Inputs			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54	−20		−55	mA
			DM74	−18		−57	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max				16	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max				19	mA

Switching Characteristics at V_{CC} = 5V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5426/DM7426 Quad 2-Input NAND Gates with High Voltage Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

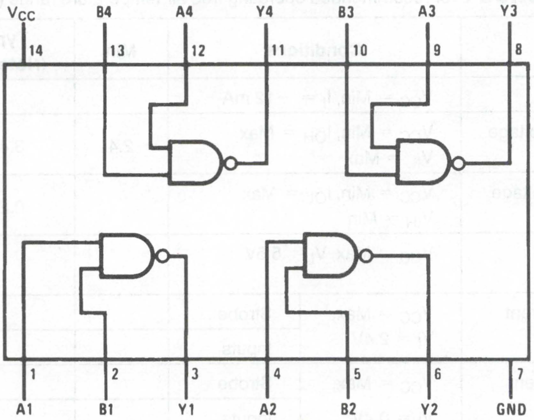
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6508–1

Order Number DM5426J or DM7426N
See NS Package Number J14A or N14A

Function Table

$Y = \overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	15V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5426			DM7426			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min V_{IL} = Max	V_O = 15V			1000	μA
			V_O = 12V			50	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			4	8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			12	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 1 kΩ (t_{PLH})		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			17	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

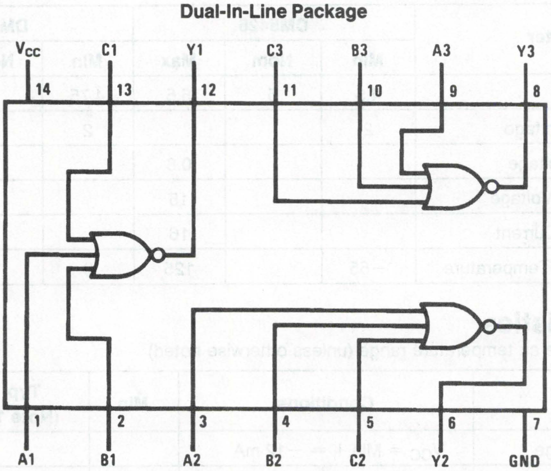
National Semiconductor

DM7427 Triple 3-Input NOR Gates

General Description

This device contains three independent gates each of which performs the logic NOR function.

Connection Diagram


Dual-In-Line Package
V_{CC}
C1
Y1
C3
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
A2
B2
C2
Y2
GND

TL/F/6509–1

Order Number DM7427N
See NS Package Number N14A

Function Table

$$Y = \overline{A + B + C}$$

Inputs			Output
A	**B**	**C**	**Y**
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = High Logic Level
L = Low Logic Level
X = Either High or Low Logic Level

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7427			Units
		Min	**Nom**	**Max**	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.8	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−18		−57	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		10	16	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		16	26	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

5430/DM5430/DM7430 8-Input NAND Gate

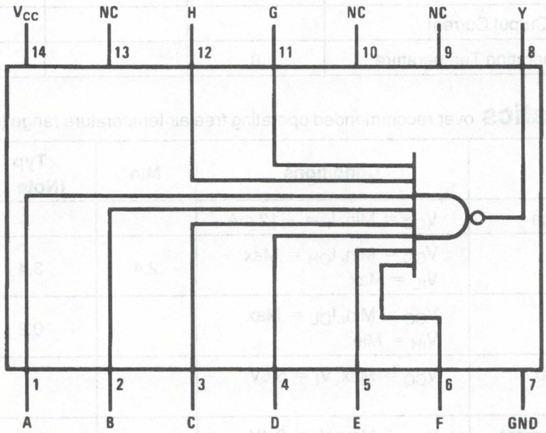
General Description

This device contains a single gate which performs the logic NAND function.

- Alternate Military/Aerospace device (5430) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6510-1

Order Number 5430DMBQ, 5430FMQB, DM5430J, DM5430W or DM7430N
See NS Package Number J14A, N14A or W14B

Function Table

$$Y = \overline{ABCDEFGH}$$

Inputs	Output
A thru H	**Y**
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5430			DM7430			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1	2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

5432/DM5432/DM7432 Quad 2-Input OR Gates

General Description

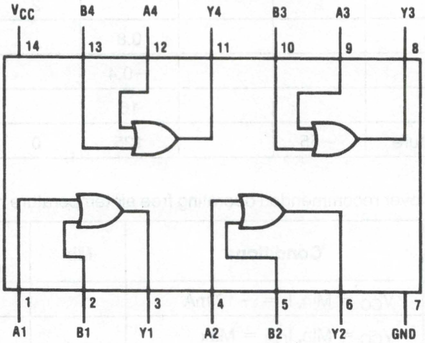
This device contains four independent gates each of which performs the logic OR function.

Features

- Alternate Military/Aerospace device (5432) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6511–1

Order Number 5432DMQB, 5432FMQB, DM5432J, DM5432W or DM7432N
See NS Package Number J14A, N14A or W14B

Function Table

Y = A + B

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	$-55^{\circ}C$ to $+125^{\circ}C$
DM74	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5432			DM7432			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -12\text{ mA}$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IH} = \text{Min}$		2.4	3.4		V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IL} = \text{Max}$			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5V$				1	mA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4V$				40	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4V$				−1.6	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	$V_{CC} = \text{Max}$			15	22	mA
I_{CCL}	Supply Current with Outputs Low	$V_{CC} = \text{Max}$			23	38	mA

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^{\circ}C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 15\text{ pF}$ $R_L = 400\Omega$		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			22	ns

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

5437/DM5437/DM7437 Quad 2-Input NAND Buffers

General Description

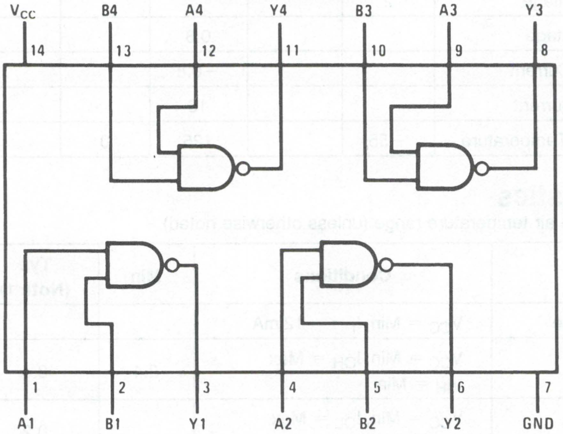
This device contains four independent gates each of which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (5437) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6512–1

Order Number 5437DMQB, 5437FMQB, DM5437J, DM5437W or DM7437N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5437			DM7437			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1.2			−1.2	mA
I_{OL}	Low Level Output Current			48			48	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−70	mA
			DM74	−18		−70	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			9	15.5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			34	54	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF R_L = 133Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

DM5438/DM7438 Quad 2-Input NAND Buffers with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

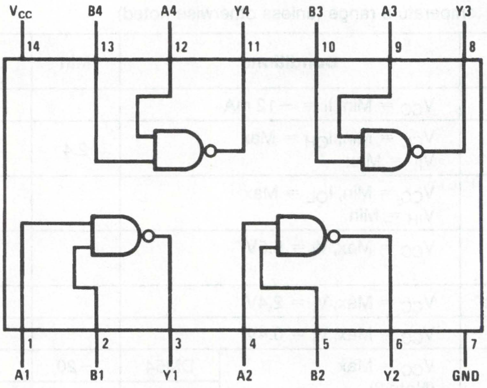
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6513–1

Order Number DM5438J, DM5438W, DM7438M or DM7438N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5438			DM7438			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			48			48	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.4	V
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		5	8.5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		34	54	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF R_L = 133Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

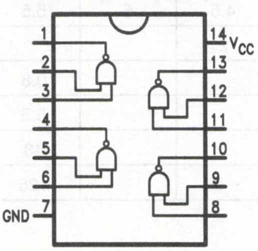
National Semiconductor

DM7439 Quad 2-Input NAND Buffer with Open-Collector Output

General Description

This device contains four independent gates with two data inputs, each which performs the logic NAND function.

Connection Diagram



Dual-In-Line Package

TL/F/9776–1

Order Number DM7439N
See NS Package Number N14A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7439			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.25	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = 250 μA V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 48 mA		0.2	0.4	V
		V_{IH} = 2.0V	I_{OL} = 60 mA			0.5	
			I_{OL} = 80 mA			0.6	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−18		−57	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max				8.5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max				54	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

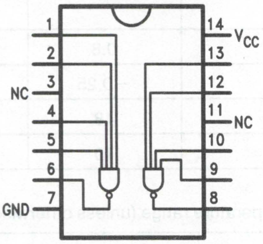
5440/DM7440 Dual 4-Input NAND Buffer

General Description

This device contains two, 4 input gates that perform the Logic NAND function. Outputs have 48 mA I_{OL}.

Connection Diagrams

Dual-In-Line Package


1
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3
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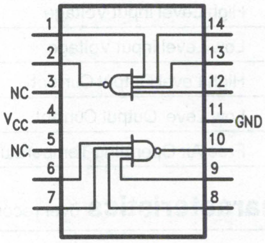
6
7
14
13
12
11
10
9
8
NC
GND
V_{CC}
NC

TL/F/9777–1

Order Number 5440DMQB, DM5440J or DM7440N
See NS Package Number J14A or N14A

Cerpak


1
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11
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9
8
NC
V_{CC}
NC
GND

TL/F/9777–2

Order Number 5440FMQB
See NS Package Number W14B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	5440			DM7440			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1.2			−0.4	mA
I_{OL}	Low Level Output Current			48			48	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -12\text{ mA}$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$		2.4	3.4		V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}$			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5V$				1	mA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4V$				40	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4V$				−1.6	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	54	−20		−70	mA
			DM74	−18		−70	
I_{CCH}	Supply Current with Outputs High	$V_{CC} = \text{Max}$				8	mA
I_{CCL}	Supply Current with Outputs Low	$V_{CC} = \text{Max}$				27	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

National Semiconductor

5442A/DM5442A/DM7442A BCD to Decimal Decoders

General Description

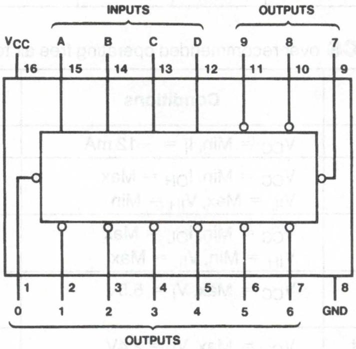
These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10–15) input conditions.

Features

- Diode clamped inputs
- Also for application as 4-line-to-16-line decoders; 3-line-to-8-line decoders
- All outputs are high for invalid input conditions
- Typical power dissipation 140 mW
- Typical propagation delay 17 ns
- Alternate Military/Aerospace device (5442A) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6516–1

Order Number 5442ADMQB, 5442AFMQB, DM5442AJ, DM5442AW or DM7442AN
See NS Package Number J16A, N16E or W16A

Function Table

No.	BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
I	H	L	H	L	H	H	H	H	H	H	H	H	H	H
N	H	L	H	H	H	H	H	H	H	H	H	H	H	H
V	H	H	L	L	H	H	H	H	H	H	H	H	H	H
A	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
I	H	H	H	H	H	H	H	H	H	H	H	H	H	H
D														

H = High Level
L = Low Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5442A			DM7442A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		28	41	mA
			DM74		28	56	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

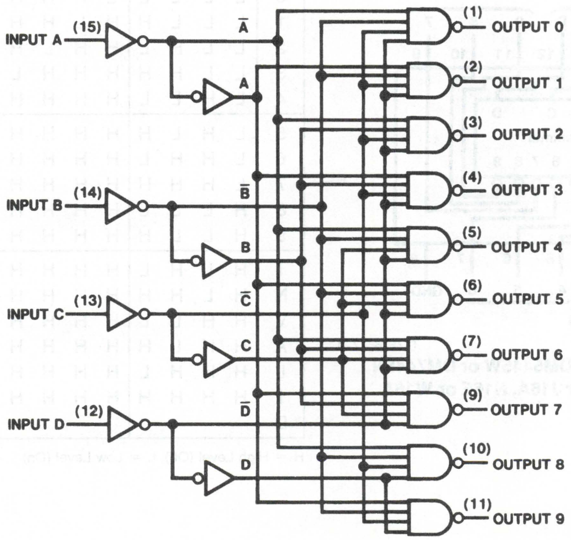
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PHL}	Propagation Delay Time High to Low Level Output from A, B, C or D through 2 Levels of Logic	C_L = 15 pF R_L = 400Ω		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output from A, B, C or D through 3 Levels of Logic			30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output from A, B, C or D through 2 Levels of Logic			25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output from A, B, C or D through 3 Levels of Logic			30	ns

Logic Diagram


INPUT A
(15)
$\overline{A}$
A
INPUT B
(14)
$\overline{B}$
B
INPUT C
(13)
$\overline{C}$
C
INPUT D
(12)
$\overline{D}$
D
(1) OUTPUT 0
(2) OUTPUT 1
(3) OUTPUT 2
(4) OUTPUT 3
(5) OUTPUT 4
(6) OUTPUT 5
(7) OUTPUT 6
(9) OUTPUT 7
(10) OUTPUT 8
(11) OUTPUT 9

TI/F/6516–2

National Semiconductor

DM5445/DM7445 BCD to Decimal Decoders/Drivers

General Description

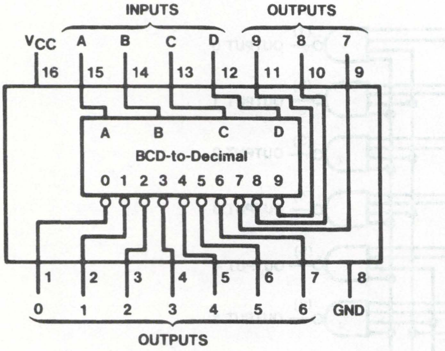
These BCD-to-decimal decoders/drivers consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (10–15) binary input conditions. These decoders feature high-performance, NPN output transistors designed for use as indicator/relay drivers, or as open-collector logic-circuit drivers. The high-breakdown output transistors are compatible for interfacing with most MOS integrated circuits.

Features

- Full decoding of input logic
- 80 mA sink-current capability
- All outputs are off for invalid BCD input conditions

Connection Diagram

Dual-In-Line Package



TL/F/6517-1

Order Number DM5445J, DM5445W or DM7445N
See NS Package Number J16A, N16E or W16A

Function Table

No.	Inputs				Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
I	H	L	H	L	H	H	H	H	H	H	H	H	H	H
N	H	L	H	H	H	H	H	H	H	H	H	H	H	H
V	H	H	L	L	H	H	H	H	H	H	H	H	H	H
A	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
I	H	H	H	H	H	H	H	H	H	H	H	H	H	H
D														

H = High Level (Off), L = Low Level (On)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	30V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5445			DM7445			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			30			30	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 30V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
		I_{OL} = 80 mA V_{CC} = Min			0.5	0.9	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)	DM54		43	62	mA
			DM74		43	70	

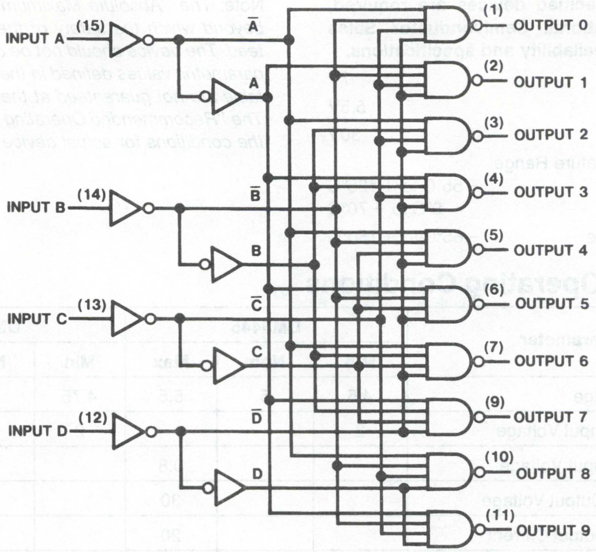
Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 100Ω		49.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			49.5	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all inputs grounded and all outputs open.

Logic Diagram


INPUT A
(15)
INPUT B
(14)
INPUT C
(13)
INPUT D
(12)
$\overline{A}$
A
$\overline{B}$
B
$\overline{C}$
C
$\overline{D}$
D
(1) OUTPUT 0
(2) OUTPUT 1
(3) OUTPUT 2
(4) OUTPUT 3
(5) OUTPUT 4
(6) OUTPUT 5
(7) OUTPUT 6
(9) OUTPUT 7
(10) OUTPUT 8
(11) OUTPUT 9

TL/F/6517-2

National Semiconductor

DM7446A, DM5447A/DM7447A BCD to 7-Segment Decoders/Drivers

General Description

The 46A and 47A feature active-low outputs designed for driving common-anode LEDs or incandescent indicators directly. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown on a following page. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

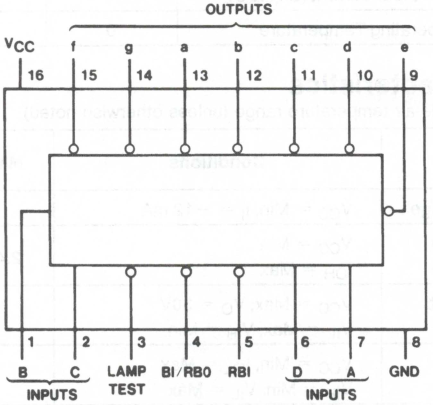
All of the circuits incorporate automatic leading and/or trailing-edge, zero-blanking control (RBI and RBO). Lamp test (LT) of these devices may be performed at any time when the BI/RBO node is at a high logic level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity (by pulsing) or to inhibit the outputs.

Features

- All circuit types feature lamp intensity modulation capability
- Open-collector outputs drive indicators directly
- Lamp-test provision
- Leading/trailing zero suppression

Connection Diagram

Dual-In-Line Package



TL/F/6518-1

Order Number DM5447AJ, DM7446AN or DM7447AN
See NS Package Number J16A or N16E

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7446A			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			30	V
I_{OH}	High Level Output Current (BI/RBO)			−0.2	μA
I_{OL}	Low Level Output Current (a thru g)			40	mA
I_{OL}	Low Level Output Current (BI/RBO)			8	mA
T_A	Free Air Operating Temperature	0		70	°C

'46A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage (BI/RBO)	V_{CC} = Min I_{OH} = Max		2.4	3.7		V
I_{CEX}	High Level Output Current (a thru g)	V_{CC} = Max, V_O = 30V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.3	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V (Except BI/RBO)				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V (Except BI/RBO)				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	BI/RBO			−4	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (BI/RBO)				−4	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			60	103	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs at 4.5V.

'46A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 120Ω		100	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			100	ns

Recommended Operating Conditions

Symbol	Parameter	DM5447A			DM7447A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			15			15	V
I_{OH}	High Level Output Current (BI/RBO)			−0.2			−0.2	μA
I_{OL}	Low Level Output Current (a thru g)			40			40	mA
I_{OL}	Low Level Output Current (BI/RBO)			8			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'47A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage (BI/RBO)	V_{CC} = Min I_{OH} = Max		2.4	3.7		V
I_{CEX}	High Level Output Current (a thru g)	V_{CC} = Max, V_O = 15V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.3	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	BI/RBO			−4	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (BI/RBO)				−4	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)	DM54		60	85	mA
			DM74		60	103	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs at 4.5V.

'47A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 120Ω		100	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			100	ns

Function Table

46A, 47A

Decimal or Function	Inputs						BI/RBO (Note 1)	Outputs							Note
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(2)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(3)
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(4)
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(5)

Note 1: BI/RBO is a wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

Note 2: The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

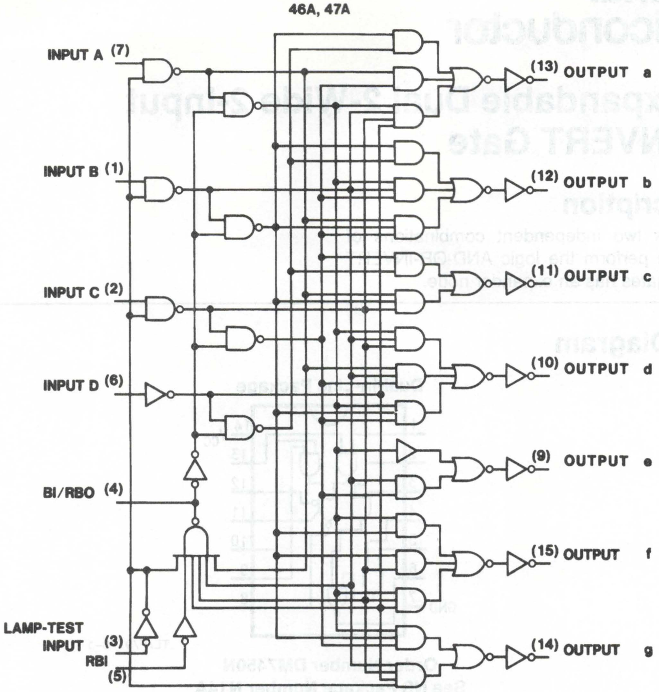
Note 3: When a low logic level is applied directly to the blanking input (BI), all segment outputs are high regardless of the level of any other input.

Note 4: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go H and the ripple-blanking output (RBO) goes to a low level (response condition).

Note 5: When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are L .

H = High level, L = Low level, X = Don't Care

Logic Diagram


46A, 47A
INPUT A (7)
INPUT B (1)
INPUT C (2)
INPUT D (6)
BI/RBO (4)
LAMP-TEST INPUT (3)
RBI (5)
(13) OUTPUT a
(12) OUTPUT b
(11) OUTPUT c
(10) OUTPUT d
(9) OUTPUT e
(15) OUTPUT f
(14) OUTPUT g

TL/F/6518-2

National Semiconductor

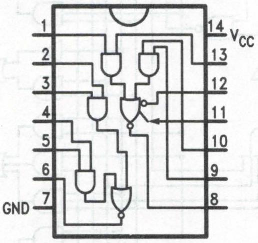
DM7450 Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate

General Description

This device contains two independent combinations of gates, each of which perform the logic AND-OR-INVERT function. One set of gates has an expander node.

Connection Diagram

Dual-In-Line Package



TL/F/9778–1

Order Number DM7450N
See NS Package Number N14A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7450			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −400 μA V_{IL} = Max	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Max		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_X	Expander Current	V1 = 0.4V, I_{OL} = 16 mA V_{CC} = Min, T_A = Min			3.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−18		−57	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			14	mA
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q	I1 = 0.62 mA I_{OL} = 16 mA R_1 = 0Ω			1.0	V

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

5451/DM7451

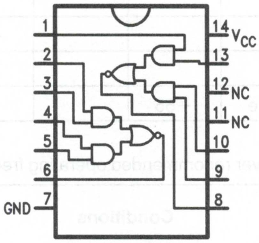
Dual 2-Wide, 2-Input AOI Gate

General Description

This device contains two independent combinations of gates, each of which perform the logic AND-OR-INVERT function.

Connection Diagram

Dual-In-Line Package



TL/F/9779–1

Order Number 5451DMQB, 5451FMQB or DM7451N
See NS Package Number J14A, N14A or W14B

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for acutual device operation.*

Recommended Operating Conditions

Symbol	Parameter	5451			DM7451			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54	−20		−55	mA
			DM74	−18		−57	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max				8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max				14	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

5473/DM5473/DM7473
Dual Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

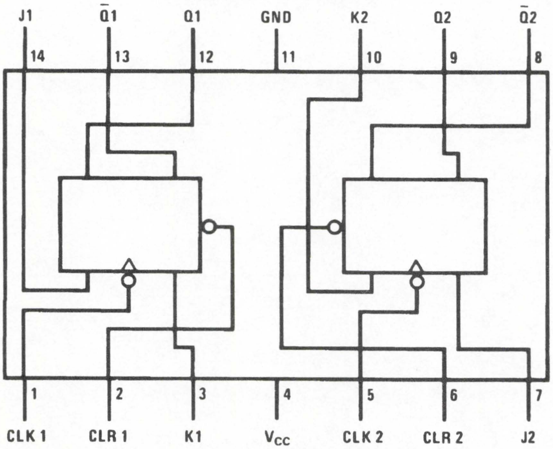
This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic states of the J and K inputs must not be allowed to change while the clock is high. Data transfers to the outputs on the falling edge of the clock pulse. A low logic level on the clear input will reset the outputs regardless of the logic states of the other inputs.

Features

- Alternate Military/Aerospace device (5473) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6525–1

Order Number 5473DMQB, 5473FMQB, DM5473J, DM5473W or DM7473N
See NS Package Number J14A, N14A or W14B

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\overline{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	Toggle	

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

⎍ = Positive pulse data. the J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each high level clock pulse.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM5473			DM7473			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 5)		0		15	0		15	MHz
t_W	Pulse Width (Note 5)	Clock High	20			20			ns
		Clock Low	47			47			
		Clear Low	25			25			
t_{SU}	Input Setup Time (Note 1 & 5)		0↑			0↑			ns
t_H	Input Hold Time (Note 1 & 5)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			40	μA
			Clock			80	
			Clear			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	J, K			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max, (Note 4)			18	34	mA

Note 1: The symbol (↑, ↓) indicates the edge of the clock pulse is used for reference: (↑) for rising edge, (↓) for falling edge.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input grounded.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15$ pF Min	Max	Units
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25	ns

National Semiconductor

5474/DM5474/DM7474
Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

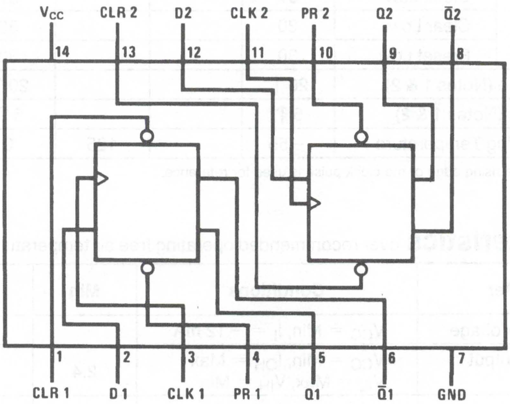
This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate Military/Aerospace device (5474) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6526–1

Order Number 5474DMQB, 5474FMQB, DM5474J, DM5474W, DM7474M or DM7474N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
PR	**CLR**	**CLK**	**D**	**Q**	**$\overline{Q}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Logic Level
X = Either Low or High Logic Level
L = Low Logic Level
↑ = Positive-going transition of the clock.
* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.
Q_0 = The output logic level of Q before the indicated input conditions were established.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM5474			DM7474			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 2)		0		15	0		15	MHz
t_W	Pulse Width (Note 2)	Clock High	30			30			ns
		Clock Low	37			37			
		Clear Low	30			30			
		Preset Low	30			30			
t_{SU}	Input Setup Time (Notes 1 & 2)		20↑			20↑			ns
t_H	Input Hold Time (Notes 1 & 2)		5↑			5↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	D			40	μA
			Clock			80	
			Clear			120	
			Preset			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V (Note 6)	D			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
			Preset			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			17	30	mA

Note 3: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 4: Not more than one output should be shorted at a time.

Note 5: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

Note 6: Clear is tested with preset high and preset is tested with clear high.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15$ pF Min	Max	Units
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25	ns

National Semiconductor

5475/DM5475/DM7475 Quad Latches

General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q input when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

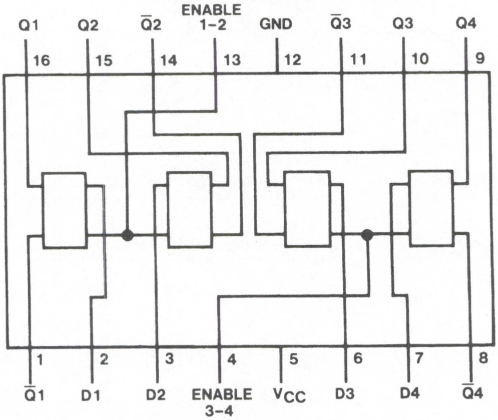
These latches feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch and are available in 16-pin packages.

Features

- Alternate Military/Aerospace device (5475) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package


Q1
Q2
$\overline{Q}$2
ENABLE 1–2
GND
$\overline{Q}$3
Q3
Q4
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
$\overline{Q}$1
D1
D2
ENABLE 3–4
V_{CC}
D3
D4
$\overline{Q}$4

TL/F/6527-1

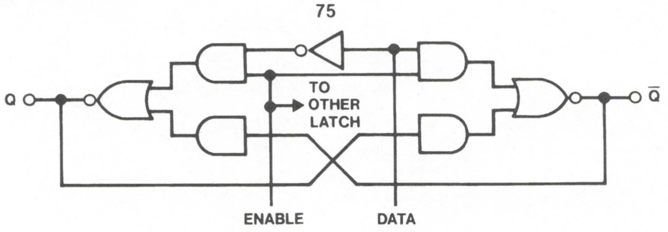
Order Number 5475DMQB, 5475FMQB, DM5475J, DM5475W or DM7475N
See NS Package Number J16A, N16E or W16A

Function Table (Each Latch)

Inputs		Outputs	
D	**G**	**Q**	**$\overline{Q}$**
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level, L = Low Level, X = Don't Care, Q_0 = The Level of Q Before the High-to-Low Transition of G

Logic Diagram (Each Latch)


75
Q
TO OTHER LATCH
$\overline{Q}$
ENABLE
DATA

TL/F/6527-2

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5475			DM7475			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
t_W	Enable Pulse Width (Note 4)	20			20			ns
t_{SU}	Setup Time (Note 4)	20			20			ns
t_H	Hold Time (Note 4)	5			5			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		32	46	mA
			DM74		32	50	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15\ pF$		Units
			Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	D to Q		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to Q		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to $\overline{Q}$		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to $\overline{Q}$		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	G to Q		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	G to Q		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	G to $\overline{Q}$		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	G to $\overline{Q}$		30	ns

National Semiconductor

5476/DM5476/DM7476
Dual Master-Slave J-K Flip-Flops with Clear, Preset, and Complementary Outputs

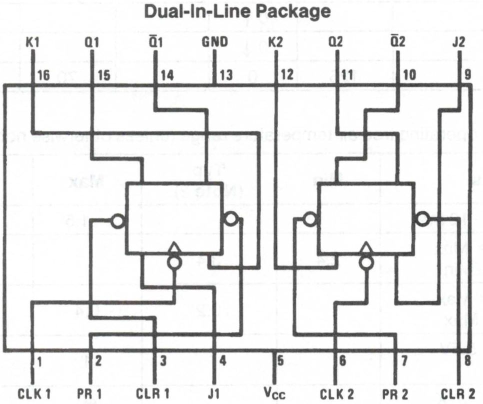
General Description

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic state of J and K inputs must not be allowed to change while the clock is high. The data is transfered to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate Military/Aerospace device (5476) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram



TL/F/6528–1

Order Number 5476DMQB, 5476FMQB, DM5476J, DM5476W or DM7476N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transfered to the outputs on the falling edge of the clock pulse.

* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete active high level clock pulse.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM5476			DM7476			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 6)		0		15	0		15	MHz
t_W	Pulse Width (Note 6)	Clock High	20			20			ns
		Clock Low	47			47			
		Preset Low	25			25			
		Clear Low	25			25			
t_{SU}	Input Setup Time (Notes 1 & 6)		0↑			0↑			ns
t_H	Input Hold Time (Notes 1 & 6)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			40	μA
			Clock			80	
			Clear			80	
			Preset			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V (Note 5)	J, K			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
			Preset			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			18	34	mA

Note 1: The symbol (↑, ↓) indicates the edge of the clock pulse is used for reference (↑) for rising edge, (↓) for falling edge.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

Note 5: Clear is measured with preset high and preset is measured with clear high.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25	ns

National Semiconductor

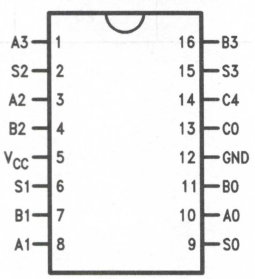
5483A
4-Bit Binary Full Adder with Fast Carry

General Description

The '83A high speed 4-bit binary full adders with internal carry lookahead accept two 4-bit binary words (A_0–A_3, B_0–B_3) and a Carry input (C_0). They generate the binary Sum outputs (S_0–S_3) and the Carry output (C_4) from the most significant bit. They operate with either HIGH or active LOW operands (positive or negative logic). The '283 is recommended for new designs since it features standard corner power pins.

Connection Diagram

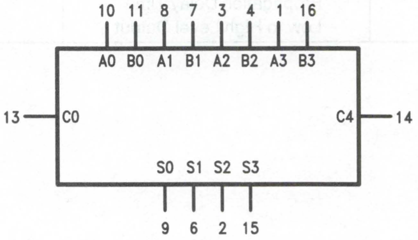
Dual-In-Line Package


A3 1
S2 2
A2 3
B2 4
VCC 5
S1 6
B1 7
A1 8
16 B3
15 S3
14 C4
13 CO
12 GND
11 BO
10 AO
9 SO

TL/F/9613-1

Order Number 5483ADMQB or 5483AFMQB
See NS Package Number J16A or W16A

Logic Symbol


10 11 8 7 3 4 1 16
A0 B0 A1 B1 A2 B2 A3 B3
13 CO
C4 14
S0 S1 S2 S3
9 6 2 15

TL/F/9613-2

V_{CC} = Pin 5
GND = Pin 12

Pin Names	Description
A_0–A_3	A Operand Inputs
B_0–B_3	B Operand Inputs
C_0	Carry Input
S_0–S_3	Sum Ouputs
C_4	Carry Ouput

Truth Table

	Inputs									Outputs					
	C_0	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	S_0	S_1	S_2	S_3	C_4	
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10 + 9 = 19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry + 5 + 6 = 12)

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		5483A			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.8	mA
I_{OL}	Low Level Output Current	S_n			16	mA
		C_4			8	
T_A	Free Air Operating Temperature		−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	Outputs	−20		−55	mA
			C_4	−20		−70	
I_{CC}	Supply Current	V_{CC} = Max				99	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	$C_L = 15$ pF $R_L = 400\Omega$		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_0 to S_n		21 21	ns
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to S_n		24 24	ns
t_{PLH} t_{PHL}	Propagation Delay C_0 to C_4		14 16	ns
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to C_4		14 16	ns

Functional Description

The '83A adds two 4-bit binary words (A and B) plus the incoming carry. The binary sum appears on the sum outputs (S_0–S_3) and outgoing carry (C_4) outputs.

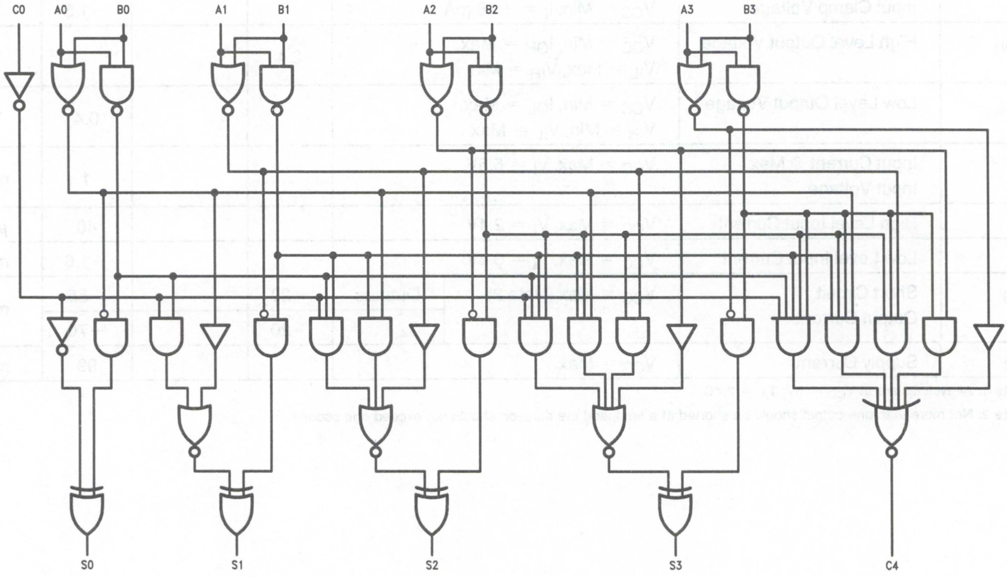
$C_0 + (A_0 + B_0) + 2(A_1 + B_1) + 4(A_2 + B_2) + 8(A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$

Where: (+) = plus

Due to the symmetry of the binary add function the '83A can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry In can not be left open, but must be held LOW when no carry in is intended.

Interchanging inputs of equal weight does not affect the operation, thus C_0, A_0, B_0 can be arbitrarily assigned to pins 10, 11, 13, etc.

Logic Diagram



TL/F/9613-3

National Semiconductor

5485/DM5485/DM7485 4-Bit Magnitude Comparators

General Description

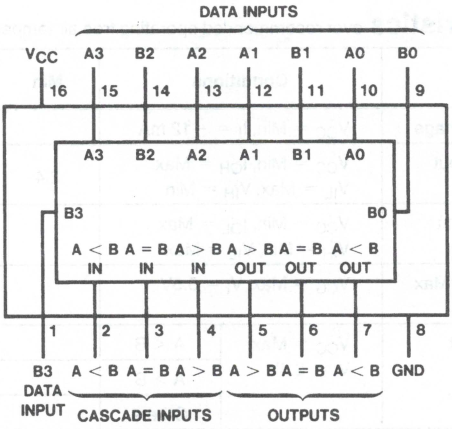
These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words.

Features

- Typical power dissipation 275 mW
- Typical delay (4-bit words) 23 ns
- Alternate Military/Aerospace device (5485) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package


DATA INPUTS
VCC
A3
B2
A2
A1
B1
A0
B0
16
15
14
13
12
11
10
9
A3
B2
A2
A1
B1
A0
B3
B0
A < B IN
A = B IN
A > B IN
A > B OUT
A = B OUT
A < B OUT
1
2
3
4
5
6
7
8
B3 DATA INPUT
A < B
A = B
A > B
A > B
A = B
A < B
GND
CASCADE INPUTS
OUTPUTS

TL/F/6530–1

Order Number 5485DMQB, 5485FMQB, DM5485J, DM5485W or DM7485N
See NS Package Number J16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5485			DM7485			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	A < B			40	μA
			A > B			40	
			Others			120	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	A < B			−1.6	mA
			A > B			−1.6	
			Others			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			55	88	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, A = B input grounded and all other inputs at 4.5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

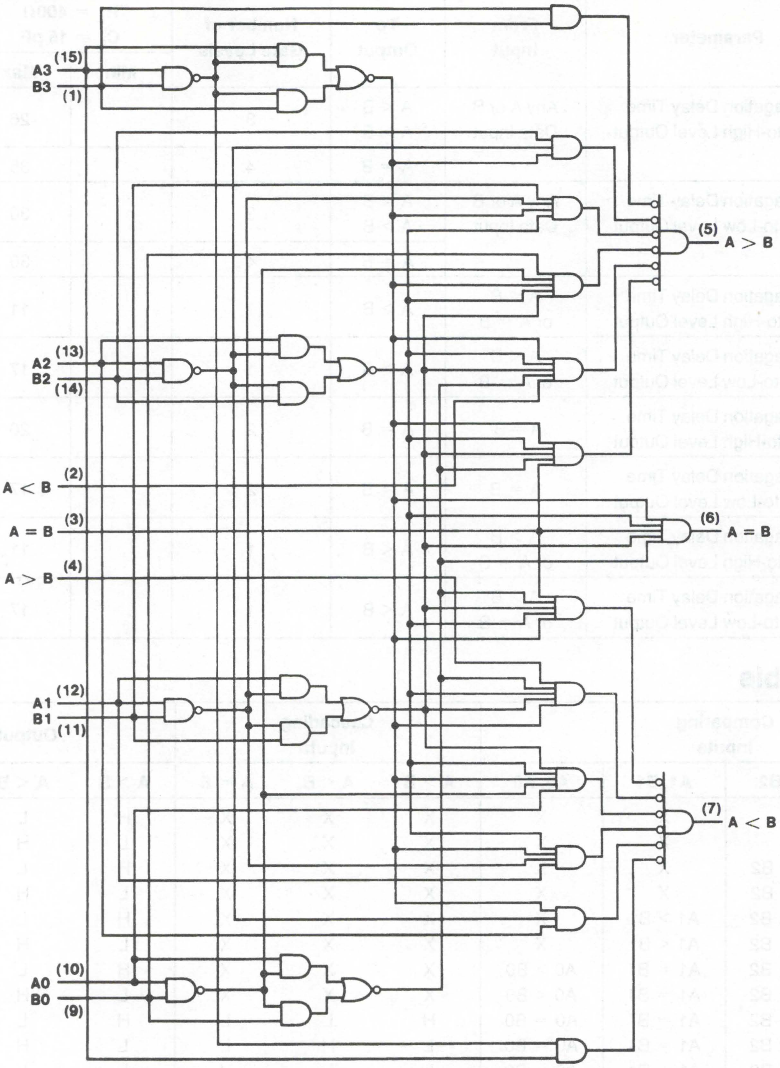
Symbol	Parameter	From Input	To Output	Number of Gate Levels	R_L = 400Ω C_L = 15 pF		Units
					Min	Max	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	Any A or B Data Input	A < B A > B	3		26	ns
			A = B	4		35	
t_{PHL}	Propagation Delay Time High-to-Low Level Output	Any A or B Data Input	A < B A > B	3		30	ns
			A = B	4		30	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A < B or A = B	A > B	1		11	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A < B or A = B	A > B	1		17	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A = B	A = B	2		20	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A = B	A = B	2		17	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A > B or A = B	A < B	1		11	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A > B or A = B	A < B	1		17	ns

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = High Level, L = Low Level, X = Don't Care

Logic Diagram


(15)
A3
B3
(1)
(13)
A2
B2
(14)
(2)
A < B
(3)
A = B
(4)
A > B
(12)
A1
B1
(11)
(10)
A0
B0
(9)
(5)
A > B
(6)
A = B
(7)
A < B

TL/F/6530-2

National Semiconductor

5486/DM5486/DM7486
Quad 2-Input Exclusive-OR Gates

General Description

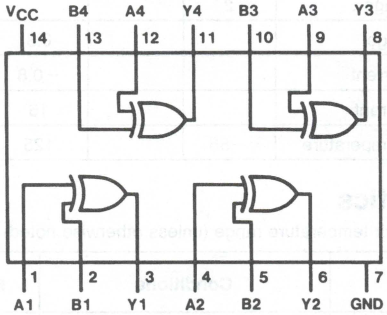
This device contains four independent gates each of which performs the logic exclusive-OR function.

Features

- Alternate Military/Aerospace device (5486) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6531–1

Order Number 5486DMQB, 5486FMQB, DM5486J, DM5486W or DM7486N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = A \oplus B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5486			DM7486			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)	DM54		30	43	mA
			DM74		30	50	
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)			36	57	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open, and all inputs at ground.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	C_L = 15 pF R_L = 400Ω		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input Low		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			17	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input High		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			22	ns

National Semiconductor

5490/DM5490A/DM7490A, DM5493A/DM7493A Decade, and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 90A and divide-by-eight for the 93A.

All of these counters have a gated zero reset and the 90A also has gated set-to-nine inputs for use in BCD nine's complement applications.

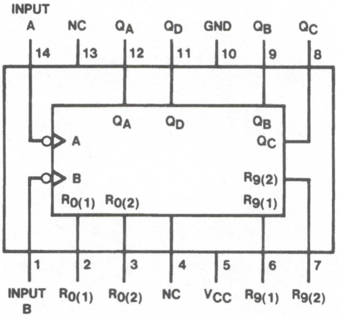
To use their maximum count length (decade or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90A counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

- Typical power dissipation
  - —90A 145 mW
  - —93A 130 mW
- Count frequency 42 MHz
- Alternate Military/Aerospace device (5490) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

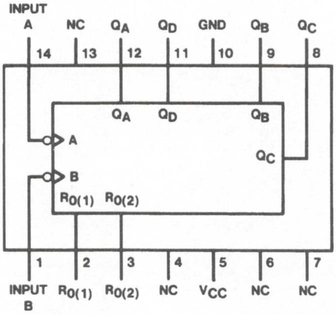
Dual-In-Line Package


INPUT A
NC
QA
QD
GND
QB
QC
14
13
12
11
10
9
8
QA
QD
QB
QC
A
B
R9(2)
R0(1)
R0(2)
R9(1)
1
2
3
4
5
6
7
INPUT B
R0(1)
R0(2)
NC
VCC
R9(1)
R9(2)

TL/F/6533-1

Order Number 5490DMQB, 5490FMQB, DM5490AJ, DM5490AW or DM7490AN
See NS Package Number J14A, N14A or W14B

Dual-In-Line Package


INPUT A
NC
QA
QD
GND
QB
QC
14
13
12
11
10
9
8
QA
QD
QB
A
QC
B
R0(1)
R0(2)
1
2
3
4
5
6
7
INPUT B
R0(1)
R0(2)
NC
VCC
NC
NC

TL/F/6533-2

Order Number DM5493AJ, DM5493AW or DM7493AN
See NS Package Number J14A, N14A or W14B

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM5490A			DM7490A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 5)	A	0		32	0		32	MHz
		B	0		16	0		16	
t_W	Pulse Width (Note 5)	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_{REL}	Reset Release Time (Note 5)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'90A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max (Note 4)			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	A			80	μA
			Reset			40	
			B			120	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	A			−3.2	mA
			Reset			−1.6	
			B			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			29	42	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Note 5: T_A = 25°C and V_{CC} = 5V.

'90A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		MHz
		B to Q_B	16		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		50	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 Any Q		40	ns

Recommended Operating Conditions

Symbol	Parameter		DM5493A Min	DM5493A Nom	DM5493A Max	DM7493A Min	DM7493A Nom	DM7493A Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 5)	A	0		32	0		32	MHz
		B	0		16	0		16	
t_W	Pulse Width (Note 5)	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_{REL}	Reset Release Time (Note 5)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'93A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max (Note 4)			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Reset			40	μA
			A			80	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Reset			−1.6	mA
			A			−3.2	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			26	39	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, both R0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Note 5: T_A = 25°C and V_{CC} = 5V.

'93A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15$ pF Min	Max	Units
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		MHz
		B to Q_B	16		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		70	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		70	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		51	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		51	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40	ns

Function Tables (Note D)

90A
BCD Count Sequence
(See Note A)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

90A
BCD Bi-Quinary (5-2)
(See Note B)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

93A
Count Sequence
(See Note C)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

90A
Reset/Count Function Table

Reset Inputs				Outputs			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

93A
Reset/Count Function Table

Reset Inputs		Outputs			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

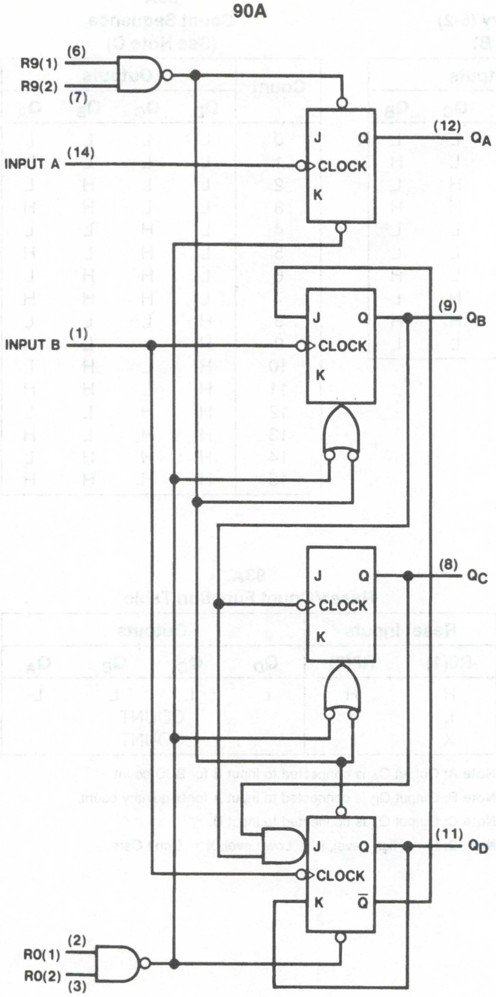
Note A: Output Q_A is connected to input B for BCD count.

Note B: Output Q_D is connected to input A for bi-quinary count.

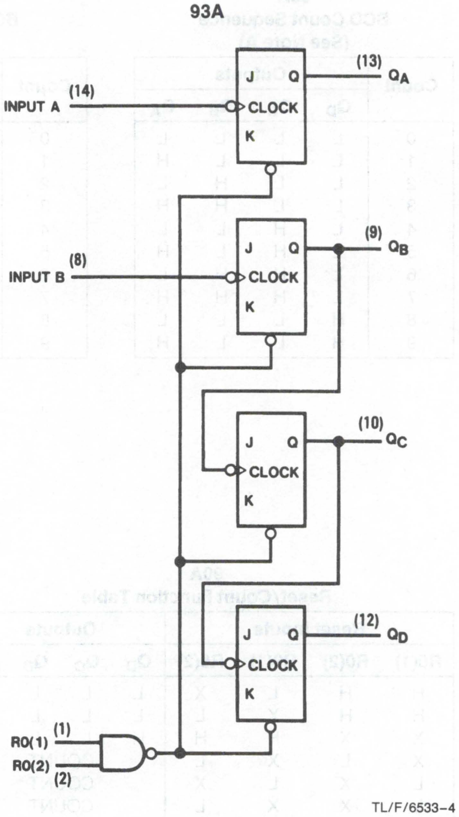
Note C: Output Q_A is connected to input B.

Note D: H = High Level, L = Low Level, X = Don't Care.

Logic Diagrams


90A
R9(1)
(6)
R9(2)
(7)
INPUT A
(14)
INPUT B
(1)
J
Q
CLOCK
K
(12)
QA
(9)
QB
(8)
QC
(11)
QD
Q̄
R0(1)
(2)
R0(2)
(3)

TL/F/6533-3


93A
INPUT A
(14)
INPUT B
(8)
J
Q
CLOCK
K
(13)
QA
(9)
QB
(10)
QC
(12)
QD
R0(1)
(1)
R0(2)
(2)

TL/F/6533-4

The J and K inputs shown without connection are for reference only and are functionally at a high level.

National Semiconductor

5495A/DM7495
4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation.

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source.

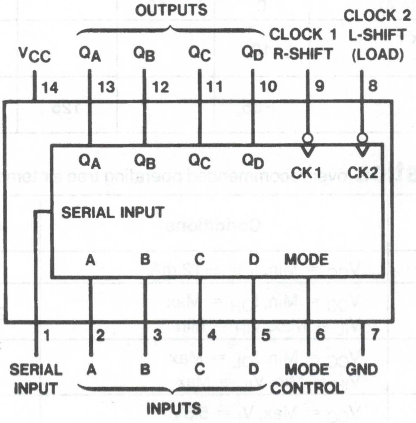
Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

Features

- Typical maximum clock frequency 36 MHz
- Typical power dissipation 250 mW

Connection Diagram

Dual-In-Line Package



TL/F/6534-1

Order Number 5495ADMQB, 5495AFMQB or DM7495N
See NS Package Number J14A, N14A or W14B

4

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54A	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		5495A			DM7495			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 4)		0	25		0		25	MHz
t_W	Clock Pulse Width (Note 4)		15	11		15			ns
t_{SU}	Data Setup Time (Note 4)		20	10		20	10		ns
t_{EN}	Time to Enable Clock (Note 4)	Clock 1	20			20			ns
		Clock 2	15			15			
t_H	Data Hold Time (Note 4)		0	−10		0	−10		ns
t_{IN}	Time to Inhibit Clock 1 or Clock 2 (Note 4)		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Mode			80	μA
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Mode			−3.2	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−18		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			50	75	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded: Mode Control at 4.5V: and a momentary 3V, then ground, applied to both clock inputs.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15\text{ pF}$		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		35	ns

Function Table

Inputs								Outputs			
Mode Control	Clocks		Serial	Parallel				Q_A	Q_B	Q_C	Q_D
	2(L)	1(R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, Q_D to C. Serial data is entered at input D.

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care (Any input, including transitions)

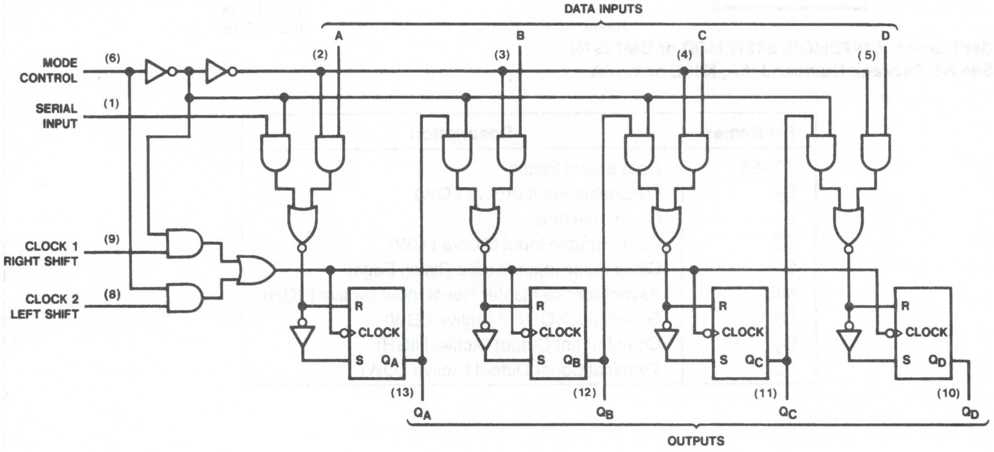
↓ = Transition from high to low level, ↑ = Transition from low to high level

a, b, c, d = The level of steady, state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, Q_D, respectively, before the most recent ↓ transition of the clock.

Logic Diagram



TL/F/6534–2

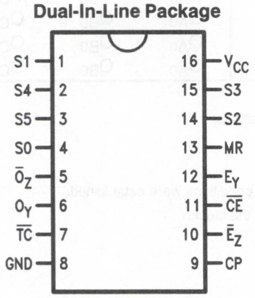
National Semiconductor

5497/DM7497
Synchronous Modulo-64 Bit Rate Multiplier

General Description

The '97 contains a synchronous 6-stage binary counter and six decoding gates that serve to gate the clock through to the output at a sub-multiple of the input frequency. The output pulse rate, relative to the clock frequency, is determined by signals applied to the Select (S0–S5) inputs. Both true and complement outputs are available, along with an enable input for each. A Count Enable input and a Terminal Count output are provided for cascading two or more packages. An asynchronous Master Reset input prevents counting and resets the counter.

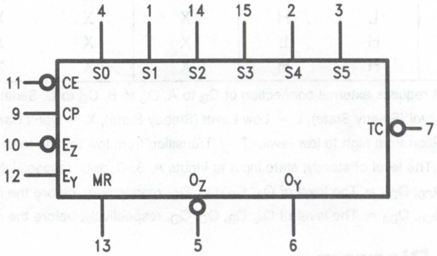
Connection Diagram


Dual-In-Line Package
S1 1
S4 2
S5 3
S0 4
$\overline{O}_Z$ 5
O_Y 6
$\overline{TC}$ 7
GND 8
16 V_{CC}
15 S3
14 S2
13 MR
12 E_Y
11 $\overline{CE}$
10 $\overline{E}_Z$
9 CP

TL/F/9780-1

Order Number 5497DMQB, 5497FMQB or DM7497N
See NS Package Number J16A, N16E or W16A

Logic Symbol


4
1
14
15
2
3
S0
S1
S2
S3
S4
S5
11 CE
9 CP
10 E_Z
12 E_Y
MR
O_Z
O_Y
TC 7
13
5
6

TL/F/9780-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
S0–S5	Rate Select Inputs
$\overline{E}_Z$	$\overline{O}_Z$ Enable Input (Active LOW)
E_Y	O_Y Enable Input
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
MR	Asynchronous Master Reset Input (Active HIGH)
$\overline{O}_Z$	Gated Clock Output (Active LOW)
O_y	Complement Output (Active HIGH)
$\overline{TC}$	Terminal Count Output (Active LOW)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for acutual device operation.*

Recommended Operating Conditions

Symbol	Parameter	5497			DM7497			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
$t_s(L)$	Setup Time LOW, $\overline{CE}$ to CP Rising	25			25			ns
$t_h(H)$	Hold Time HIGH, $\overline{CE}$ to CP Rising	0			0			ns
$t_h(L)$	Hold Time LOW, $\overline{CE}$ to CP Falling	0			0			ns
$t_w(H)$	CP Pulse Width HIGH	20			20			ns
$t_w(L)$	CP Pulse Width LOW	20						ns
$t_w(H)$	MR Pulse Width HIGH	15			15			ns

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

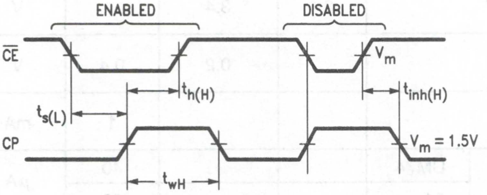
Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V Clock Inputs	DM74			40	μA
			54			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V Clock Inputs	DM74			−1.6	mA
			54			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current With Outputs High	V_{CC} = Max				120	mA

Switching Characteristics

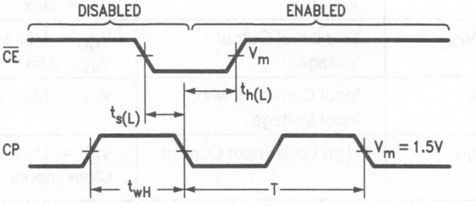
$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	5497 $C_L = 15$ pF $R_L = 400\Omega$ Min	5497 $C_L = 15$ pF $R_L = 400\Omega$ Max	DM7497 $C_L = 15$ pF $R_L = 400\Omega$ Min	DM7497 $C_L = 15$ pF $R_L = 400\Omega$ Max	Units
f_{max}	Maximum Clock Frequency	25		25		MHz
t_{PLH}	Propagation Delay		18		18	ns
t_{PHL}	$\overline{E}_Z$ to $\overline{O}_Z$		23		23	
t_{PLH}	Propagation Delay		30		30	ns
t_{PHL}	$\overline{E}_Z$ to O_Y		33		33	
t_{PLH}	Propagation Delay		14		14	ns
t_{PHL}	E_Y to O_Y		10		10	
t_{PLH}	Propagation Delay		23		23	ns
t_{PHL}	S_n to O_Y		23		23	
t_{PLH}	Propagation Delay		14		14	ns
t_{PHL}	S_n to $\overline{O}_Z$		14		14	
t_{PLH}	Propagation Delay		39		39	ns
t_{PHL}	CP to O_Y		30		30	
t_{PLH}	Propagation Delay		18		18	ns
t_{PHL}	CP to O_Z		26		26	
t_{PLH}	Propagation Delay		35		30	ns
t_{PHL}	CP to $\overline{TC}$		33		33	
t_{PLH}	Propagation Delay		25		20	ns
t_{PHL}	$\overline{CE}$ to $\overline{TC}$		21		21	
t_{PLH}	Propagation Delay MR to O_Y		43		36	ns
t_{PHL}	Propagation Delay MR to $\overline{O}_Z$		34		23	ns

Timing Diagrams


ENABLED
DISABLED
$\overline{CE}$
V_m
$t_{h(H)}$
$t_{inh(H)}$
$t_{s(L)}$
CP
$V_m = 1.5V$
t_{wH}

TL/F/9780-5


DISABLED
ENABLED
$\overline{CE}$
V_m
$t_{h(L)}$
$t_{s(L)}$
CP
$V_m = 1.5V$
t_{wH}
T

TL/F/9780-6

Functional Description

The '97 contains six JK flip-flops connected as a synchronous modulo-64 binary counter. A LOW signal on the Count Enable ($\overline{CE}$) input permits counting, with all state changes initiated simultaneously by the rising edge of the clock. When the count reaches maximum (63), with all Qs HIGH, the Terminal Count ($\overline{TC}$) output will be LOW if $\overline{CE}$ is LOW. A HIGH signal on Master Reset (MR) resets the flip-flops and prevents counting, although output pulses can still occur if the clock is running, $\overline{E}_Z$ is LOW and S5 is HIGH.

The flip-flop outputs are decoded by a 6-wide AND-OR-INVERT gate. Each AND gate also contains the buffered and inverted CP and Z-enable ($\overline{E}_Z$) functions, as well as one of the Select (S0–S5) inputs. The Z output, $\overline{O}_Z$ is normally HIGH and goes LOW when CP and $\overline{E}_Z$ are LOW and any of the AND gates has its other inputs HIGH. The AND gates are enabled by the counter at different times and different rates relative to the clock. For example, the gate to which S5 is connected is enabled during every other clock period, assuming S5 is HIGH. Thus, during one complete cycle of the counter (64 clocks) the S5 gate is enabled 32 times and can therefore gate 32 clocks per cycle to the output. The S4 gate is enabled 16 times per cycle, the S3 gate 8 times per cycle, etc. The output pulse rate thus depends on the clock rate and which of the S0–S5 inputs is HIGH.

$$f_{out} = \frac{m}{64} \bullet f_{in}$$

Where: $m = S5 \bullet 2^5 + S4 \bullet 2^4 + S3 \bullet 2_3 + S2 \bullet 2^2 + S1 \bullet 2^1 + S0 \bullet 2^0$

Thus by appropriate choice of signals applied to the S0–S5 inputs, the output pulse rate can range from $1/64$ to $63/64$ of the clock rate, as suggested in Rate Select Table. There is no output pulse when the counter is in the "all ones" condition. When m is 1, 2, 4, 8, 16 or 32, the output pulses are evenly spaced, assuming that the clock frequency is constant. For any other value of m the output pulses are not evenly spaced, since the pulse train is formed by interleaving pulses passed by two or more of the AND gates. The Pulse Pattern Table indicates the output pattern for several values of m. In each row, a one means that the $\overline{O}_Z$ output will be HIGH during that entire clock period, while a zero means that $\overline{O}_Z$ will be LOW when the clock is LOW in that period. The first column in the output field coincides with the "all zeroes" condition of the counter, while the last column represents the "all ones" condition. The pulse pattern for any particular value of m can be deduced by factoring it into the sum of appropriate powers of two (e.g. 19 = 16 + 2 + 1) and combining the pulses (i.e., the zeroes) shown for each for the relevant powers of two (e.g. for m = 16, 2 and 1).

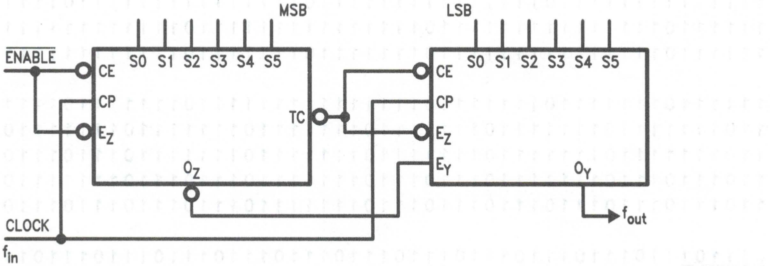
The Y output O_Y is the complement of $\overline{O}_Z$ and is thus normally LOW. A LOW signal on the Y-enable input, E_Y, disables O_Y. To expand the multiplier to 12-bit rate select, two packages can be cascaded as shown in *Figure A*. Both circuits operate from the basic clock, with the $\overline{TC}$ output of the first acting to enable both counting and the output pulses of the second package. Thus the second counter advances at only $1/64$ the rate of the first and a full cycle of the two counters combined requires 4096 clocks. Each rate select input of the first package has 64 times the weight of its counterpart in the second package.

$$f_{out} = \frac{m_1 + m_2}{64 \bullet 64} \bullet f_{in}$$

Where: $m_1 = S5 \bullet 2^{11} + S4 \bullet 2^{10} + S3 \bullet 2^9 + S2 \bullet 2^8 + S1 \bullet 2^7 + S0 \bullet 2^6$ (first package)

$m_2 = S5 \bullet 2^5 + S4 \bullet 2^4 + S3 \bullet 2^3 + S2 \bullet 2_2 + S1 \bullet 2^1 + S0 \bullet 2^0$ (second package)

Combined output pulses are obtained in *Figure A* by letting the Z output of the first circuit act as the Y-enable function for the second, with the interleaved pulses obtained from the Y output of the second package being opposite in phase to the clock.



TL/F/9780-3

FIGURE A. Cascading for 12-Bit Rate Select

Functional Description (Continued)

Mode and Rate Select Table (Note 1)

Inputs									Clock Pulses	Outputs				Notes
MR	CE	$\overline{E}_Z$	S5	S4	S3	S 2	S1	S0		E_Y	O_Y	$\overline{O}_Z$	$\overline{TC}$	
H	X	H	X	X	X	X	X	X	X	H	L	H	H	2
L	L	L	L	L	L	L	L	L	64	H	L	H	1	3
L	L	L	L	L	L	L	L	H	64	H	1	1	1	3
L	L	L	L	L	L	L	H	L	64	H	2	2	1	3
L	L	L	L	L	L	H	L	L	64	H	4	4	1	3
L	L	L	L	L	H	L	L	L	64	H	8	8	1	3
L	L	L	L	H	L	L	L	L	64	H	16	16	1	3
L	L	L	H	L	L	L	L	L	64	H	32	32	1	3
L	L	L	H	H	H	H	H	H	64	H	63	62	1	3
L	L	L	H	H	H	H	H	H	64	L	H	63	1	4
L	L	L	H	L	L	L	L	L	64	H	40	40	1	5

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Note 1: Numerals indicate number of pulses per cycle.

Note 2: This is a simplified illustration of the clear function. CP and $\overline{E}_Z$ also affect the logic level of O_Y and $\overline{O}_Z$. A LOW signal on E_Y will cause O_Y to remain HIGH.

Note 3: Each rate illustrated assumes S0–S5 are constant throughout the cycle; however, these illustrations in no way prohibit variable-rate operation.

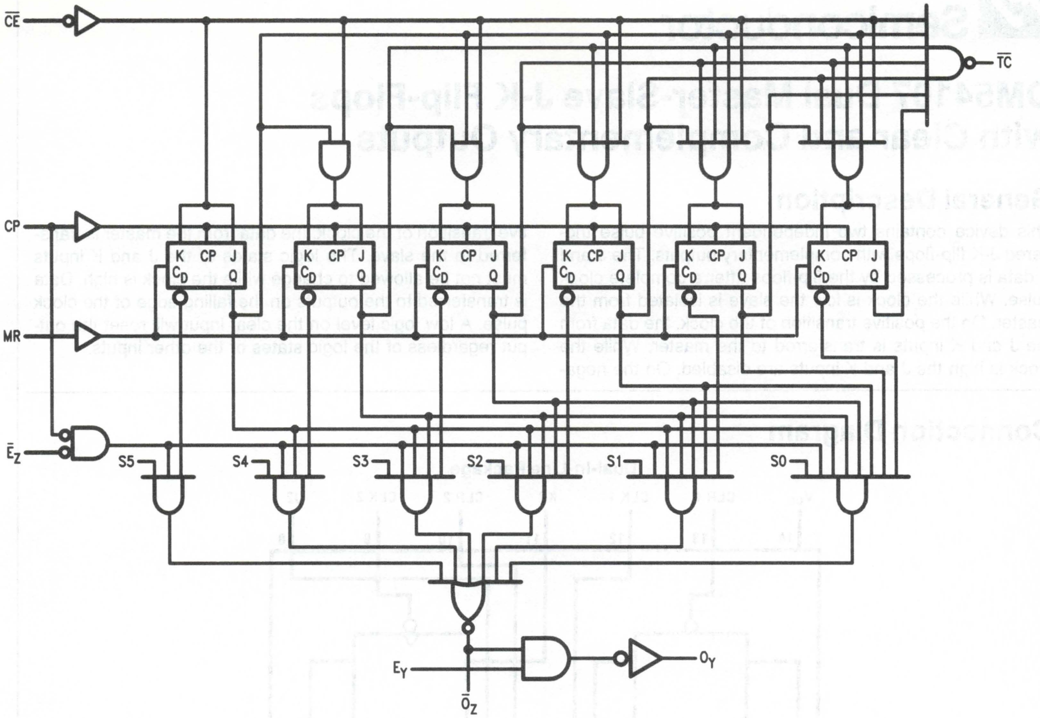
Note 4: E_Y is used to inhibit output Y.

Note 5: $f_{out} = m \bullet \frac{f_{in}}{64} = \frac{(32 + 8)\, f_{in}}{64} = \frac{40\, f_{in}}{64} = 0.625\, f_{in}$

Pulse Pattern Table

m	Output Pulse Pattern at $\overline{O}_Z$
1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
2	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
3	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
4	1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1
5	1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1
6	1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1
8	1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1
10	1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 1
12	1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 1
14	1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 1
16	1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1
20	1 0 1 1 1 0 1 0 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 0 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 0 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 1 1
24	1 0 1 0 1 0 1 1 1 0 1 0 1 0 1 1 1 0 1 0 1 0 1 1 1 0 1 0 1 0 1 1 1 0 1 0 1 0 1 1 1 1 1 0 1 0 1 1 1 0 1 0 1 0 1 1 1 0 1 0 1 0 1 1
28	1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1
32	0 1 0 1 0 1 . . . . . .0 1 0 1

Logic Diagram


CE
CP
MR
EZ
TC
K CP J
CD Q
S5
S4
S3
S2
S1
S0
EY
OZ
OY

TL/F/9780-4

National Semiconductor

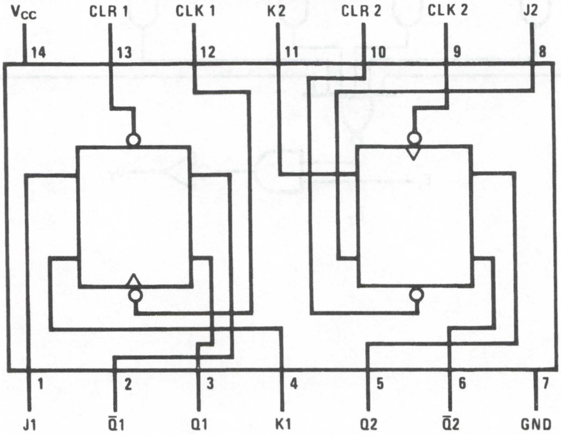
DM54107 Dual Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic states of the J and K inputs must not be allowed to change while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the clear input will reset the output regardless of the logic states of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6536-1

Order Number DM54107J
See NS Package Number J14A

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\overline{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	Toggle	

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_0 = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete positive clock pulse.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54107			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				16	mA
f_{CLK}	Clock Frequency (Note 5)		0	20	15	MHz
t_W	Pulse Width (Note 5)	Clock High	20			ns
		Clock Low	47			
		Clear Low	25			
t_{SU}	Input Setup Time (Notes 1 & 5)		0↑			ns
t_H	Input Hold Time (Notes 1 & 5)		0↓			ns
T_A	Free Air Operating Temperature		−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			40	μA
			Clock			80	
			Clear			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	J, K			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)		−20		−55	mA
I_{CC}	Supply Current	V_{CC} = Max, (Note 4)			18	34	mA

Note 1: The symbols (↑, ↓) indicate the edge of the clock pulse is used for reference: (↑) for rising edge, (↓) for falling edge.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15$ pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25	ns

National Semiconductor

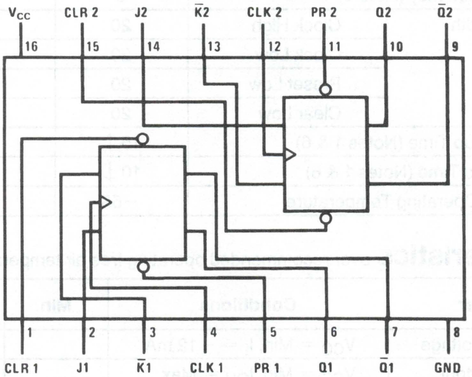
DM54109 Dual Positive-Edge-Triggered J-$\overline{K}$ Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered J-$\overline{K}$ flip-flops with complementary outputs. The J and $\overline{K}$ data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the J and $\overline{K}$ inputs may be changed while the clock is high or low as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6537-1

Order Number DM54109J or DM54109W
See NS Package Number J16A or W16A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level

L = Low Logic Level

↑ = Rising Edge of Pulse.

* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Q_0 = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each active transition of the clock pulse.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54109 Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−1.2	mA
I_{OL}	Low Level Output Current				16	mA
f_{CLK}	Clock Frequency (Note 6)		0		30	MHz
t_W	Pulse Width (Note 6)	Clock High	20			ns
		Clock Low	20			
		Preset Low	20			
		Clear Low	20			
t_{SU}	Input Setup Time (Notes 1 & 6)		15↑			ns
t_H	Input Hold Time (Notes 1 & 6)		10↓			ns
T_A	Free Air Operating Temperature		−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J,$\overline{K}$			40	μA
			Preset			80	
			Clock			80	
			Clear			160	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V (Note 5)	J, $\overline{K}$			−1.6	mA
			Preset			−3.2	
			Clock			−3.2	
			Clear			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)		−30		−85	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			20	30	mA

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input grounded.

Note 5: Clear is tested with preset high and preset is tested with clear high.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15$ pF Min	$R_L = 400\Omega$ $C_L = 15$ pF Max	Units
f_{MAX}	Maximum Clock Frequency		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		29	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		28	ns

National Semiconductor

54121/DM54121/DM74121 One-Shot with Clear and Complementary Outputs

General Description

The DM54/74121 is a monostable multivibrator featuring both positive and negative edge triggering with complementary outputs. An internal 2kΩ timing resistor is provided for design convenience minimizing component count and layout problems. This device can be used with a single external capacitor. Inputs (A) are active-low trigger transition inputs and input (B) is an active-high transition Schmitt-trigger input that allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second. A high immunity to V_{CC} noise of typically 1.5V is also provided by internal circuitry at the input stage.

To obtain optimum and trouble free operation please read operating rules and NSC one-shot application notes carefully and observe recommendations.

Features

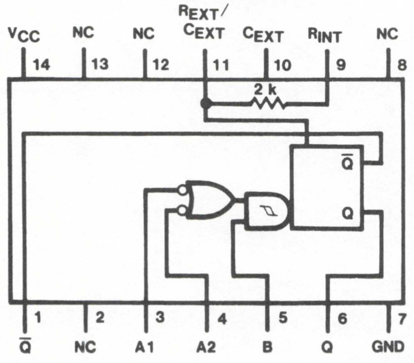
- Triggered from active-high transition or active-low transition inputs
- Variable pulse width from 30 ns to 28 seconds
- Jitter free Schmitt-trigger input
- Excellent noise immunity typically 1.2V
- Stable pulse width up to 90% duty cycle
- TTL, DTL compatible
- Compensated for V_{CC} and temperature variations
- Input clamp diodes
- Alternate Military/Aerospace device (54121) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Functional Description

The basic output pulse width is determined by selection of an internal resistor R_{INT} or an external resistor (R_X) and capacitor (C_X). Once triggered the output pulse width is independent of further transitions of the inputs and is a function of the timing components. Pulse width can vary from a few nano-seconds to 28 seconds by choosing appropriate R_X and C_X combinations. There are three trigger inputs from the device, two negative edge-triggering (A) inputs, one positive edge Schmitt-triggering (B) input.

Connection Diagram

Dual-In-Line Package



TL/F/6538-1

Order Number 54121DMQB, 54121FMQB, DM54121J, DM54121W or DM74121N
See NS Package Number J14A, N14A or W14B

Function Table

Inputs			Outputs	
A1	**A2**	**B**	**Q**	**Q̄**
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⊓	⊔
↓	H	H	⊓	⊔
↓	↓	H	⊓	⊔
L	X	↑	⊓	⊔
X	L	↑	⊓	⊔

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⊓ = A Positive Pulse
⊔ = A Negative Pulse

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54121			DM74121			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage at the A Input (V_{CC} = Min)			1.4	2		1.4	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the A Input (V_{CC} = Min)		0.8	1.4		0.8	1.4		V
V_{T+}	Positive-Going Input Threshold Voltage at the B Input (V_{CC} = Min)			1.5	2		1.5	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the B Input (V_{CC} = Min)		0.8	1.3		0.8	1.3		V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
t_W	Input Pulse Width (Note 1)		40			40			ns
dV/dt	Rate of Rise or Fall of Schmidt Input (B) (Note 1)				1			1	V/s
dV/dt	Rate of Rise or Fall of Logic Input (A) (Note 1)				1			1	V/μs
R_{EXT}	External Timing Resistor (Note 1)		1.4		30	1.4		40	kΩ
C_{EXT}	External Timing Capacitance (Note 1)		0		1000	0		1000	μF
DC	Duty Cycle (Note 1)	R_T = 2 kΩ			67			67	%
		R_T = R_{EXT} (Max)			90			90	
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	A1, A2			40	μA
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	A1, A2			−1.6	mA
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max	Quiescent		13	25	mA
			Triggered		23	40	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Outout Load)

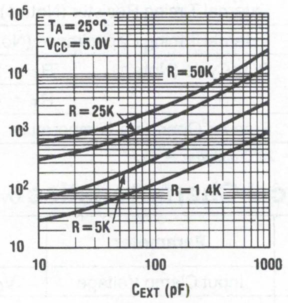
Symbol	Parameter	From (Input) To (Output)	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	A1, A2 to Q	$C_{EXT} = 80$ pF R_{INT} to V_{CC} $C_L = 15$ pF $R_L = 400\Omega$		70	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q			55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A1, A2 to $\overline{Q}$			80	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to $\overline{Q}$			65	ns
$t_{W(OUT)}$	Output Pulse Width Using the Internal Timing Resistor	A1, A2 or B to Q, $\overline{Q}$	$C_{EXT} = 80$ pF R_{INT} to V_{CC} $R_L = 400\Omega$ $C_L = 15$ pF	70	150	ns
$t_{W(OUT)}$	Output Pulse Width Using Zero Timing Capacitance	A1, A2 to Q, $\overline{Q}$	$C_{EXT} = 0$ pF R_{INT} to V_{CC} $R_L = 400\Omega$ $C_L = 15$ pF		50	ns
$t_{W(OUT)}$	Output Pulse Width Using External Timing Resistor	A1, A2 to Q, $\overline{Q}$	$C_{EXT} = 100$ pF $R_{INT} = 10$ kΩ $R_L = 400\Omega$ $C_L = 15$ pF	600	800	ns
		A1, A2 to Q, $\overline{Q}$	$C_{EXT} = 1\ \mu$F $R_{INT} = 10$ kΩ $R_L = 400\Omega$ $C_L = 15$ pF	6	8	ms

Operating Rules

1. To use the internal 2 kΩ timing resistor, connect the R_{INT} pin to V_{CC}.
2. An external resistor (R_X) or the internal resistor (2 kΩ) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants use high-quality mica, glass, polypropylene, polycarbonate, or polystyrene capacitors. For large time constants use solid tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
3. The pulse width is essentially determined by external timing components R_X and C_X. For $C_X < 1000$ pF see *Figure 1* design curves on T_W as function of timing components value. For $C_X > 1000$ pF the output is defined as:

   $t_W = K\, R_X\, C_X$

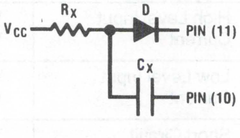
   where [R_X is in Kilo-ohm]
   [C_X is in pico Farad]
   [T_W is in nano second]
   [$K \approx 0.7$]



TL/F/6538–2

FIGURE 1

4. If C_X is an electrolytic capacitor a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current *(Figure 2)*.

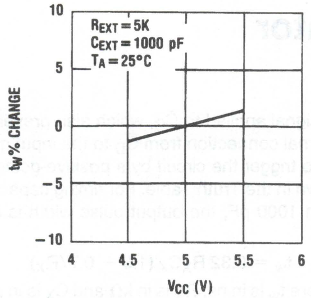


TL/F/6538–3

FIGURE 2

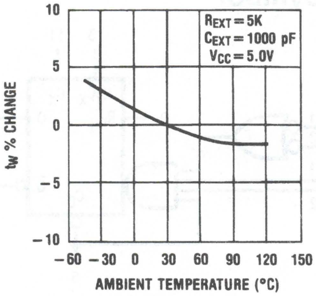
Operating Rules (Continued)

5. Output pulse width versus V_{CC} and operation temperatures: *Figure 3* depicts the relationship between pulse width variation versus V_{CC}. *Figure 4* depicts pulse width variation versus ambient temperature.



TL/F/6538–4

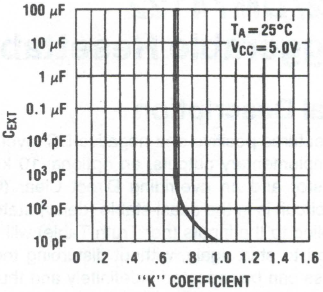
FIGURE 3



TL/F/6538–5

FIGURE 4

6. The "K" coefficient is not a constant, but varies as a function of the timing capacitor C_X. *Figure 5* details this characteristic.



TL/F/6538–6

FIGURE 5

7. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I × R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (10) and (11) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.

8. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 μF to 0.10 μF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC}-pin as space permits.

For further detailed device characteristics and output performance please refer to the NSC one-shot application note, AN-366.

National Semiconductor

54122/DM74122
Retriggerable Resettable Multivibrator

General Description

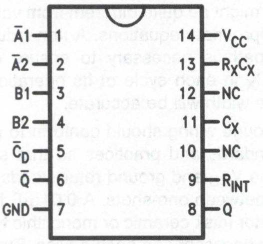
The '122 features positive and negative DC level triggering inputs, complementary outputs, an optional 10 kΩ internal timing resistor and an overriding Direct Clear ($\overline{C}_D$) input. When the circuit is in the quasi-stable (delay) state, another trigger applied to the inputs (per Truth Table) will cause the delay period to start again, without disturbing the outputs. This process can be repeated indefinitely and thus the output pulse period (Q HIGH, $\overline{Q}$ LOW) can be made as long as desired. Alternatively, a delay period can be terminated by a LOW signal applied to $\overline{C}_D$, which also prevents triggering. An internal connection from $\overline{C}_D$ to the input gate makes it possible to trigger the circuit by a positive-going signal on $\overline{C}_D$, as shown in the Truth Table. For timing capacitor values greater than 1000 pF, the output pulse width is defined as follows:

$$t_W = 0.32\, R_X C_X\, (1.0 + 0.7/R_X)$$

Where t_W is in ns, R_X is in kΩ and C_X is in pF.

Connection Diagram

Dual-In-Line Package

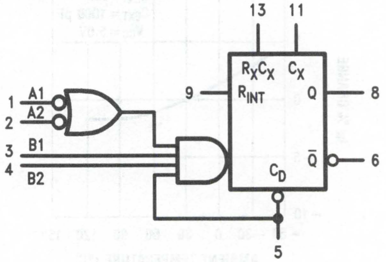


$\overline{A1}$ 1
$\overline{A2}$ 2
B1 3
B2 4
$\overline{C}_D$ 5
$\overline{Q}$ 6
GND 7
14 V_{CC}
13 R_XC_X
12 NC
11 C_X
10 NC
9 R_{INT}
8 Q

TL/F/10212-1

Order Number 54122DMQB, 54122FMQB or DM74122N
See NS Package Number J14A, N14A or W14B

Logic Symbol



13
11
R_XC_X
C_X
9
R_{INT}
Q
8
1
$\overline{A1}$
2
$\overline{A2}$
3
B1
4
B2
$\overline{Q}$
6
C_D
5

TL/F/10212-2

V_{CC} = Pin 14
GND = Pin 7
NC = Pins 10 and 12

Pin Names	Description
$\overline{A}_1, \overline{A}_2$	Trigger Inputs (Active Falling Edge)
B_1, B_2	Trigger Inputs (Active Rising Edge)
$\overline{C}_D$	Direct Clear Inputs (Active LOW)
$Q, \overline{Q}$	Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54122			DM74122			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	−55		70	°C

Recommended Operating Conditions $V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter		Conditions	DM74		Units
				Min	Max	
t_W	Trigger Pulse Width		Over Operating V_{CC} and Temperature Range	40		ns
R_X	External Timing Resistor	XC		5.0	50	kΩ
		XM		5.0	25	
C_X	External Timing Capacitor			No Restrictions		pF

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = Min				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			40	μA
			Clear			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Inputs			−1.6	mA
			Clear			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−10		−40	mA
I_{CC}	Supply Current	V_{CC} = Max				28	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 3 for waveforms and load configurations)

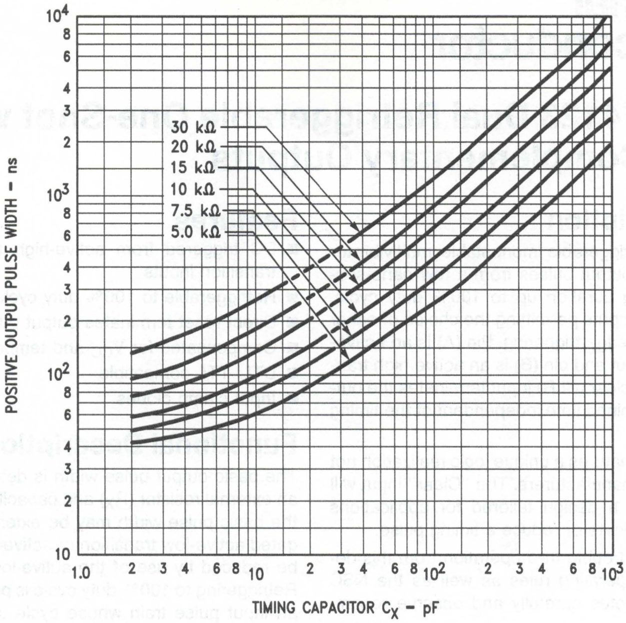
Symbol	Parameter	Conditions	54/74 $C_L = 15$ pF $R_L = 400\Omega$		Units
			Min	Max	
t_{PLH}	Propagation Delay B to Q	$C_X = 0$ pF, $R_X = 5$ kΩ *Figure 3-1, Figure a*		28	ns
t_{PLH}	Propagation Delay $\overline{A}$ to Q			33	ns
t_{PLH}	Propagation Delay B to $\overline{Q}$			36	ns
t_{PHL}	Propagation Delay $\overline{A}$ to $\overline{Q}$			40	ns
t_{PLH}	Propagation Delay $\overline{C}_D$ to $\overline{Q}$	$C_X = 0$ pF, $R_X = 5$ kΩ *Figure 3-1, Figure 3-10*		40	ns
t_{PHL}	Propagation Delay $\overline{C}_D$ to Q			27	ns
$t_{w(out)}$	Pulse Width at Q with Zero Timing Capacitor	$C_X = 0$ pF, $R_X = 5$ kΩ *Figure 3-1, Figure a*		65	ns
$t_{w(out)}$	Pulse Width with External Timing Components	$C_X = 1000$ pF, $R_X = 10$ kΩ *Figure 3-1, Figure a*	3.08	3.76	µs

Triggering Truth Table

Inputs*					Response
$\overline{C}_D$	$\overline{A}_1$	$\overline{A}_2$	B_1	B_2	
L	X	X	X	X	No Trigger
X	↓	L	X	X	No Trigger
X	↓	X	L	X	No Trigger
H	↓	H	H	H	Trigger
X	X	X	↑	L	No Trigger
X	H	H	↑	X	No Trigger
H	L	X	↑	H	Trigger
↑	L	X	H	H	Trigger

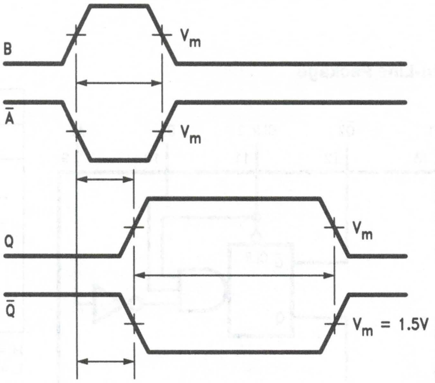
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
*Input pins 1 and 2 are logically interchangeable, as are input pins 3 and 4.

Pulse Width vs R_X and C_X



TL/F/10212-3

Timing Capacitor C_X–pF



B
V_m
$\overline{A}$
V_m
Q
V_m
$\overline{Q}$
$V_m = 1.5V$

TL/F/10212-4

FIGURE A

National Semiconductor

54123/DM74123 Dual Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The '123 is a dual retriggerable monostable multivibrator capable of generating output pulses from a few nano-seconds to extremely long duration up to 100% duty cycle. Each device has three inputs permitting the choice of either leading-edge or trailing edge triggering. Pin (A) is an active-low transition trigger input and pin (B) is an active-high transition trigger input. The clear (CLR) input terminates the output pulse at a predetermined time independent of the timing components.

National's '123 device features a unique logic realization not implemented by other manufacturers. The "Clear" input will not trigger the device, a design tailored for applications where it shall only terminate or reduce a timing pulse.

To obtain the best and trouble free operation from this device please read the operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

Features

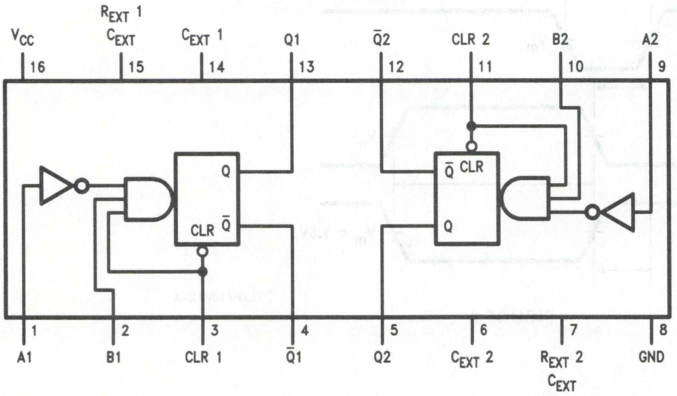
- DC triggered from active-high transition or active-low transition inputs
- Retriggerable to 100% duty cycle
- Direct reset terminates output pulse
- Compensated for V_{CC} and temperature variations
- DTL, TTL compatible
- Input clamp diodes

Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width may be extended by retriggering the gated active-low transition or active-high transition inputs or be reduced by use of the active-low transition clear input. Retriggering to 100% duty cycle is possible by application of an input pulse train whose cycle time is shorter than the output cycle time such that a continuous "HIGH" logic state is maintained at the "Q" output.

Connection Diagram

Dual-In-Line Package



TL/F/6539-1

Order Number 54123DMQB, 54123FMQB or DM74123N
See NS Package Number J16A, N16A or W16A

Triggering Truth Table

Inputs			Response
A	B	CLR	
X	X	L	No Trigger
↓	L	X	No Trigger
↓	H	H	Trigger
H	↑	X	No Trigger
L	↑	H	Trigger
L	H	↑	Trigger

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		54123			DM74123			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
t_W	Pulse Width (Note 5)	A or B High				40			ns
		A or B Low				40			
		Clear Low				40			
T_{WQ} (Min)	Minimum Width of Pulse at Q (Note 5)	A or B			80			65	ns
R_{EXT}	External Timing Resistor					5		50	kΩ
C_{EXT}	External Timing Capacitance						No Restriction		μF
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal (Note 5)							50	pF
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	54	2.4	3.4		V
			DM74	2.5			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Data			40	μA
			Clear			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clear			−3.2	mA
			Data			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54	−10		−40	mA
			DM74	−10		−40	
I_{CC}	Supply Current	V_{CC} = Max (Notes 3 and 4)			46	66	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open,C_{EXT} = 0.02 μF, and R_{EXT} = 25 KΩ.

Note 4: I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{EXT} = 0.02 μF, and R_{EXT} = 25 kΩ.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	54123 C_L = 15 pF, R_L = 400Ω C_{EXT} = 0 pF, R_{EXT} = 5 kΩ		DM74123 C_L = 15 pF, R_L = 400Ω C_{EXT} = 1000 pF, R_{EXT} = 10 KΩ		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	$\overline{A}$ to Q		33		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q		28		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{A}$ to $\overline{Q}$		40		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to $\overline{Q}$		36		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		40		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{\text{Clear}}$ to Q		27		27	ns
$t_{W(out)}$	Output Pulse Width*	A or B to Q	3.08	3.76	3.08	3.76	μs

*C_{ECT} = 1000 pF, R_{EXT} = 10 kΩ

Operating Rules

1. An external resistor (R_X) and external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitors may be used. For large time constants use tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current *(Figure 2)*. However, its use in general is not recommended with retriggerable operation.
3. The output pulse width (T_W) for C_X > 1000 pF is defined as follows:

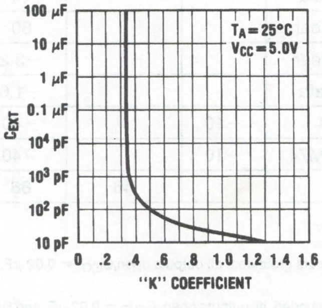
   $T_W = K\ R_X\ C_X\ (1 + 0.7/R_X)$

   where [R_X is in Kilo-ohm]

   [C_X is in pico Farad]

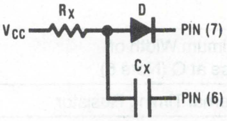
   [T_W is in nano second]

   [$K \approx 0.34$]
4. The multiplicative factor K is plotted as a function of C_X below for design considerations:



TL/F/6539–2

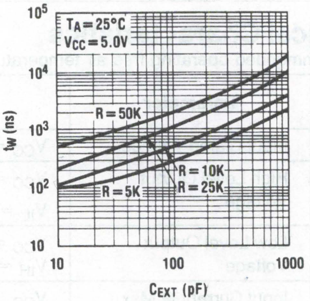
FIGURE 1



TL/F/6539–3

FIGURE 2

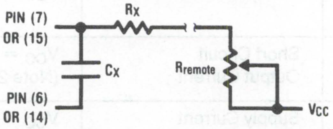
5. For C_X < 1000 pF see *Figure 3* for T_W vs C_X family curves with R_X as a parameter:



TL/F/6539–4

FIGURE 3

6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



TL/F/6539–5

Note: "R_{remote}" should be as close to the one-shot as possible.

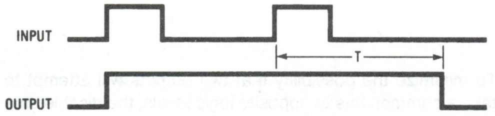
FIGURE 4

Operating Rules (Continued)

7. The retriggerable pulse width is calculated as shown below:

$$T = T_W + t_{PLH} = K \times R_X \times C_X + t_{PLH}$$

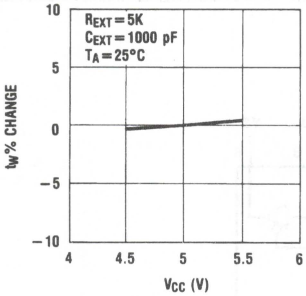
The retriggered pulse width is equal to the pulse width plus a delay time period *(Figure 5).*



TL/F/6539-6

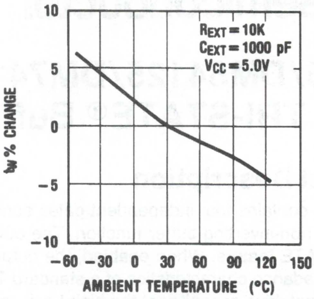
FIGURE 5

8. Output pulse width versus V_{CC} and Temperatures: *Figure 6* depicts the relationship between pulse width variation versus operating V_{CC}. *Figure 7* depicts pulse width variation versus ambient temperatures.



TL/F/6539-7

FIGURE 6



TL/F/6539-8

FIGURE 7

9. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I × R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.

10. The C_{EXT} pins of this device are internally connected to the internal ground. For optimum system performance they should be hard wired to the system's return ground plane.

    * However, it should be noted that although the 74221 series one-shot is pin-for-pin compatiable with the '123 device, its C_{EXT} pin is not an internal connection to ground. Hence, if substitution of an '221 on to an '123 design layout whose C_{EXT} pin is wired to the ground is attempted, the '221 device will not function!

11. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 μF to 0.10 μF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC} pin as space permits.

***For further detailed device characteristics and output performance please refer to the NSC one-shot application note, AN-366.**

National Semiconductor

54125/DM54125/DM74125 Quad TRI-STATE® Buffers

General Description

This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability at the high Logic level to permit the driving of bus lines without external pull-up resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver.

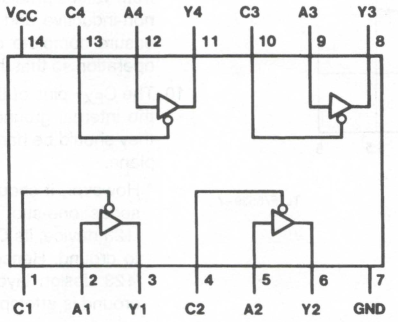
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Features

- Alternate Military/Aerospace device (54125) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6540-1

Order Number 54125DMQB, 54125FMQB, DM54125J, DM54125W or DM74125N
See NS Package Number J14A, N14A or W14B

Function Table

Y = A

Inputs		Output
A	**C**	**Y**
L	L	L
H	L	H
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54125			DM74125			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{IZL}	Off-State Input Current with Low Level Input Voltage Applied	V_{CC} = Max, V_I = 0.4V				−40	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−30		−70	mA
			DM74	−28		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			36	54	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the output control (C) inputs at 4.5V, the data inputs grounded, and the outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 400\Omega$				Units
		$C_L = 5$ pF		$C_L = 50$ pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output				15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				18	ns
t_{PZH}	Output Enable Time to High Level Output				18	ns
t_{PZL}	Output Enable Time to Low Level Output				25	ns
t_{PHZ}	Output Disable Time from High Level Output		8			ns
t_{PLZ}	Output Disable Time from Low Level Output		14			ns

National Semiconductor

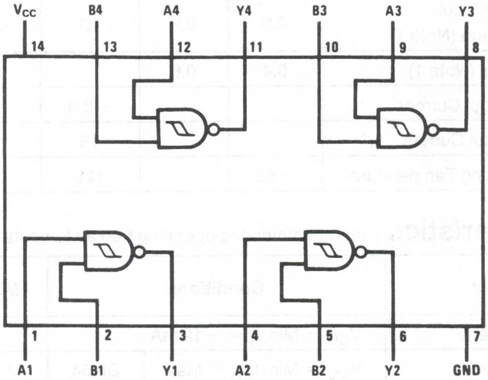
DM54132/DM74132 Quad 2-Input NAND Gates with Schmitt Trigger Inputs

General Description

This device contains four independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter-free output.

Connection Diagram

Dual-In-Line Package



TL/F/6542-1

Order Number DM54132J or DM74132N
See NS Package Number J14A or N14A

Function Table

$Y = \overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54132			DM74132			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.5	1.7	2	1.5	1.7	2	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.6	0.9	1.1	0.6	0.9	1.1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_I = V_{T-}Min	DM54	2.4	3.4		V
			DM74	2.4	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_I = V_{T+}Max			0.2	0.4	V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}			−0.43		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}			−0.56		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.8	−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−18		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			15	24	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			26	40	mA

Note 1: V_{CC} = 5V.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 400\Omega$ $C_L = 15\ pF$		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		22	ns

National Semiconductor

DM54145/DM74145 BCD to Decimal Decoders/Drivers

General Description

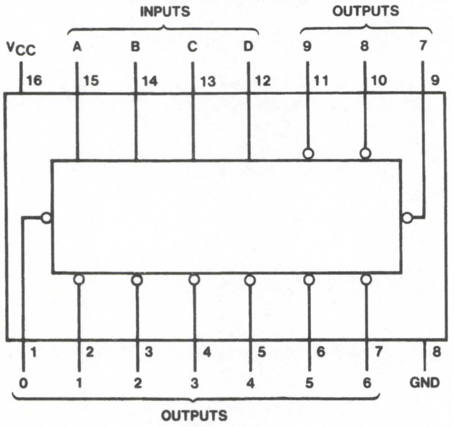
These BCD-to-decimal decoders/drivers consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (10–15) binary input conditions. These decoders feature high-performance, NPN output transistors designed for use as indicator/relay drivers, or as open-collector logic-circuit drivers. The high-breakdown output transistors are compatible for interfacing with most MOS integrated circuits.

Features

- Full decoding of input logic
- 80 mA sink-current capability
- All outputs are off for invalid BCD input conditions

Connection Diagram

Dual-In-Line Package



TL/F/6544–1

Order Number DM54145J, DM54145W or DM74145N
See NS Package Number J16A, N16E or W16A

Function Table

No.	Inputs				Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
I	H	L	H	L	H	H	H	H	H	H	H	H	H	H
N	H	L	H	H	H	H	H	H	H	H	H	H	H	H
V	H	H	L	L	H	H	H	H	H	H	H	H	H	H
A	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
I	H	H	H	H	H	H	H	H	H	H	H	H	H	H
D														

H = High Level (Off), L = Low Level (On)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	$-55°C$ to $+125°C$
DM74	$0°C$ to $+70°C$
Storage Temperature Range	$-65°C$ to $+150°C$

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54145			DM74145			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_{OH} = Max V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
		I_{OL} = 80 mA V_{CC} = Min			0.5	0.9	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)	DM54		43	62	mA
			DM74		43	70	

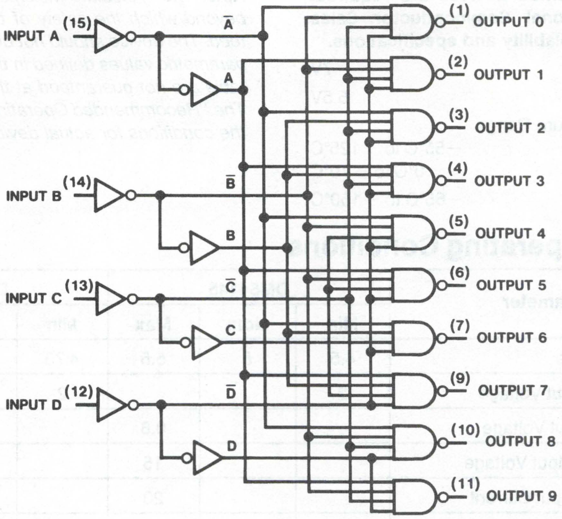
Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 100Ω		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs grounded.

Logic Diagram


INPUT A
(15)
A̅
A
INPUT B
(14)
B̅
B
INPUT C
(13)
C̅
C
INPUT D
(12)
D̅
D
(1) OUTPUT 0
(2) OUTPUT 1
(3) OUTPUT 2
(4) OUTPUT 3
(5) OUTPUT 4
(6) OUTPUT 5
(7) OUTPUT 6
(9) OUTPUT 7
(10) OUTPUT 8
(11) OUTPUT 9

TL/F/6544–2

National Semiconductor

DM54148 Priority Encoder

General Description

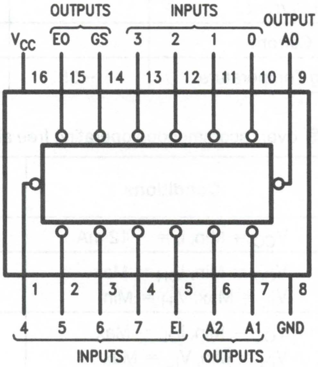
This TTL encoder features priority decoding of the input data to ensure that only the highest-order data line is encoded. The DM54148 encodes eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output E0) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

Features

- Encodes 8 data lines to 3-line binary (octal)
- Applications include:
  - N-bit encoding
  - Code converters and generators

Connection Diagram

Dual-In-Line Package



TL/F/6545-1

Order Number DM54148J or DM54148W
See NS Package Number J16A or W16A

Function Table

DM54148

Inputs									Outputs				
E1	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**A2**	**A1**	**A0**	**GS**	**E0**
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = High Logic Level, L = Low Logic Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54148			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.8	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	0 Input			40	μA
			Others			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	0 Input			−1.6	mA
			Others			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−35		−85	mA
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			40	60	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			35	55	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

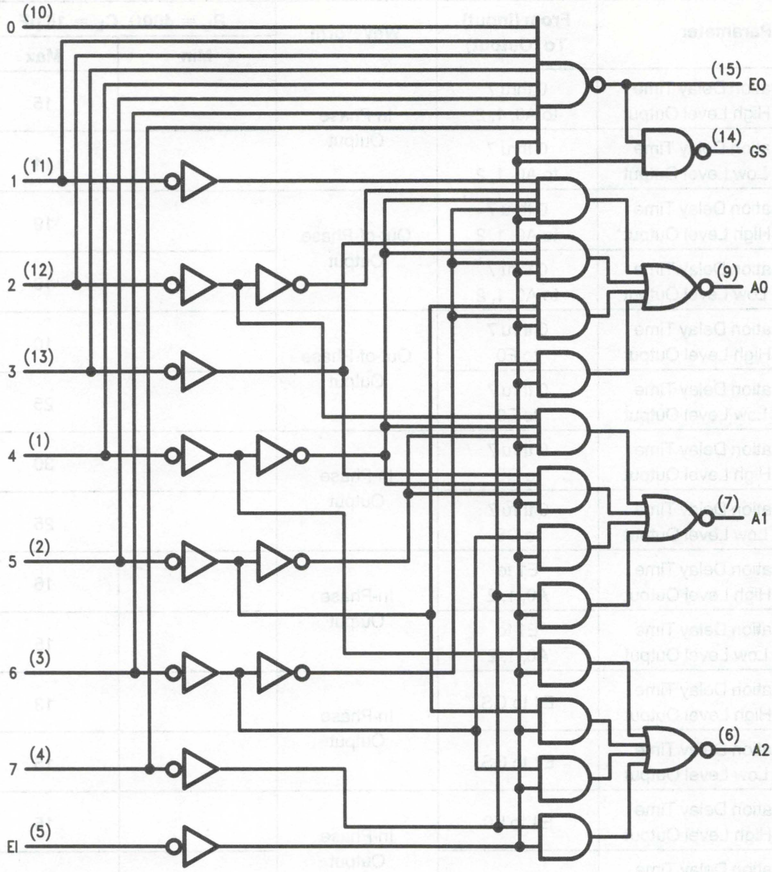
Note 3: I_{CC1} is measured with inputs E1 and 7 grounded, other inputs and outputs open.

Note 4: I_{CC2} is measured with all inputs and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Waveform	$R_L = 400\Omega$, $C_L = 15$ pF		Units
				Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to A0, 1, 2	In-Phase Output		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to A0, 1, 2			14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to A0, 1, 2	Out-of-Phase Output		19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to A0, 1, 2			19	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to E0	Out-of-Phase Output		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to E0			25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to GS	In-Phase Output		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to GS			25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	E1 to A0, 1, 2	In-Phase Output		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	E1 to A0, 1, 2			15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	E1 to GS	In-Phase Output		13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	E1 to GS			15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	E1 to E0	In-Phase Output		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	E1 to E0			30	ns

Logic Diagram


0
(10)
1
(11)
2
(12)
3
(13)
4
(1)
5
(2)
6
(3)
7
(4)
EI
(5)
(15)
EO
(14)
GS
(9)
A0
(7)
A1
(6)
A2

TL/F/6545–2

National Semiconductor

54150/DM54150/DM74150, 54151A/DM54151A/DM74151A Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The 150 selects one-of-sixteen data sources; the 151A selects one-of-eight data sources. The 150 and 151A have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high and the Y output (as applicable) low.

The 151A features complementary W and Y outputs, whereas the 150 has an inverted (W) output only.

The 151A incorporates address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the 151A outputs are enabled (i.e., strobe low).

Features

- 150 selects one-of-sixteen data lines
- 151A selects one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time, data input to W output

150	11 ns
151A	9 ns

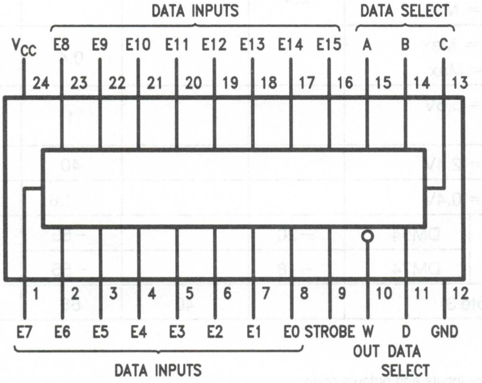
- Typical power dissipation

150	200 mW
151A	135 mW

- Alternate Military/Aerospace device (54150, 54151A) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

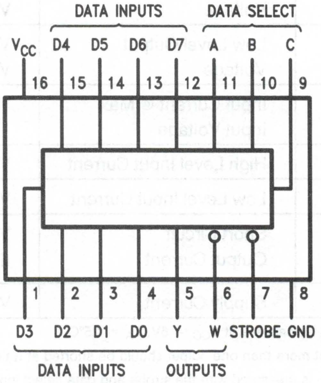
Dual-In-Line Package


DATA INPUTS
DATA SELECT
V_{CC}
E8
E9
E10
E11
E12
E13
E14
E15
A
B
C
24
23
22
21
20
19
18
17
16
15
14
13
1
2
3
4
5
6
7
8
9
10
11
12
E7
E6
E5
E4
E3
E2
E1
E0
STROBE
W
OUT
D
DATA SELECT
GND
DATA INPUTS

TL/F/6546-1

Order Number 54150DQMB, 54150FMQB, DM54150J or DM74150N
See NS Package Number J24A, N24A or W24C

Dual-In-Line Package


DATA INPUTS
DATA SELECT
V_{CC}
D4
D5
D6
D7
A
B
C
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
D3
D2
D1
D0
Y
W
STROBE
GND
DATA INPUTS
OUTPUTS

TL/F/6546-2

Order Number 54151ADMQB, 54151AFMQB, DM54151AJ, DM54151AW or DM74151AN
See NS Package Number J16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54150			DM74150			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'150 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max, (Note 3)			40	68	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the strobe and data select inputs at 4.5V, all other inputs and outputs open.

’150 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to W		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to W		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to W		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to W		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	E0-E15 to W		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	E0-E15 to W		14	ns

Recommended Operating Conditions

Symbol	Parameter	DM54151A			DM74151A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

’151A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max, (Note 3)			27	48	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the strobe and data select inputs at 4.5V, all other inputs and outputs open.

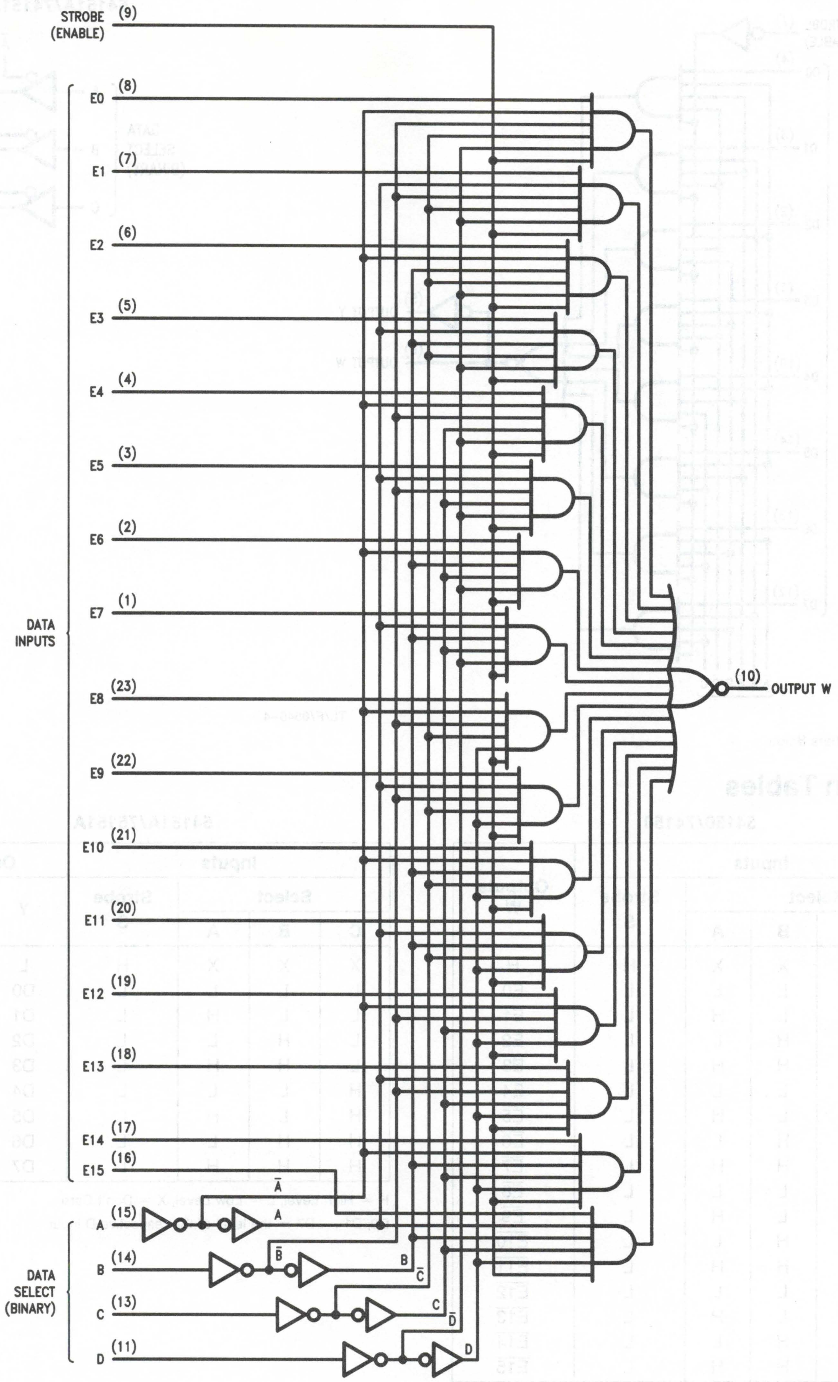
’151A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select (4 Levels) to Y		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select (4 Levels) to Y		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select (3 Levels) to W		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select (3 Levels) to W		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to W		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to W		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D0-D7 to Y		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D0-D7 to Y		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D0-D7 to W		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D0-D7 to W		14	ns

Logic Diagrams

150

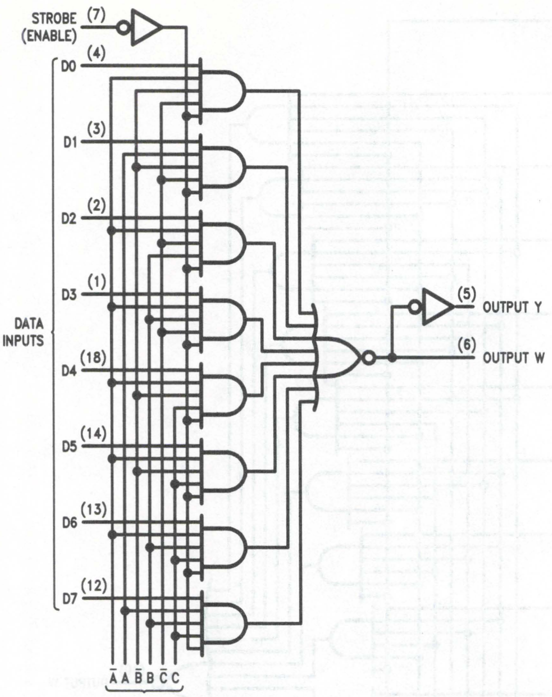


STROBE (ENABLE) (9)
E0 (8)
E1 (7)
E2 (6)
E3 (5)
E4 (4)
E5 (3)
E6 (2)
E7 (1)
E8 (23)
E9 (22)
E10 (21)
E11 (20)
E12 (19)
E13 (18)
E14 (17)
E15 (16)
DATA INPUTS
A (15)
B (14)
C (13)
D (11)
DATA SELECT (BINARY)
$\bar{A}$
A
$\bar{B}$
B
$\bar{C}$
C
$\bar{D}$
D
(10) OUTPUT W

TL/F/6546–3

Logic Diagrams

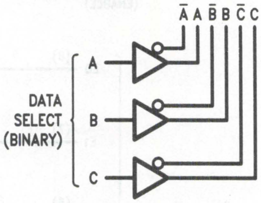
151A


STROBE (ENABLE)
(7)
D0
(4)
D1
(3)
D2
(2)
D3
(1)
DATA INPUTS
D4
(18)
D5
(14)
D6
(13)
D7
(12)
(5)
OUTPUT Y
(6)
OUTPUT W
Ā A B̄ B C̄ C

TL/F/6546-4

See Address Buffers Below

Address Buffers for 54151A/74151A


Ā A B̄ B C̄ C
A
DATA SELECT (BINARY)
B
C

TL/F/6546-5

Function Tables

54150/74150

Inputs					Outputs W
Select				Strobe S	
D	C	B	A		
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

H = High Level, L = Low Level, X = Don't Care

$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input

54151A/75151A

Inputs				Outputs	
Select			Strobe S	Y	W
C	B	A			
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care

D0, D1 . . . D7 = the level of the respective D input

National Semiconductor

54153/DM54153/DM74153 Dual 4-Line to 1-Line Data Selectors/Multiplexers

General Description

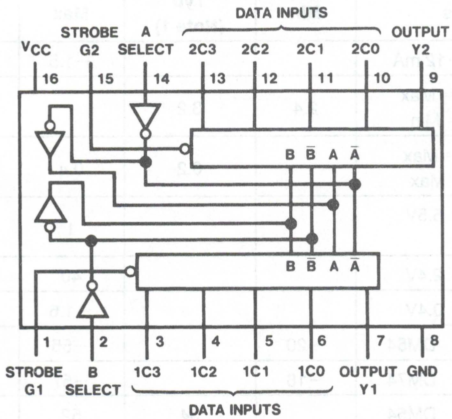
Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low-impedance, totem-pole outputs
- Typical average propagation delay times
  From data 11 ns
  From strobe 18 ns
  From select 20 ns
- Typical power dissipation 170 mW
- Alternate Military/Aerospace device (54153) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package


DATA INPUTS
STROBE G2
A SELECT
VCC
2C3
2C2
2C1
2C0
OUTPUT Y2
16
15
14
13
12
11
10
9
B B̄ A Ā
B B̄ A Ā
1
2
3
4
5
6
7
8
STROBE G1
B SELECT
1C3
1C2
1C1
1C0
OUTPUT Y1
GND
DATA INPUTS

TL/F/6547–1

Order Number 54153DMQB, 54153FMQB, DM54153J, DM54153W or DM74153N
See NS Package Number J16A, N16E or W16A

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54153			DM74153			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		34	52	mA
			DM74		34	60	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

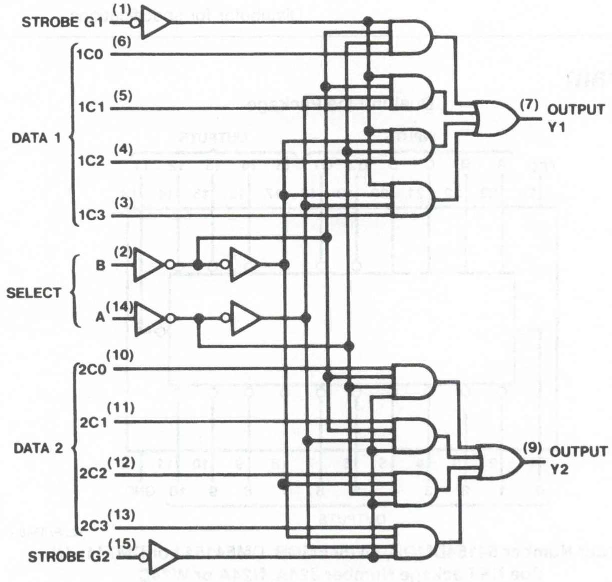
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 30 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		34	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		34	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		23	ns

Logic Diagram


STROBE G1
(1)
(6)
1C0
(5)
1C1
DATA 1
(4)
1C2
(3)
1C3
(2)
B
SELECT
(14)
A
(10)
2C0
(11)
2C1
DATA 2
(12)
2C2
(13)
2C3
(15)
STROBE G2
(7)
OUTPUT
Y1
(9)
OUTPUT
Y2

TL/F/6547-2

National Semiconductor

54154/DM54154/DM74154
4-Line to 16-Line Decoders/Demultiplexers

General Description

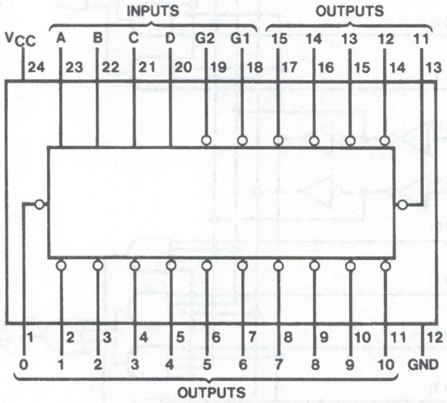
Each or these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay
  - 3 levels of logic 19 ns
  - Strobe 18 ns
- Typical power dissipation 170 mW
- Alternate Military/Aerospace device (54154) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6548–1

Order Number 54154DMQB, 54154FMQB, DM54154J or DM74154N
See NS Package Number J24A, N24A or W24C

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54154			DM74154			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.25	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		34	49	mA
			DM74		34	56	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

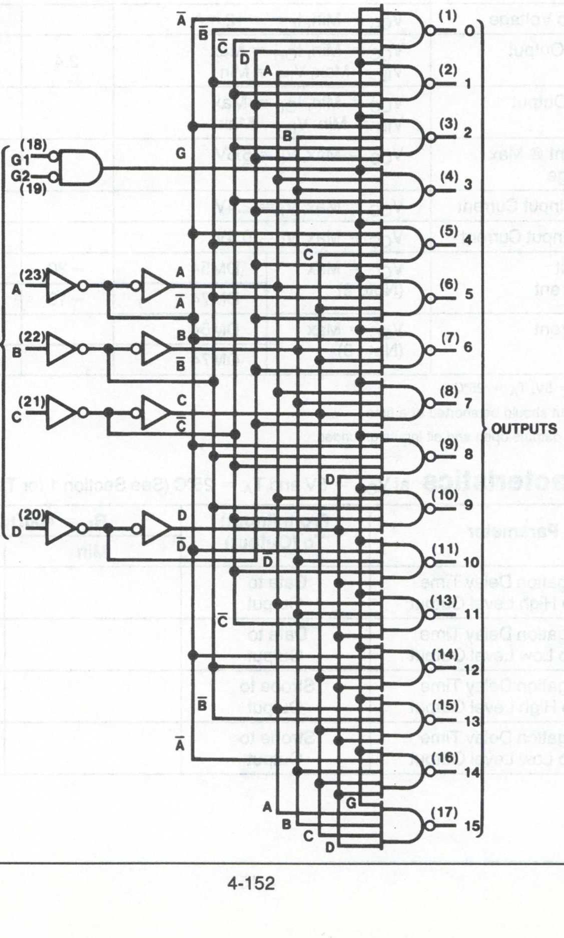
Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		27	ns

Function Table

Inputs						Outputs															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Logic Diagram


(18)
G1
G2
(19)
G
INPUTS
(23)
A
(22)
B
(21)
C
(20)
D
A
A̅
B
B̅
C
C̅
D
D̅
(1) 0
(2) 1
(3) 2
(4) 3
(5) 4
(6) 5
(7) 6
(8) 7
(9) 8
(10) 9
(11) 10
(13) 11
(14) 12
(15) 13
(16) 14
(17) 15
OUTPUTS

TL/F/6548–2

National Semiconductor

DM54155/DM74155 Dual 2-Line to 4-Line Decoders/Demultiplexers

General Description

These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demultiplexer, without external gating.

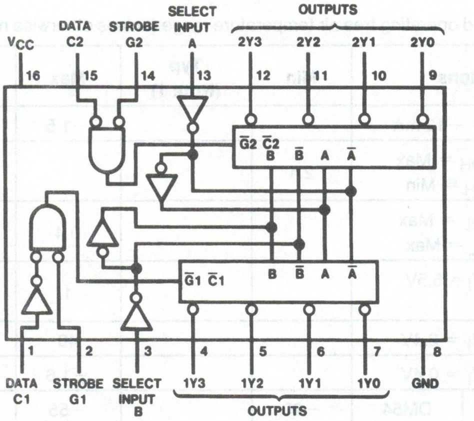
Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

Features

- Applications:
  Dual 2-to-4-line decoder
  Dual 1-to-4-line demultiplexer
  3-to-8-line decoder
  1-to-8-line demultiplexer
- Individual strobes simplify cascading for decoding or demultiplexing larger words
- Input clamping diodes simplify system design

Connection Diagram and Function Tables

Dual-In-Line Package



TL/F/6549–1

Order Number DM54155J, DM54155W or DM74155N
See NS Package Number J16A, N16A or W16A

2-Line-to-4-Line Decoder or 1-Line-to-4-Line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer

Inputs				Outputs							
Select			Strobe Or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs C1 and C2 connected together
‡G = inputs G1 and G2 connected together
H = high level, L = low level, X = don't care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54155			DM74155			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -12\text{ mA}$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$		2.4			V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}, V_{IL} = \text{Max}$				0.4	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5\text{V}$				1	mA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4\text{V}$				40	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4\text{V}$				−1.6	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 3)	DM54		25	35	mA
			DM74		25	40	

Note 1: All typicals are at $V_{CC} = 5\text{V}$, $T_A = 25°\text{C}$.

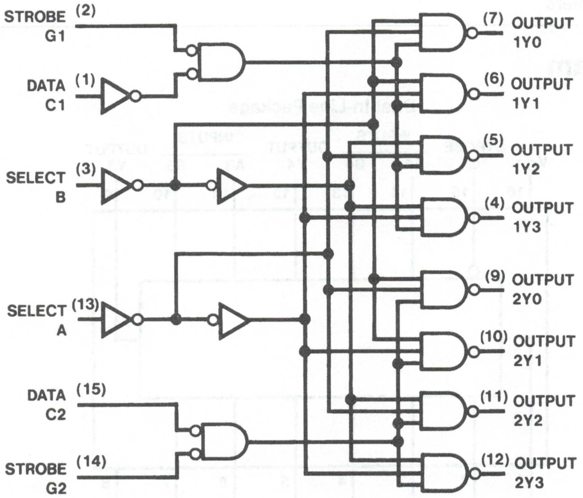
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the outputs open, A, B, and C1 inputs at 4.5V, and C2, G1, and G2 inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C2, G1 or G2 to Y		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C2, G1 or G2 to Y		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to Y		FSC	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to Y		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C1 to Y		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C1 to Y		27	ns

Logic Diagram


STROBE G1 (2)
DATA C1 (1)
SELECT B (3)
SELECT A (13)
DATA C2 (15)
STROBE G2 (14)
(7) OUTPUT 1Y0
(6) OUTPUT 1Y1
(5) OUTPUT 1Y2
(4) OUTPUT 1Y3
(9) OUTPUT 2Y0
(10) OUTPUT 2Y1
(11) OUTPUT 2Y2
(12) OUTPUT 2Y3

TL/F/6549–2

National Semiconductor

54157/DM54157/DM74157 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs.

Applications

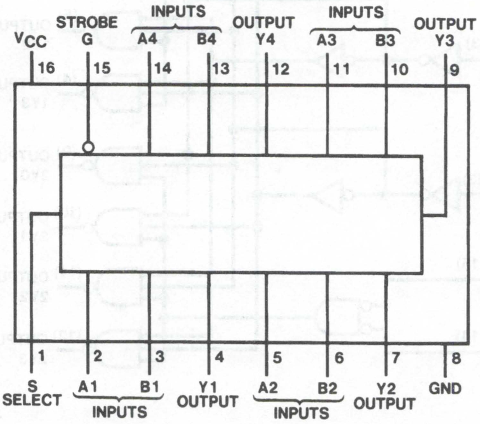
- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Features

- Buffered inputs and outputs
- Typical propagation time 9 ns
- Typical power dissipation 150 mW
- Alternate Military/Aerospace device (54157) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package


STROBE
INPUTS
OUTPUT
INPUTS
OUTPUT
V_{CC}
G
A4
B4
Y4
A3
B3
Y3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
S
SELECT
A1
B1
INPUTS
Y1
OUTPUT
A2
B2
INPUTS
Y2
OUTPUT
GND

TL/F/6550–1

Order Number 54157DMQB, 54157FMQB, DM54157J, DM54157W or DM74157N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs				Output Y
Strobe	Select	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54157			DM74157			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	48	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

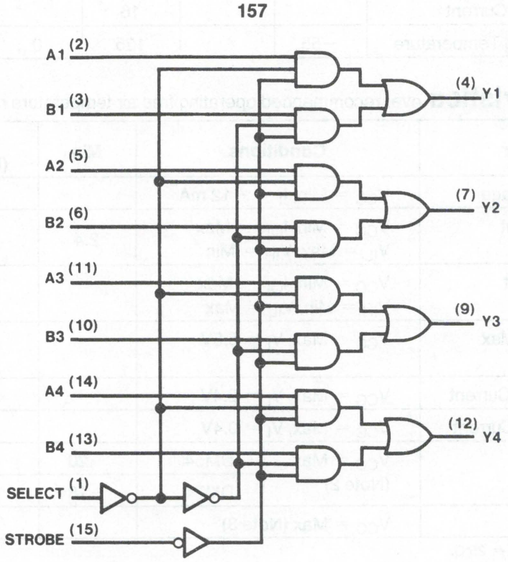
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		27	ns

Logic Diagram



157
A1 (2)
B1 (3)
A2 (5)
B2 (6)
A3 (11)
B3 (10)
A4 (14)
B4 (13)
SELECT (1)
STROBE (15)
(4) Y1
(7) Y2
(9) Y3
(12) Y4

TL/F/6550–2

National Semiconductor

54161/DM54161A/DM74161A DM54163A/DM74163A Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 161A and 163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. Low-to-high transitions at the load input of the 161A and 163A are perfectly acceptable, regardless of the logic levels on the clock or enable inputs. The clear function for the 161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low, regardless of the levels of clock, load, or enable inputs. The clear function for the 163A is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low-to-high transitions at the clear input of the 163A are also permissible, regardless of the logic levels on the clock, enable, or load inputs.

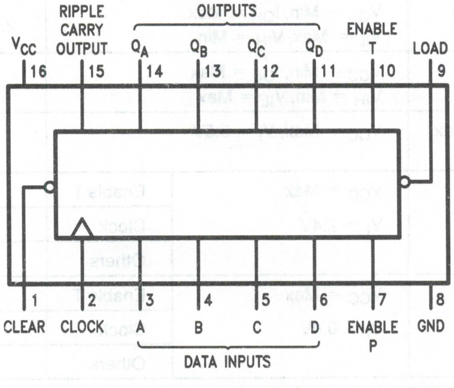
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the 161A through 163A may occur, regardless of the logic level on the clock.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Alternate Military/Aerospace device (54161) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6551–1

Order Number 54161DMQB, 54161FMQB, DM54161AJ, DM54161AW, DM54163AJ, DM54163AW, DM74161AN or DM74163AN
See NS Package Number J16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54161A and 163A			DM74161A and 163A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 6)		0		25	0		25	MHz
t_W	Pulse Width (Note 6)	Clock	25			25			ns
		Clear	20			20			
t_{SU}	Setup Time (Note 6)	Data	20			20			ns
		Enable P	34			34			
		Load	25			25			
		Clear (Note 5)	20			20			
t_H	Hold Time (Note 6)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Enable T			80	µA
			Clock			80	
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Enable T			−3.2	mA
			Clock			−3.2	
			Others			−1.6	

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−20		−57	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)	DM54		59	85	mA
			DM74		59	94	
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)	DM54		63	91	mA
			DM74		63	101	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with the LOAD high, then again with the LOAD low, with all inputs high and all outputs open.

Note 4: I_{CCL} is measured with the CLOCK high, then again with the CLOCK input low, with all inputs low and all outputs open.

Note 5: Applies to '163A which has synchronous clear inputs.

Note 6: T_A = 25°C and V_{CC} = 5V.

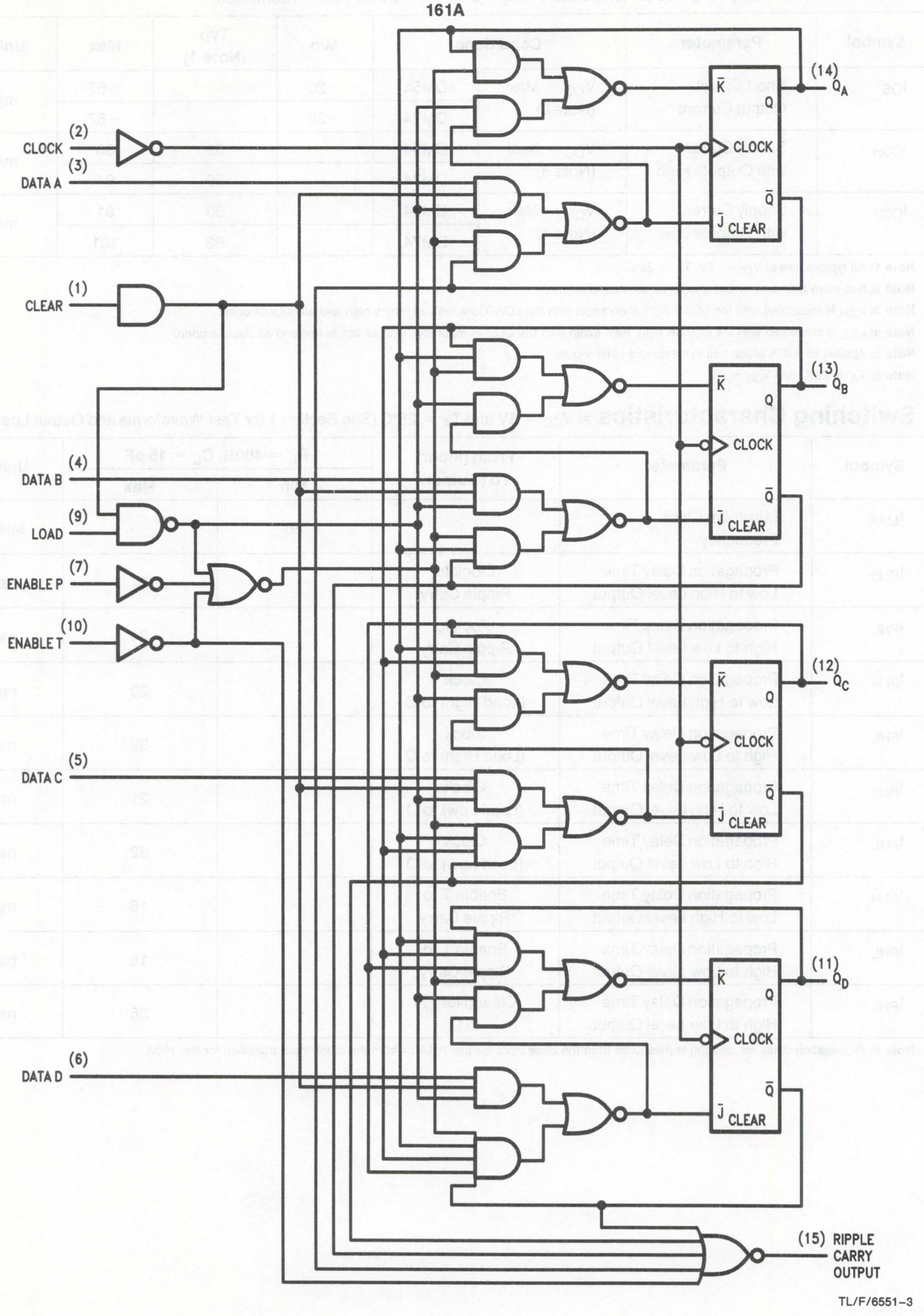
Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock (Load High) to Q		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock (Load High) to Q		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock (Load Low) to Q		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock (Load Low) to Q		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear (Note 7) to Q		36	ns

Note 7: Propagation delay for clearing is measured from the clear input for the 161A or from the clock input transition for the 163A.

4

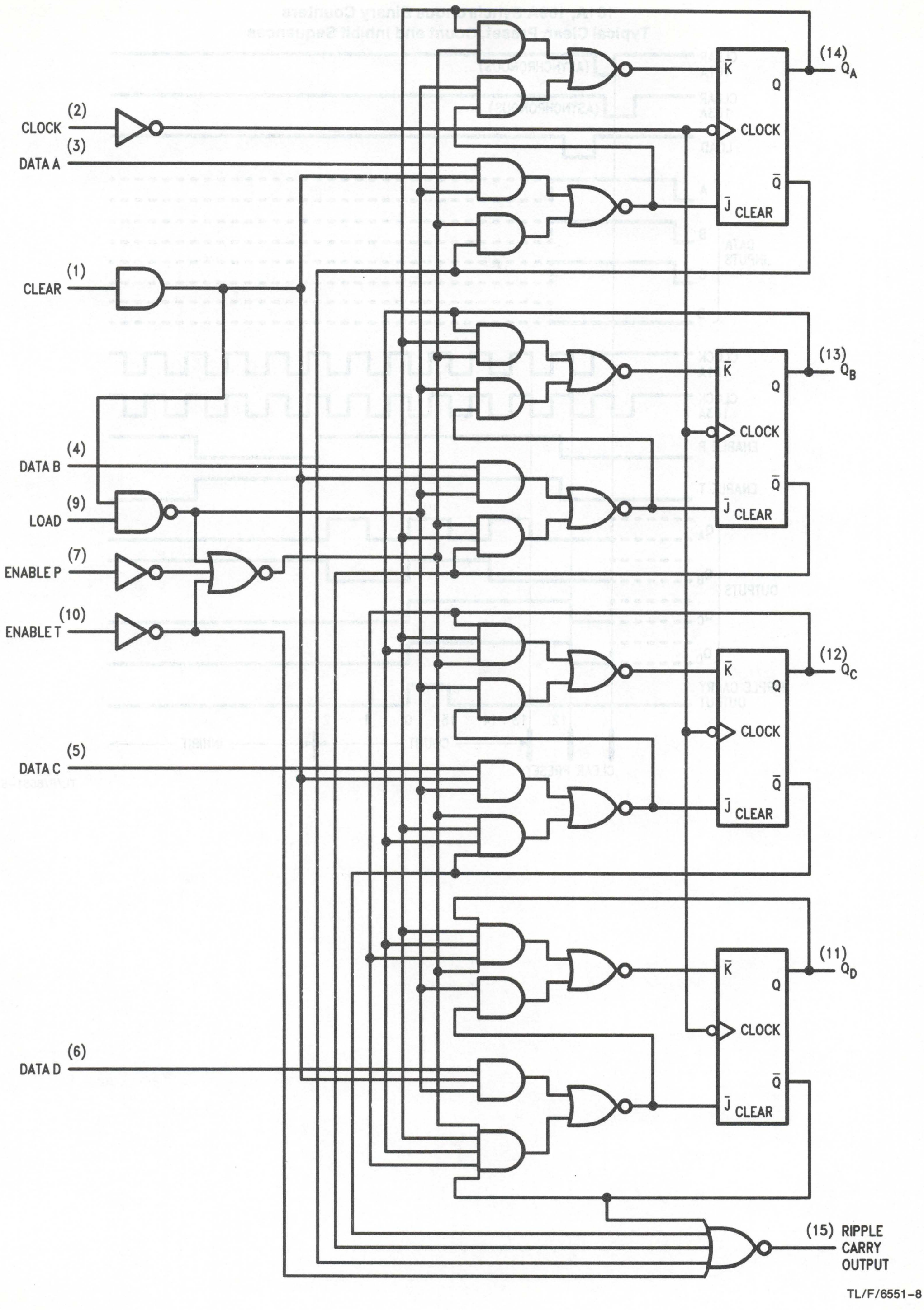
Logic Diagrams


161A
(2)
CLOCK
(3)
DATA A
(1)
CLEAR
(4)
DATA B
(9)
LOAD
(7)
ENABLE P
(10)
ENABLE T
(5)
DATA C
(6)
DATA D
K̄
Q
CLOCK
Q̄
J
CLEAR
(14) Q_A
(13) Q_B
(12) Q_C
(11) Q_D
(15) RIPPLE CARRY OUTPUT

TL/F/6551-3

Logic Diagrams (Continued)

163A

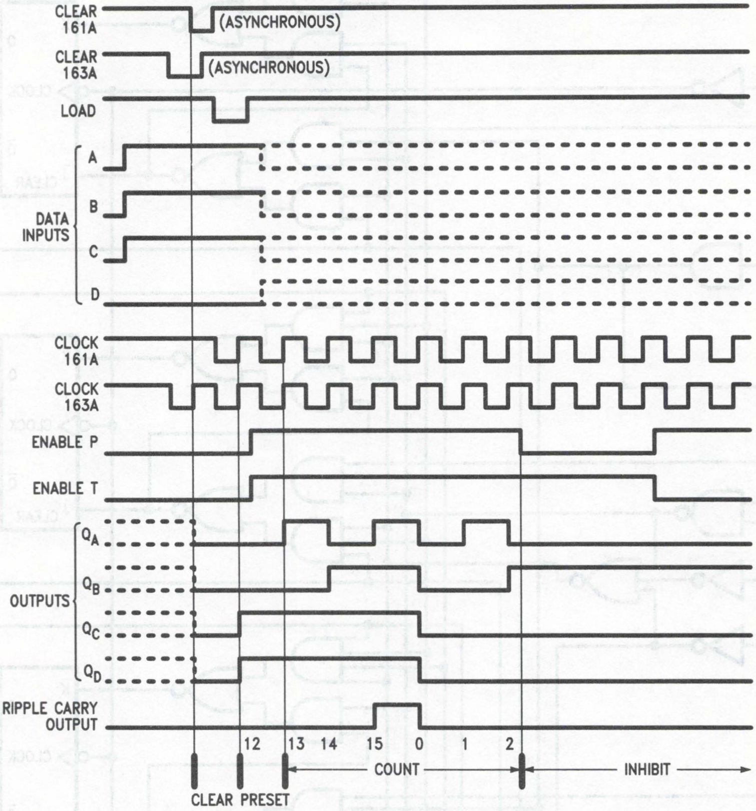


(2) CLOCK
(3) DATA A
(1) CLEAR
(4) DATA B
(9) LOAD
(7) ENABLE P
(10) ENABLE T
(5) DATA C
(6) DATA D
K̄
Q
CLOCK
Q̄
J̄
CLEAR
(14) Q_A
(13) Q_B
(12) Q_C
(11) Q_D
(15) RIPPLE CARRY OUTPUT

TL/F/6551-8

Logic Diagrams (Continued)

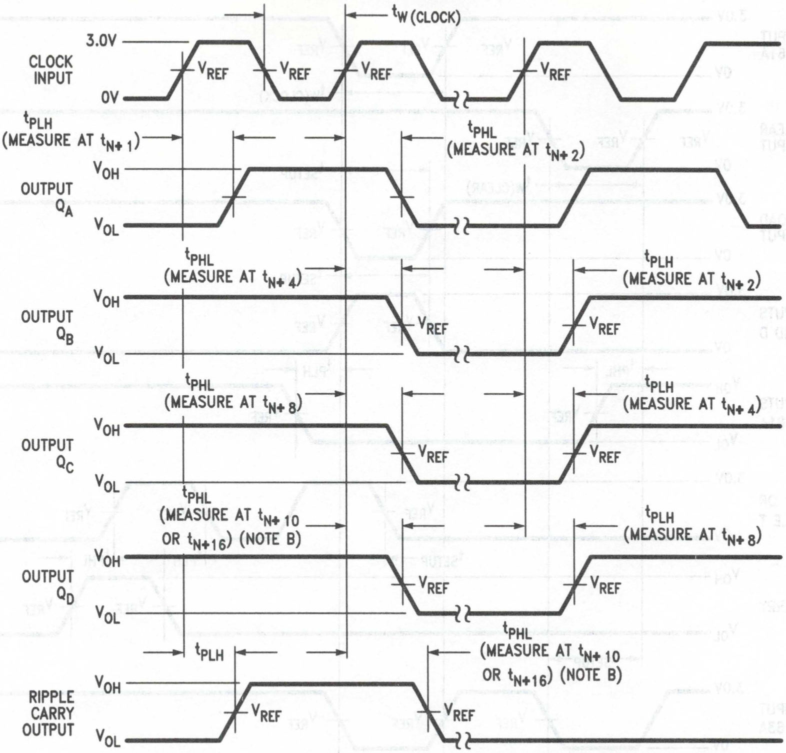
161A, 163A Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences


CLEAR 161A
(ASYNCHRONOUS)
CLEAR 163A
(ASYNCHRONOUS)
LOAD
DATA INPUTS
A
B
C
D
CLOCK 161A
CLOCK 163A
ENABLE P
ENABLE T
OUTPUTS
Q_A
Q_B
Q_C
Q_D
RIPPLE CARRY OUTPUT
12
13
14
15
0
1
2
COUNT
INHIBIT
CLEAR
PRESET

TL/F/6551-5

Parameter Measurement Information

Switching Time Waveforms


$t_{W(CLOCK)}$
3.0V
CLOCK INPUT
0V
V_{REF}
t_{PLH} (MEASURE AT t_{N+1})
t_{PHL} (MEASURE AT t_{N+2})
V_{OH}
OUTPUT Q_A
V_{OL}
t_{PHL} (MEASURE AT t_{N+4})
t_{PLH} (MEASURE AT t_{N+2})
OUTPUT Q_B
t_{PHL} (MEASURE AT t_{N+8})
t_{PLH} (MEASURE AT t_{N+4})
OUTPUT Q_C
t_{PHL} (MEASURE AT t_{N+10} OR t_{N+16}) (NOTE B)
t_{PLH} (MEASURE AT t_{N+8})
OUTPUT Q_D
t_{PLH}
t_{PHL} (MEASURE AT t_{N+10} OR t_{N+16}) (NOTE B)
RIPPLE CARRY OUTPUT

TL/F/6551-6

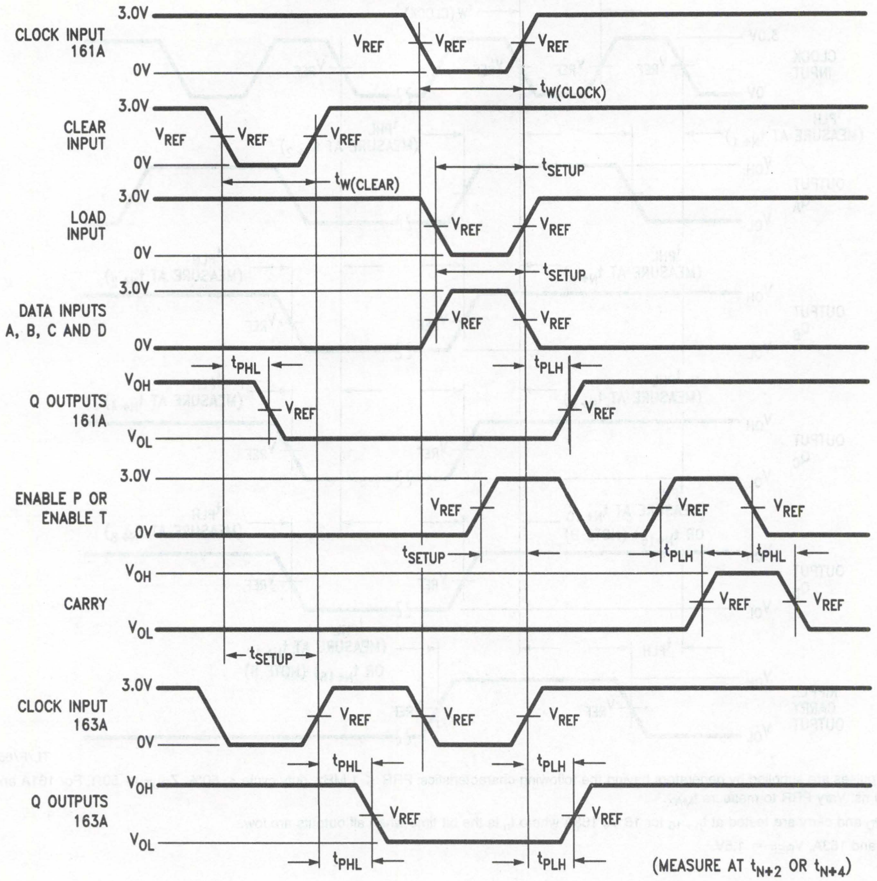
Note A: The input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$. For 161A and 163A, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+16} for 161A, 163A where t_n is the bit time when all outputs are low.

Note C: For 161A and 163A, $V_{REF} = 1.5V$.

Parameter Measurement Information (Continued)

Switching Time Waveforms


3.0V
CLOCK INPUT 161A
0V
V_{REF}
$t_{W(CLOCK)}$
CLEAR INPUT
$t_{W(CLEAR)}$
t_{SETUP}
LOAD INPUT
DATA INPUTS A, B, C AND D
t_{PHL}
t_{PLH}
V_{OH}
Q OUTPUTS 161A
V_{OL}
ENABLE P OR ENABLE T
CARRY
CLOCK INPUT 163A
Q OUTPUTS 163A
(MEASURE AT t_{N+2} OR t_{N+4})

TL/F/6551-7

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. For 161A and 163A, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Enable P and enable T setup times are measured at t_{n+0}.

Note C: For 161A and 163A, $V_{REF} = 1.5V$.

National Semiconductor

54164/DM74164
8-Bit Serial In/Parallel Out Shift Registers

General Description

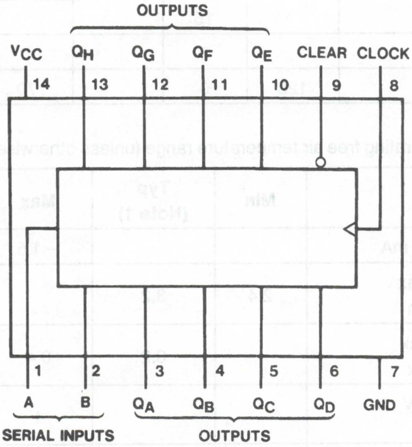
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either serial input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 185 mW

Connection Diagram

Dual-In-Line Package



TL/F/6552–1

Order Number 54164DMQB, 54164FMQB or DM74164N
See NS Package Number J14A, N14A or W14B

Function Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		54164			DM74164			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				8			8	mA
f_{CLK}	Clock Frequency (Note 4)				25	0		25	MHz
t_W	Pulse Width (Note 4)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time (Note 4)		15			15			ns
t_H	Data Hold Time (Note 4)		0			5			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −14 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54	−10		−27.5	mA
			DM74	−9		−27.5	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			37	54	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

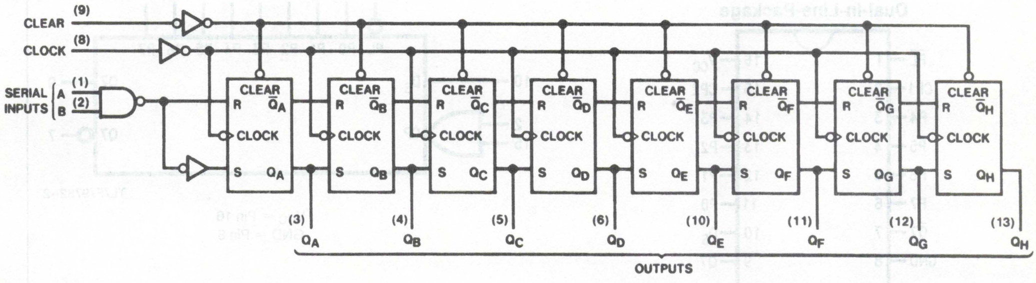
Note 3: I_{CC} is measured with all outputs open, SERIAL inputs grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 800Ω C_L = 15 pF Min	 Max	 C_L = 50 pF Min	 Max	Units
f_{MAX}	Maximum Clock Frequency		25				MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		32		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		36		42	ns

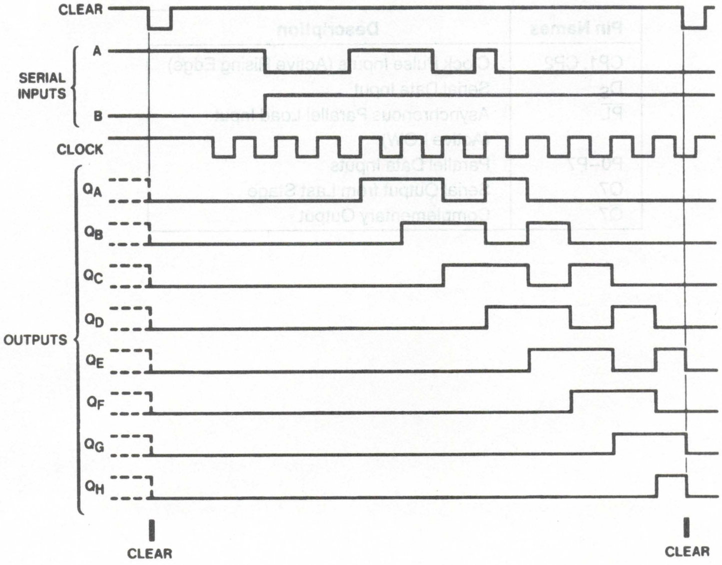
Logic Diagram



CLEAR (9)
CLOCK (8)
SERIAL INPUTS A (1) B (2)
CLEAR
R
CLOCK
S
Q_A $\overline{Q}_A$ Q_B $\overline{Q}_B$ Q_C $\overline{Q}_C$ Q_D $\overline{Q}_D$ Q_E $\overline{Q}_E$ Q_F $\overline{Q}_F$ Q_G $\overline{Q}_G$ Q_H $\overline{Q}_H$
(3) Q_A
(4) Q_B
(5) Q_C
(6) Q_D
(10) Q_E
(11) Q_F
(12) Q_G
(13) Q_H
OUTPUTS

TL/F/6552-2

Timing Diagram



CLEAR
SERIAL INPUTS
A
B
CLOCK
OUTPUTS
Q_A
Q_B
Q_C
Q_D
Q_E
Q_F
Q_G
Q_H
CLEAR
CLEAR

TL/F/6552-3

National Semiconductor

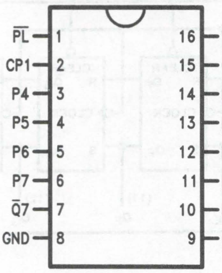
54165/DM74165
8-Bit Parallel-to-Serial Converter

General Description

The '165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputting occurs asynchronously when the Parallel Load ($\overline{PL}$) input is LOW. With $\overline{PL}$ HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (D_S) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

Connection Diagram

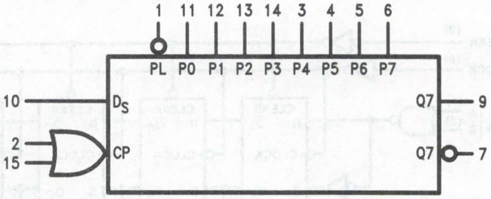
Dual-In-Line-Package


PL 1
CP1 2
P4 3
P5 4
P6 5
P7 6
Q7 7
GND 8
16 VCC
15 CP2
14 P3
13 P2
12 P1
11 P0
10 DS
9 Q7

TL/F/9782-1

Order Number 54165DMQB, 54165FMQB or DM74165N
See NS Package Number J16A, N16E or W16A

Logic Symbol


1
11
12
13
14
3
4
5
6
PL
P0
P1
P2
P3
P4
P5
P6
P7
10
DS
2
15
CP
Q7
9
Q7
7

TL/F/9782-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
CP1, CP2	Clock Pulse Inputs (Active Rising Edge)
D_S	Serial Data Input
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
P0–P7	Parallel Data Inputs
Q7	Serial Output from Last Stage
$\overline{Q7}$	Complementary Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54165			DM74165			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW P_n to $\overline{PL}$	10 10			10 10			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW P_n to $\overline{PL}$	10 10			0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW D_S to CP_n	20 20			20 20			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW D_S to CP_n	0 0			0 0			ns
$t_s(H)$	Setup Time HIGH CP1 to CP2 or CP2 to CP1	30			30			ns
$t_w(H)$	CP_n Pulse Width HIGH	25			25			ns
$t_w(L)$	$\overline{PL}$ Pulse Width LOW	15			15			ns
t_{rec}	Recovery Time, $\overline{PL}$ to CP_n	45			45			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	$\overline{PL}$			80	μA
			Inputs			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	$\overline{PL}$			−3.2	mA
			Inputs			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max, $\overline{PL}$ = ⊔ P_n = ⟍, CP_1, CP_2 = 4.5V				63	mA

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF R_L = 400Ω Min	Max	Units
f_{max}	Maximum Clock Frequency	20		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q7 or $\overline{Q}7$		31 40	ns
t_{PLH} t_{PHL}	Propagation Delay CP1 to Q7 or $\overline{Q}7$		24 31	ns
t_{PLH} t_{PHL}	Propagation Delay P7 to Q7		17 36	ns
t_{PLH} t_{PHL}	Propagation Delay P7 to $\overline{Q}7$		27 27	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Functional Description

The '165 contains eight clocked master/slave RS flip-flops connected as a shift register with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the $\overline{PL}$ signal is LOW. The parallel data can change while $\overline{PL}$ is LOW provided that the recommended setup and hold times are observed.

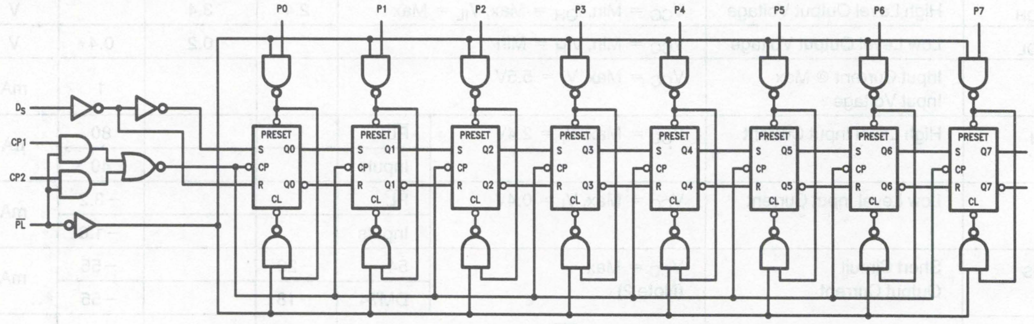
For clocked operation, $\overline{PL}$ must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit by applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

Truth Table

$\overline{PL}$	CP		Contents								Response
	1	2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	X	X	P0	P1	P2	P3	P4	P5	P6	P7	Parallel Entry
H	L	⟋	D_S	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Right Shift
H	H	⟋	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	No Change
H	⟋	L	D_S	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Right Shift
H	⟋	H	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⟋ = Positive Rising Edge

Logic Diagram



TL/F/9782–3

National Semiconductor

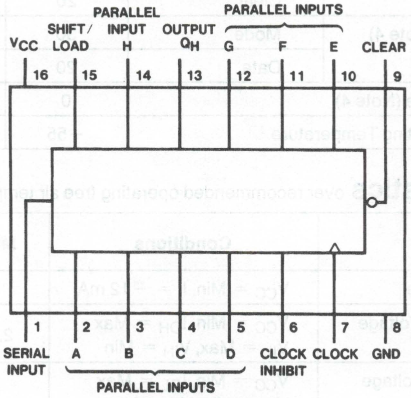
DM54166
8-Bit Parallel In/Serial Out Shift Registers

General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

Connection Diagram

Dual-In-Line Package



TL/F/6554-1

Order Number DM54166J
See NS Package Number J16A

Function Table

Inputs						Internal Outputs		Output
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from Low to High Level

a . . . h = The level of stead-state input at inputs A through H, respectively

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, Q_H, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Gn} = The level of Q_A, Q_G, respectively, before the most recent ↑ transition of the clock

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range DM54	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54166 Min	DM54166 Nom	DM54166 Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.8	mA
I_{OL}	Low Level Output Current				16	mA
f_{CLK}	Clock Frequency (Note 4)		0		25	MHz
t_W	Pulse Width (Note 4)	Clock	24			ns
		Clear	20			
t_{SU}	Setup Time (Note 4)	Mode	30			ns
		Data	20			
t_H	Data Hold Time (Note 4)		0			ns
T_A	Free Air Operating Temperature		−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−57	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)		72	104	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

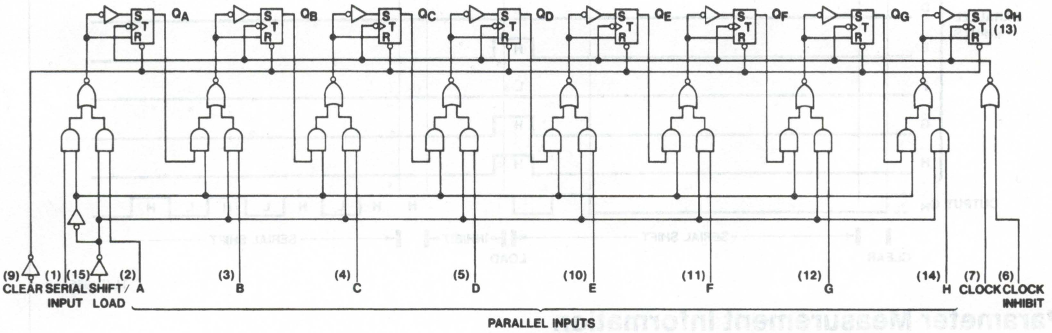
Note 3: With all outputs open, 4.5V applied to the SERIAL input, all other inputs except CLOCK grounded, I_{CC} is measured after a momentary ground, then 4.5V, is applied to the CLOCK.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega, C_L = 15$ pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output	8	26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output	8	30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		35	ns

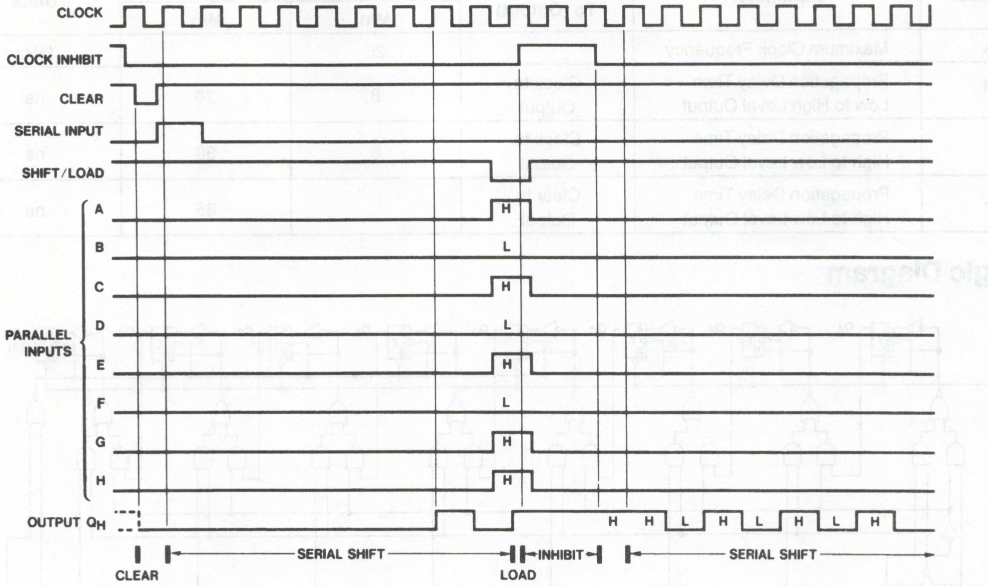
Logic Diagram


S
T
R
Q_A
Q_B
Q_C
Q_D
Q_E
Q_F
Q_G
Q_H
(13)
(9)
CLEAR
(1)
SERIAL INPUT
(15)
SHIFT/LOAD
(2)
A
(3)
B
(4)
C
(5)
D
(10)
E
(11)
F
(12)
G
(14)
H
(7)
CLOCK
(6)
CLOCK INHIBIT
PARALLEL INPUTS

TL/F/6554-2

Timing Diagram

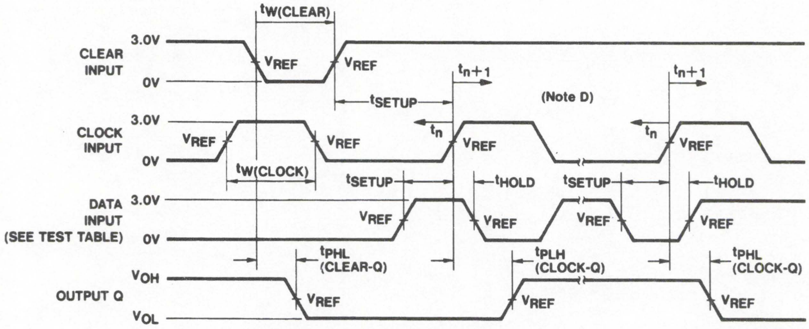
Typical Clear, Shift, Load, Inhibit, and Shift Sequences


CLOCK
CLOCK INHIBIT
CLEAR
SERIAL INPUT
SHIFT/LOAD
PARALLEL INPUTS
A
B
C
D
E
F
G
H
H
L
H
L
H
L
H
H
OUTPUT QH
H
H
L
H
L
H
L
H
CLEAR
SERIAL SHIFT
LOAD
INHIBIT
SERIAL SHIFT

TL/F/6554–3

Parameter Measurement Information

Voltage Waveforms


tW(CLEAR)
3.0V
CLEAR INPUT
0V
VREF
VREF
tn+1
tn+1
tSETUP
(Note D)
3.0V
CLOCK INPUT
0V
tn
tn
VREF
VREF
VREF
VREF
tW(CLOCK)
tSETUP
tHOLD
tSETUP
tHOLD
DATA INPUT (SEE TEST TABLE)
3.0V
0V
VREF
VREF
VREF
VREF
tPHL (CLEAR-Q)
tPLH (CLOCK-Q)
tPHL (CLOCK-Q)
OUTPUT Q
VOH
VOL
VREF
VREF
VREF

TL/F/6554–4

Test Table for Synchronous Inputs

Data Input For Test	Shift/Load	Output Tested (See Note C)
H	0V	Q_H at T_{N+1}
Serial Input	4.5V	Q_H at T_{N+8}

Note A: The clock pulse has the following characteristics:
$t_{W(clock)} \geq 20$ ns and PRR = 1 MHz.
The clear pulse has the following characteristics:
$t_{W(clear)} \geq 20$ ns and $t_{HOLD} = 0$ ns.
When testing f_{MAX}, vary the clock PRR.

Note B: A clear pulse is applied prior to each test.

Note C: Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

Note D: t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+8} = bit time after eight clocking transitions.

Note E: V_{REF} = 1.5V for 166.

National Semiconductor

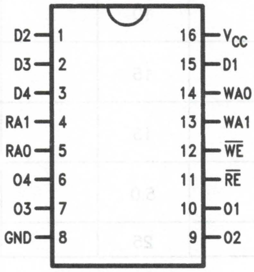
54170/DM74170
4 x 4 Register File with Open-Collector Outputs

General Description

The '170 contains 16 high speed, low power, transparent D-type latches arranged as four words of four bits each, to function as a 4 x 4 register file. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. Open-collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

Connection Diagram

Dual-In-Line Package

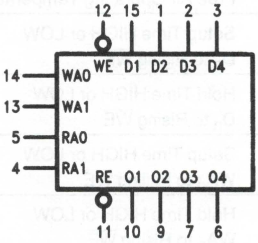


D2 1
D3 2
D4 3
RA1 4
RA0 5
O4 6
O3 7
GND 8
16 V_CC
15 D1
14 WA0
13 WA1
12 WE
11 RE
10 O1
9 O2

TL/F/9783-1

Order Number 54170DMQB, 54170FMQB or DM74170N
See NS Package Number J16A, N16E and W16A

Logic Symbol



12 15 1 2 3
WE D1 D2 D3 D4
14 WA0
13 WA1
5 RA0
4 RA1
RE O1 O2 O3 O4
11 10 9 7 6

TL/F/9783-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
D1–D4	Data Inputs
WA0, WA1	Write Address Inputs
$\overline{\text{WE}}$	Write Enable Input (Active LOW)
RA0–RA1	Read Address Inputs
$\overline{\text{RE}}$	Read Enable Input (Active LOW)
O1–O4	Data Outputs

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54170			DM74170			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5				V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s	Setup Time HIGH or LOW D_n to Rising $\overline{WE}$	10			10			ns
t_h	Hold Time HIGH or LOW D_n to Rising $\overline{WE}$	15			15			ns
t_s	Setup Time HIGH or LOW WA_n to Falling $\overline{WE}$	15			15			ns
t_h	Hold Time HIGH or LOW WA_n to Rising $\overline{WE}$	5.0			5.0			ns
t_w (L)	$\overline{WE}$ or $\overline{RE}$ Pulse Width LOW	25			25			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{OH} = Max V_{IL} = Max				30	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max, RA_n = 0V D_n, $\overline{WE}$, $\overline{RE}$ = 4.5V	54			140	mA
			DM74			150	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

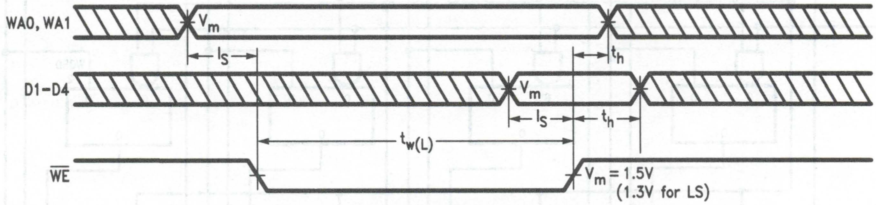
Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 2 for waveforms and load configurations)

Symbol	Parameter	54/DM74		Units
		$C_L = 15$ pF $R_L = 400\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay* RA_0 or RA_1 to O_n		35 40	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{RE}$ to O_n		15 30	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{WE}$ to O_n		40 45	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n		30 45	ns

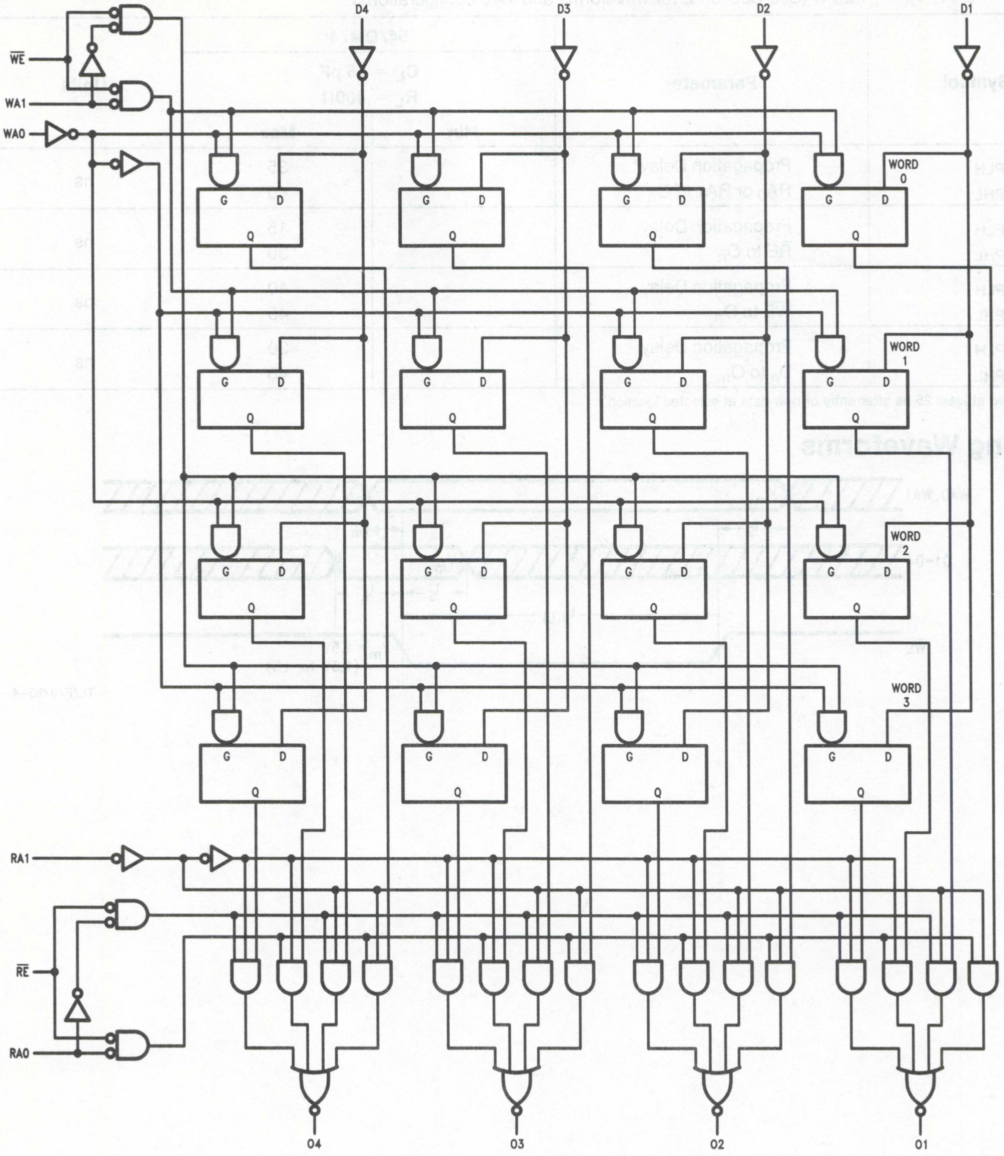
*Measured at least 25 ns after entry of new data at selected location.

Timing Waveforms


WA0, WA1
V_m
t_s
t_h
D1-D4
V_m
t_s
t_h
$t_{w(L)}$
$\overline{WE}$
$V_m = 1.5V$
(1.3V for LS)

TL/F/9783-4

Logic Diagram


D4
D3
D2
D1
WE
WA1
WA0
WORD 0
WORD 1
WORD 2
WORD 3
G
D
Q
RA1
RE
RA0
O4
O3
O2
O1

TL/F/9783-3

Write Function Table

Write Inputs			D Inputs To
$\overline{WE}$	WA_1	WA_0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (Hold)

Read Function Table

Read Inputs			Outputs From
$\overline{RE}$	RA_1	RA_0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (HIGH Z)

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

National Semiconductor

54173/DM54173/DM74173 TRI-STATE® Quad D Registers

General Description

These four-bit registers contain D-type flip-flops with totem-pole TRI-STATE outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

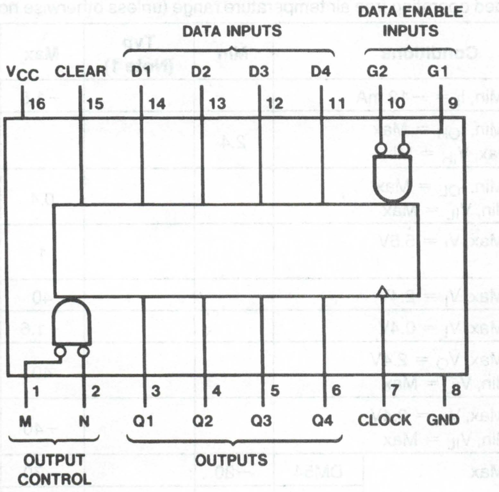
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock elminates restrictions for operating in one of two modes:
  - Parallel load
  - Do nothing (hold)
- For application as bus buffer registers
- Typical propagation delay 18 ns
- Typical frequency 30 MHz
- Typical power dissipation 250 mW
- Alternate Military/Aerospace device (54173) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6556–1

Order Number 54173DMQB, 54173FMQB, DM54173J, DM54173W or DM74173N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs					Output
Clear	Clock	Data Enable		Data	Q
		G1	G2	D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = high level (steady state)
L = low level (steady state)
↑ = low-to-high level transition
X = don't care (any input including transitions)
Q_0 = the level of Q before the indicated steady state input conditions were established

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54173 Min	DM54173 Nom	DM54173 Max	DM74173 Min	DM74173 Nom	DM74173 Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−5.2	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 4)		0		25	0		25	MHz
t_W	Pulse Width (Note 4)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Setup Time (Note 4)	Enable	17			17			ns
		Data	10			10			
t_H	Hold Time (Note 4)	Enable	2			2			ns
		Data	10			10			
t_{REL}	Clear Release Time (Note 4)		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−30		−70	mA
			DM74	−30		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			50	72	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

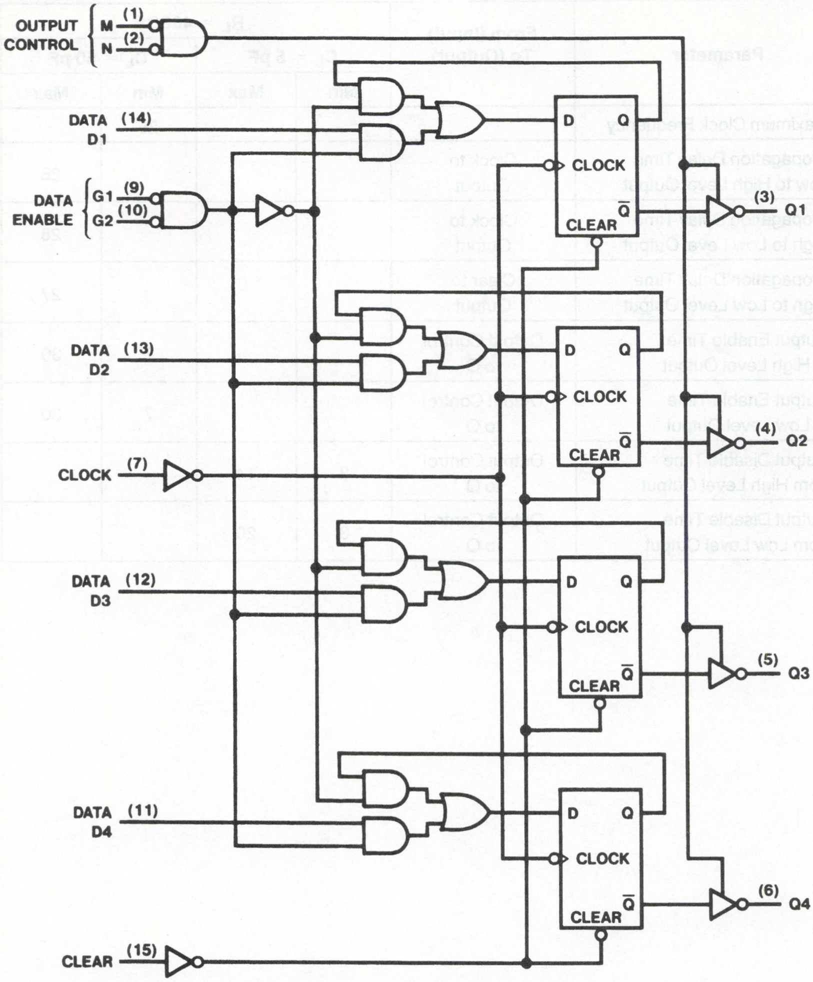
Note 3: I_{CC} is measured with all outputs open, CLEAR grounded after a momentary connection to 4.5V: N, G1, G2 and all DATA inputs grounded: and the CLOCK input and M input at 4.5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω				Units
			C_L = 5 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency				25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output				25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output				28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output				27	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Q			7	30	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Q			7	30	ns
t_{PHZ}	Output Disable Time from High Level Output	Output Control to Q	3	14			ns
t_{PLZ}	Output Disable Time from Low Level Output	Output Control to Q	3	20			ns

Logic Diagram


OUTPUT CONTROL
M
(1)
N
(2)
DATA D1
(14)
DATA ENABLE
G1
(9)
G2
(10)
DATA D2
(13)
CLOCK
(7)
DATA D3
(12)
DATA D4
(11)
CLEAR
(15)
D
Q
CLOCK
$\overline{Q}$
CLEAR
(3)
Q1
(4)
Q2
(5)
Q3
(6)
Q4

TL/F/6556–2

National Semiconductor

54174/DM54174/DM74174, 54175/DM54175/DM74175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) version features complementary outputs from each flip-flop.

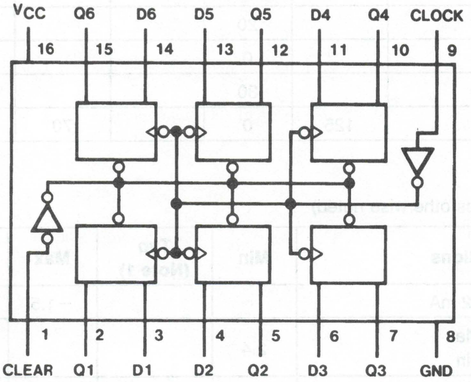
Information at the D inputs meeting the setup and hold time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- 174 contains six flip-flops with single-rail outputs
- 175 contains four flip-flops with double-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 40 MHz
- Typical power dissipation per flip-flop 38 mW
- Alternate Military/Aerospace device (54174, 54175) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

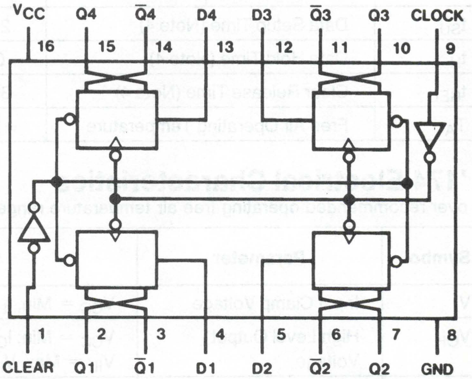
Dual-In-Line Package



TL/F/6557–1

Order Number 54174DMQB, 54174FMQB, DM54174J, DM54174W or DM74174N
See NS Package Number J16A, N16E or W16A

Dual-In-Line Package



TL/F/6557–2

Order Number 54175DMQB, 54175FMQB, DM54175J, DM54175W or DM74175N
See NS Package Number J16A, N16E or W16A

Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = 175 only

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54174 Min	DM54174 Nom	DM54174 Max	DM74174 Min	DM74174 Nom	DM74174 Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 4)		0		30	0		30	MHz
t_W	Pulse Width (Note 4)	Clock Low	25			25			ns
		Clock High	10			10			
		Clear	20			20			
t_{SU}	Data Setup Time (Note 4)		20			20			ns
t_H	Data Hold Time (Note 4)		0			0			ns
t_{REL}	Clear Release Time (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'174 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			45	65	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open and all DATA and CLEAR inputs at 4.5V, I_{CC} is measured after a momentary ground, then 4.5V applied to the CLOCK input.

Note 4: T_A = 25°C and V_{CC} = 5V.

'174 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		40	ns

Recommended Operating Conditions

Symbol	Parameter		DM54175			DM74175			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
t_W	Pulse Width (Note 1)	Clock Low	25			25			ns
		Clock High	10			10			
		Clear	20			20			
t_{SU}	Data Setup Time (Note 1)		20			20			ns
t_H	Data Hold Time (Note 1)		0			0			ns
t_{REL}	Clear Release Time (Note 1)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: T_A = 25°C and V_{CC} = 5V.

'175 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	45	mA

'175 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q or $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q or $\overline{Q}$		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to Any $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		40	ns

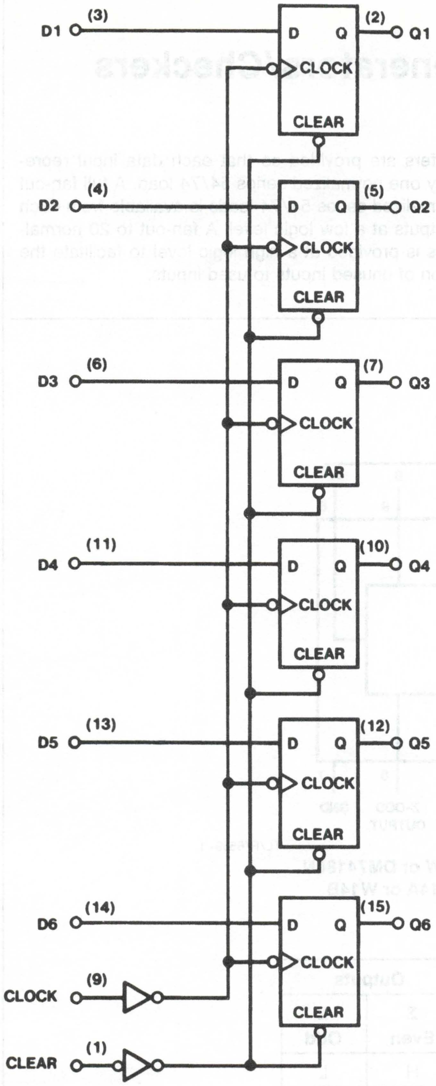
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open and 4.5V applied to all DATA and CLEAR inputs, I_{CC} is measured after a momentary ground then 4.5V applied to the CLOCK.

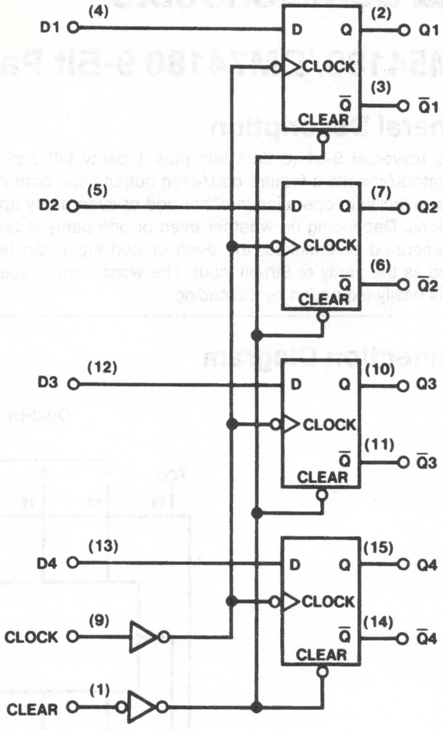
Logic Diagrams

174


D1 (3)
(2) Q1
D2 (4)
(5) Q2
D3 (6)
(7) Q3
D4 (11)
(10) Q4
D5 (13)
(12) Q5
D6 (14)
(15) Q6
D
Q
CLOCK
CLEAR
CLOCK (9)
CLEAR (1)

TL/F/6557-3

175


D1 (4)
(2) Q1
(3) $\overline{Q}$1
D2 (5)
(7) Q2
(6) $\overline{Q}$2
D3 (12)
(10) Q3
(11) $\overline{Q}$3
D4 (13)
(15) Q4
(14) $\overline{Q}$4
D
Q
$\overline{Q}$
CLOCK
CLEAR
CLOCK (9)
CLEAR (1)

TL/F/6557-4

National Semiconductor

DM54180/DM74180 9-Bit Parity Generators/Checkers

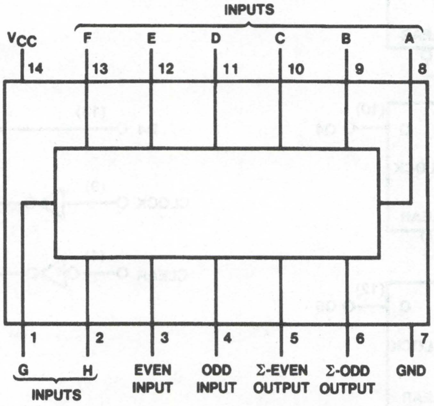
General Description

These universal 9-bit (8 data bits plus 1 parity bit) parity generators/checkers feature odd/even outputs and control inputs to facilitate operation in either odd or even parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd input can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6559–1

Order Number DM54180J, DM54180W or DM74180N
See NS Package Number J14A, N14A or W14B

Function Table

Inputs			Outputs	
Σ of H's at A thru H	Even	Odd	Σ Even	Σ Odd
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54180			DM74180			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Odd or Even			80	μA
			Data			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Odd or Even			−3.2	mA
			Data			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		34	49	mA
			DM74		34	56	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

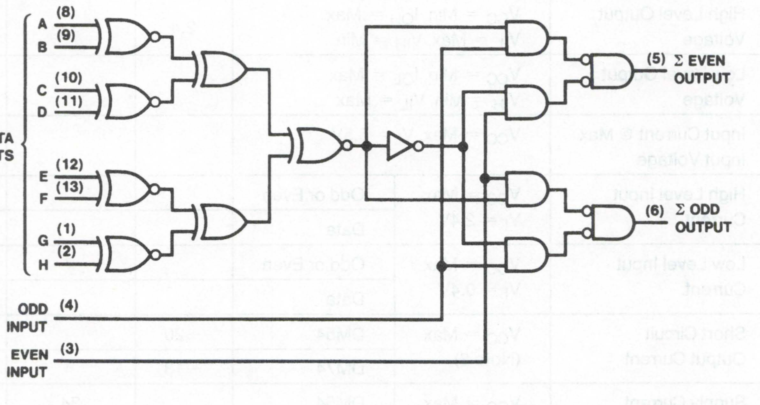
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with EVEN and ODD inputs at 4.5V, all other inputs and outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Even	$C_L = 15$ pF $R_L = 400\Omega$ Odd Input Low		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Even			68	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Odd			48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Odd			38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Even	$C_L = 15$ pF $R_L = 400\Omega$ Odd Input High		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Even			38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Odd			60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Odd			68	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Even or Odd to Σ Even or Σ Odd	$C_L = 15$ pF $R_L = 400\Omega$		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Even or Odd to Σ Even or Σ Odd			10	ns

Logic Diagram



TL/F/6559–2

National Semiconductor

DM54181
Arithmetic Logic Unit/Function Generators

General Description

These arithmetic logic units (ALU)/function generators perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables I and II. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (P and G) for the four bits in the package. When used in conjunction with the DM54S182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown below illustrate how little time is required for addition of longer words, when full carry look-ahead is employed. The method of cascading 182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the DM54S182.

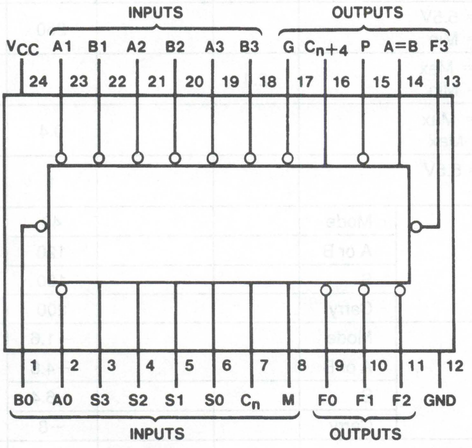
(Continued)

Features

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - EXCLUSIVE-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high-speed operations on long words

Connection Diagram

Dual-In-Line Package



TL/F/6560–1

Order Number DM54181J
See NS Package Number J24A

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
P	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

Number of Bits	Typical Addition Times	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	20 ns	1	0	None
5 to 8	30 ns	2	0	Ripple
9 to 16	30 ns	3 or 4	1	Full Look-Ahead
17 to 64	50 ns	5 to 16	2 to 5	Full Look-Ahead

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage (A = B Output)	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54181 Min	DM54181 Nom	DM54181 Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Voltage (A = B Output)			5.5	V
I_{OH}	High Level Output Current (All Except A = B)			−800	µA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current (A = B Output)	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min			250	µA
V_{OH}	High Level Output Voltage (All Except A = B)	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Mode		40	µA
			A or B		120	
			S		160	
			Carry		200	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Mode		−1.6	mA
			A or B		−4.8	
			S		−6.4	
			Carry		−8	
I_{OS}	Short Circuit Output Current (All Except A = B)	V_{CC} = Max V_I = 2.4V	−20		−55	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)		88	127	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)		92	135	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with S0 through S3, M, and A inputs at 4.5V, all other inputs grounded and all outputs open.

Note 4: I_{CCL} is measured with S0 through S3 and M inputs at 4.5V, all other inputs grounded and all outputs open.

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input)	To (Output)	Conditions	DM54181 $R_L = 400\Omega$, $C_L = 15$ pF Min	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	C_n+4			18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					19	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	C_n+4	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{\text{SUM}}$ mode)		30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					33	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	C_n+4	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{\text{DIFF}}$ mode)		30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					33	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	Any F	M = 0V ($\overline{\text{SUM}}$ or $\overline{\text{DIFF}}$ mode)		19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					18	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	G	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{\text{SUM}}$ mode)		19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					19	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	G	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{\text{DIFF}}$ mode)		20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					25	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	P	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{\text{SUM}}$ mode)		19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					25	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	P	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{\text{DIFF}}$ mode)		25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					25	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{\text{SUM}}$ mode)		30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					30	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{\text{DIFF}}$ mode)		24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					24	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 4.5V (logic mode)		28	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					30	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	A = B	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{\text{DIFF}}$ mode)		40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					40	

General Description (Continued)

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition, where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to provide A—B.

The 181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_n+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The DM54181 can be used with the signal designations of either *Figure 1* or *Figure 2*.

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table I; those obtained with the signal designations of *Figure 2* are given in Table II.

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table I)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_n+4$	X	Y
Active-Low Data (Table II)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	C_n	C_n+4	$\overline{P}$	$\overline{G}$

Input C_n	Output C_n+4	Active-High Data (Figure 1)	Active-Low Data (Figure 2)
H	H	A≤B	A≥B
H	L	A>B	A<B
L	H	A<B	A>B
L	L	A≥B	A≤B

General Description (Continued)

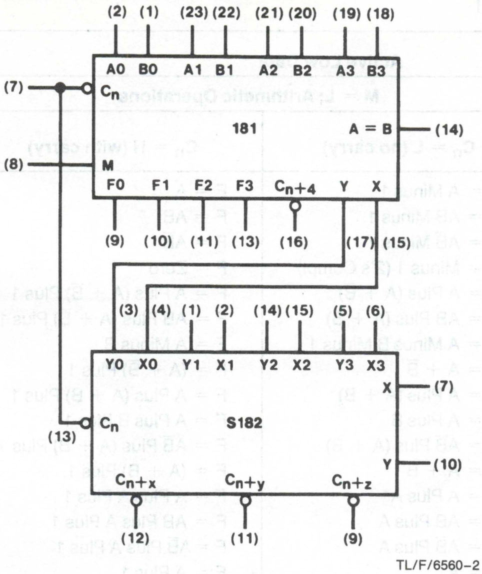

(2) (1) (23) (22) (21) (20) (19) (18)
A0 B0 A1 B1 A2 B2 A3 B3
(7)
C_n
181
A = B
(14)
(8)
M
F0 F1 F2 F3 C_{n+4} Y X
(9) (10) (11) (13) (16) (17) (15)
(3) (4) (1) (2) (14) (15) (5) (6)
Y0 X0 Y1 X1 Y2 X2 Y3 X3
X
(7)
C_n
S182
(13)
Y
(10)
C_{n+x} C_{n+y} C_{n+z}
(12) (11) (9)
TL/F/6560-2

FIGURE 1

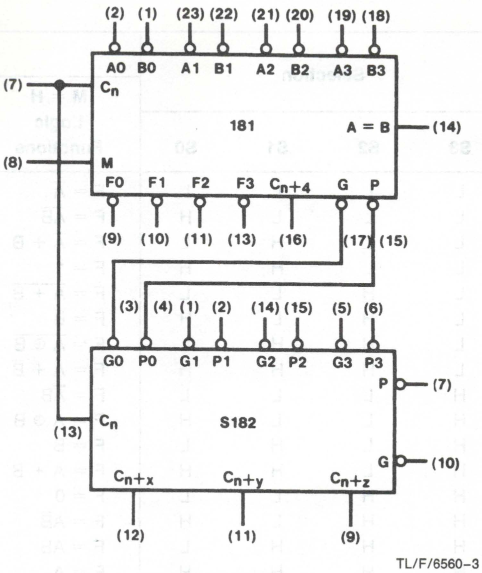

(2) (1) (23) (22) (21) (20) (19) (18)
A0 B0 A1 B1 A2 B2 A3 B3
(7)
C_n
181
A = B
(14)
(8)
M
F0 F1 F2 F3 C_{n+4} G P
(9) (10) (11) (13) (16) (17) (15)
(3) (4) (1) (2) (14) (15) (5) (6)
G0 P0 G1 P1 G2 P2 G3 P3
P
(7)
C_n
S182
(13)
G
(10)
C_{n+x} C_{n+y} C_{n+z}
(12) (11) (9)
TL/F/6560-3

FIGURE 2

TABLE I

Selection				Active High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A Plus 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + \overline{B})$ Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	$F = \overline{AB}$	F = A Plus $A\overline{B}$	F = A Plus $A\overline{B}$ Plus 1
L	H	L	H	$F = \overline{B}$	F = (A + B) Plus $A\overline{B}$	F = (A + B) Plus $A\overline{B}$ Plus 1
L	H	H	L	$F = A \oplus B$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A\overline{B}$	F = $A\overline{B}$ Minus 1	$F = A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = $(A + \overline{B})$ Plus AB	F = $(A + \overline{B})$ Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = $(A + \overline{B})$ Plus A	F = $(A + \overline{B})$ Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

*Each bit is shifted to the next more significant position.

General Description (Continued)

TABLE II

Selection				M = H Logic Functions	Active Low Data M = L; Arithmetic Operations	
S3	S2	S1	S0		C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + $\overline{B}$)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A ⊕ B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Parameter Measurement Information

Logic Mode Test Table
Function Inputs: S1 = S2 = M = 4.5V, S0 = S3 = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	A_i	B_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PHL}							
t_{PLH}	B_i	A_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PHL}							

SUM Mode Test Table
Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	A_i	B_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PHL}							
t_{PLH}	B_i	A_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PHL}							
t_{PLH}	A_i	B_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}							
t_{PLH}	B_i	A_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}							

Parameter Measurement Information (Continued)

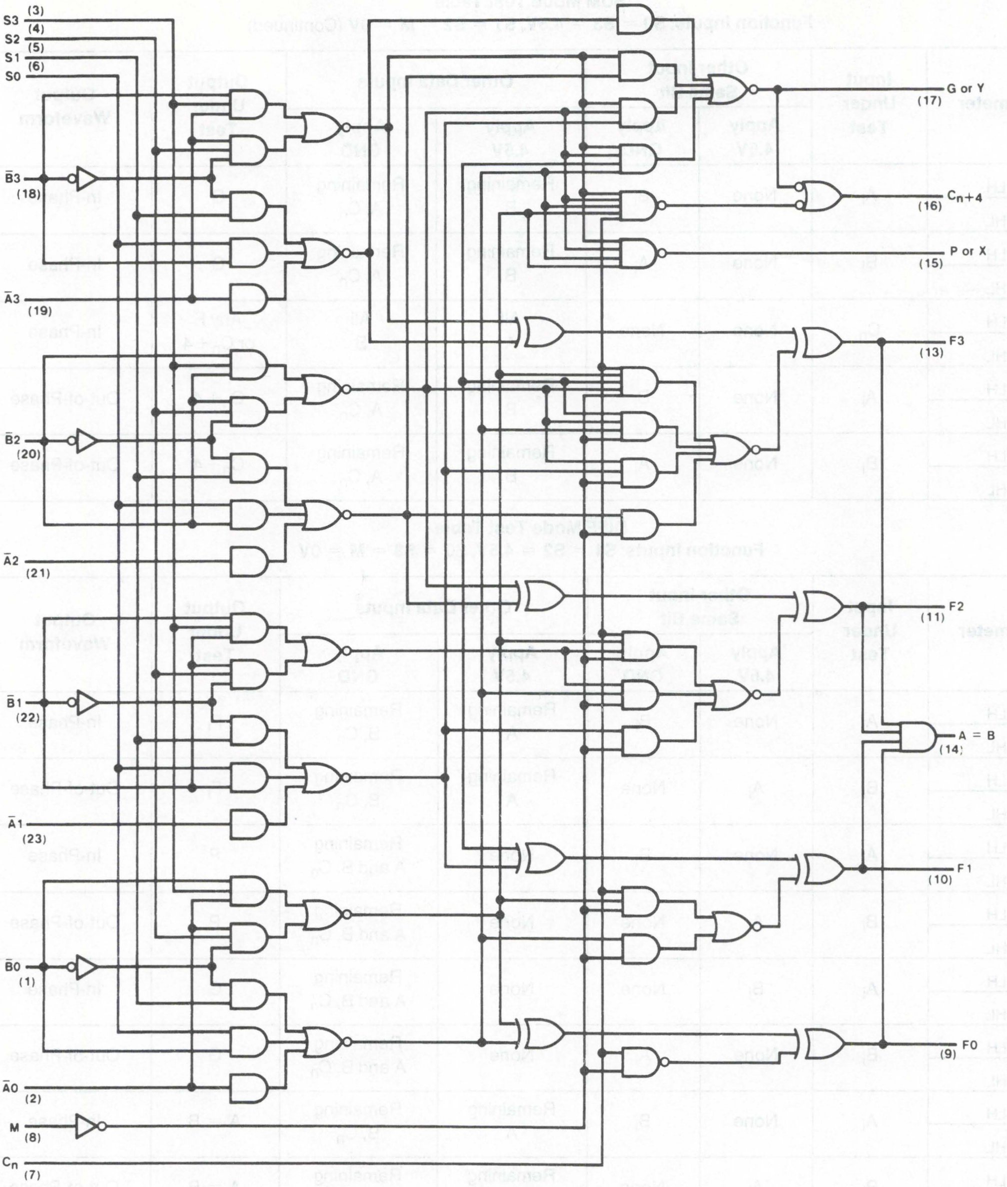
$\overline{\text{SUM}}$ Mode Test Table
Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V (Continued)

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} t_{PHL}	C_n	None	None	All A	All B	Any F or C_n+4	In-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase

$\overline{\text{DIFF}}$ Mode Test Table
Function Inputs: S1 = S2 = 4.5V, S0 = S3 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	F_i	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	F_i	Out-of-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	G	In-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PLH} t_{PHL}	C_n	None	None	All A and B	None	C_n+4 or any F	In-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A, B, C_n	C_n+4	Out-of-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	None	Remaining A, B, C_n	C_n+4	In-Phase

Logic Diagram


S3 (3)
S2 (4)
S1 (5)
S0 (6)
B̄3 (18)
Ā3 (19)
B̄2 (20)
Ā2 (21)
B̄1 (22)
Ā1 (23)
B̄0 (1)
Ā0 (2)
M (8)
C_n (7)
G or Y (17)
C_{n+4} (16)
P or X (15)
F3 (13)
F2 (11)
A = B (14)
F1 (10)
F0 (9)

TL/F/6560-4

V_{CC} = PIN 24
GND = PIN 12

National Semiconductor

DM74184/DM74185A BCD-to-Binary and Binary-to-BCD Converters

General Description

These monolithic converters are derived from the 256-bit read only memories, DM5488, and DM7488. Emitter connections are made to provide direct read-out of converted codes at outputs Y8 through Y1, as shown in the function tables. These converters demonstrate the versatility of a read only memory in that an unlimited number of reference tables or conversion tables may be built into a system. Both of these converters comprehend that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6-bit converter is produced in each case. Both devices are cascadable to N bits.

An overriding enable input is provided on each converter which when taken high inhibits the function, causing all outputs to go high. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the 185A and all "don't care" conditions of the 184 are programmed high. The outputs are of the open-collector type.

DM74184 BCD-TO-BINARY CONVERTERS

The 6-bit BCD-to-binary function of the DM74184 is analogous to the algorithm:

a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.

b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

In addition to BCD-to-binary conversion, the DM74184 is programmed to generate BCD 9's complement or BCD 10's complement. Again, in each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7 and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the function table when the devices are connected as shown.

DM74185A BINARY-TO-BCD CONVERTERS

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

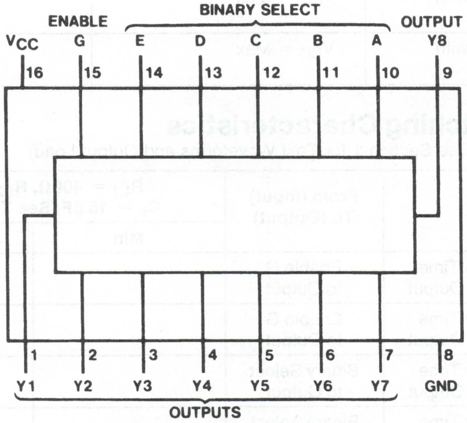
a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.

b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.

c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

(Continued)

Connection Diagram



TL/F/6561–1

Order Number DM74184N or DM74185AN
See NS Package Number N16E

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Voltage			5.5	V
I_{OL}	Low Level Output Current			12	mA
T_A	Free Air Operating Temperature	0		70	°C

'184 and '185A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min			100	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		65	95	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		80	99	mA

'184 and '185A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_{L1} = 400\Omega$, $R_{L2} = 600\Omega$ C_L = 15 pF (See Test Circuit)		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable G to Output		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable G to Output		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Binary Select to Output		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Binary Select to Output		35	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

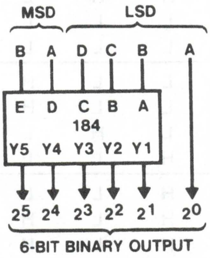
General Description (Continued)

DM74184 BCD-to-Binary

TABLE I. Package Count and Delay Times for BCD-to-Binary Conversion

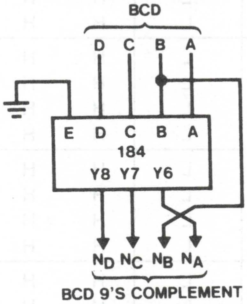
Input (Decades)	Packages Required	Total Delay Times (ns)	
		Typ	Max
2	2	56	80
3	6	140	200
4	12	196	280
5	19	280	400
6	28	364	520

6-Bit Converter


MSD
LSD
B A D C B A
E D C B A
184
Y5 Y4 Y3 Y2 Y1
2^5 2^4 2^3 2^2 2^1 2^0
6-BIT BINARY OUTPUT

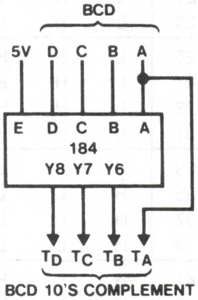
TL/F/6561–2

BCD 9's Complement Converter


BCD
D C B A
E D C B A
184
Y8 Y7 Y6
N_D N_C N_B N_A
BCD 9'S COMPLEMENT

TL/F/6561–3

BCD's 10's Complement Converter


BCD
5V D C B A
E D C B A
184
Y8 Y7 Y6
T_D T_C T_B T_A
BCD 10'S COMPLEMENT

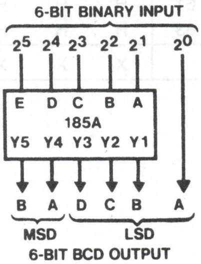
TL/F/6561–4

DM74185A Binary-to-BCD

TABLE II. Package Count and Delay Times for Binary-to-BCD Conversion

Input (Bits)	Packages Required	Total Delay Times (ns)	
		Typ	Max
4 to 6	1	25	40
7 or 8	3	50	80
9	4	75	120
10	6	100	160
11	7	125	200
12	8	125	200
13	10	150	240
14	12	175	280
15	14	175	280
16	16	200	320
17	19	225	360
18	21	225	360
19	24	250	400
20	27	275	440

6-Bit Converter


6-BIT BINARY INPUT
2^5 2^4 2^3 2^2 2^1 2^0
E D C B A
185A
Y5 Y4 Y3 Y2 Y1
B A D C B A
MSD
LSD
6-BIT BCD OUTPUT

TL/F/6561–5

Function Tables

Binary Words		Inputs						Outputs							
		Binary Select					Enable								
		E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2	3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4	5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6	7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8	9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10	11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12	13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14	15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16	17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18	19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20	21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22	23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24	25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26	27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28	29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30	31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32	33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34	35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36	37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38	39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40	41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42	43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44	45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46	47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48	49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50	51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52	53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54	55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56	57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58	59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60	61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62	63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
All		X	X	X	X	X	H	H	H	H	H	H	H	H	H

Function Tables (Continued)

BCD-to-Binary Converter

BCD Words		Inputs (See Note A)						Outputs (See Note B)				
		E	D	C	B	A	G	Y5	Y4	Y3	Y2	Y1
0	1	L	L	L	L	L	L	L	L	L	L	L
2	3	L	L	L	L	H	L	L	L	L	L	H
4	5	L	L	L	H	L	L	L	L	L	H	L
6	7	L	L	L	H	H	L	L	L	L	H	H
8	9	L	L	H	L	L	L	L	L	H	L	L
10	11	L	H	L	L	L	L	L	L	H	L	H
12	13	L	H	L	L	H	L	L	L	H	H	L
14	15	L	H	L	H	L	L	L	L	H	H	H
16	17	L	H	L	H	H	L	L	H	L	L	L
18	19	L	H	H	L	L	L	L	H	L	L	H
20	21	H	L	L	L	L	L	L	H	L	H	L
22	23	H	L	L	L	H	L	L	H	L	H	H
24	25	H	L	L	H	L	L	L	H	H	L	L
26	27	H	L	L	H	H	L	L	H	H	L	H
28	29	H	L	H	L	L	L	L	H	H	H	L
30	31	H	H	L	L	L	L	L	H	H	H	H
32	33	H	H	L	L	H	L	H	L	L	L	L
34	35	H	H	L	H	L	L	H	L	L	L	H
36	37	H	H	L	H	H	L	H	L	L	H	L
38	39	H	H	H	L	L	L	H	L	L	H	H
Any		X	X	X	X	X	H	H	H	H	H	H

BCD 9's or BCD 10's Complement Converter

BCD Word	Inputs (See Note C)						Outputs (See Note D)		
	E†	D	C	B	A	G	Y8	Y7	Y6
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	H	L	L	H	L
6	L	L	H	H	L	L	L	L	H
7	L	L	H	H	H	L	L	L	L
8	L	H	L	L	L	L	L	L	H
9	L	H	L	L	H	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	H	L	L	H	L
6	H	L	H	H	L	L	L	H	L
7	H	L	H	H	H	L	L	L	H
8	H	H	L	L	L	L	L	L	H
9	H	H	L	L	H	L	L	L	L
Any	X	X	X	X	X	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Note A: Input Conditions other than those shown produce highs at outputs Y1 through Y5.

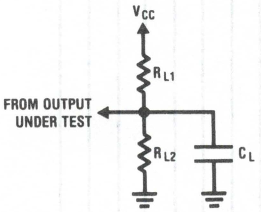
Note B: Output Y6, Y7, and Y8 are not used for BCD-to-Binary conversion.

Note C: Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

Note D: Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

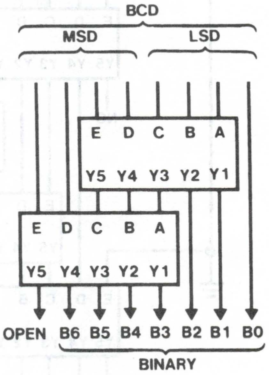
Test Circuit



TL/F/6561-6

C_L includes probe and jig capacitance

Typical Applications

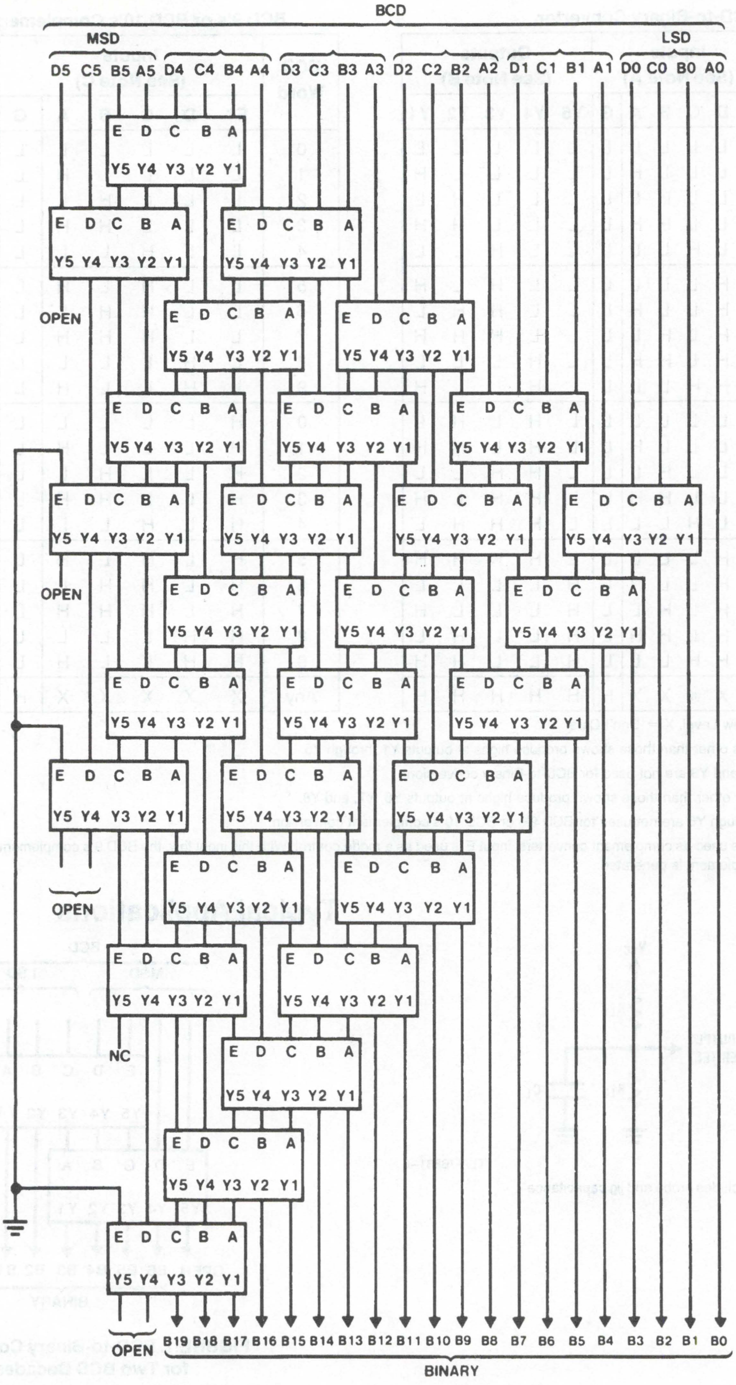


TL/F/6561-7

FIGURE 1. BCD-to-Binary Converter for Two BCD Decades

MSD—Most significant decade
LSD—Least significant decade
Each rectangle represents a DM74184

Typical Applications (Continued)

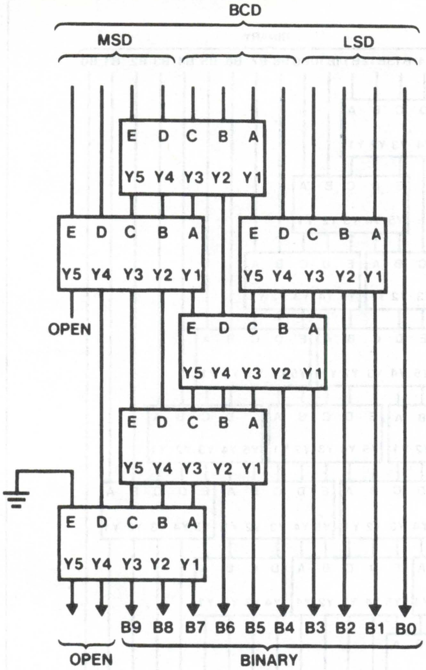

BCD
MSD
LSD
D5 C5 B5 A5 D4 C4 B4 A4 D3 C3 B3 A3 D2 C2 B2 A2 D1 C1 B1 A1 D0 C0 B0 A0
E D C B A
Y5 Y4 Y3 Y2 Y1
OPEN
OPEN
OPEN
NC
OPEN
B19 B18 B17 B16 B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
BINARY

TL/F/6561-9

FIGURE 2. BCD-to-Binary Converter for Six BCD Decades

MSD—Most significant decade
LSD—Least significant decade
Each rectangle represents a DM74184

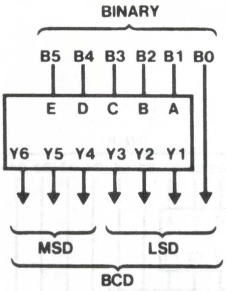
Typical Applications (Continued)


BCD
MSD
LSD
E D C B A
Y5 Y4 Y3 Y2 Y1
OPEN
B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
OPEN
BINARY

TL/F/6561-8

FIGURE 3. BCD-to-Binary Converter for Three BCD Decades

MSD—Most significant decade
LSD—Least significant decade
Each rectangle represents a DM74184


BINARY
B5 B4 B3 B2 B1 B0
E D C B A
Y6 Y5 Y4 Y3 Y2 Y1
MSD
LSD
BCD

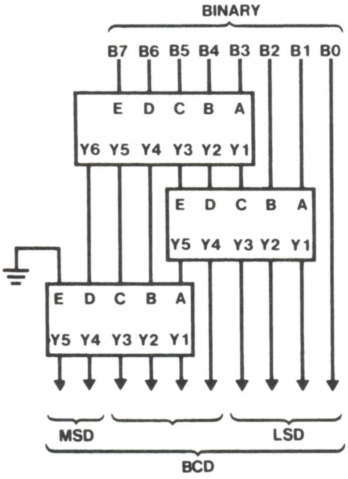
TL/F/6561-10

FIGURE 4. 6-Bit Binary-to-BCD Converter

MSD—Most significant decade
LSD—Least significant decade

Note A: Each rectangle represents a DM74185A.

Note B: All unused E inputs are grounded.


BINARY
B7 B6 B5 B4 B3 B2 B1 B0
E D C B A
Y6 Y5 Y4 Y3 Y2 Y1
E D C B A
Y5 Y4 Y3 Y2 Y1
E D C B A
Y5 Y4 Y3 Y2 Y1
MSD
LSD
BCD

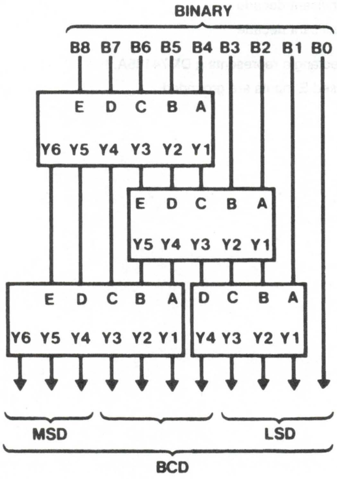
TL/F/6561-11

FIGURE 5. 8-Bit Binary-to-BCD Converter

MSD—Most significant decade
LSD—Least significant decade

Note A: Each rectangle represents a DM74185A.

Note B: All unused E inputs are grounded.


BINARY
B8 B7 B6 B5 B4 B3 B2 B1 B0
E D C B A
Y6 Y5 Y4 Y3 Y2 Y1
E D C B A
Y5 Y4 Y3 Y2 Y1
E D C B A
Y6 Y5 Y4 Y3 Y2 Y1
D C B A
Y4 Y3 Y2 Y1
MSD
LSD
BCD

TL/F/6561-12

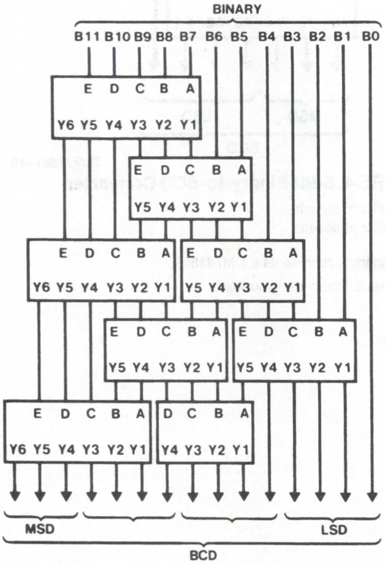
FIGURE 6. 9-Bit Binary-to-BCD Converter

MSD—Most significant decade
LSD—Least significant decade

Note A: Each rectangle represents a DM74185A.

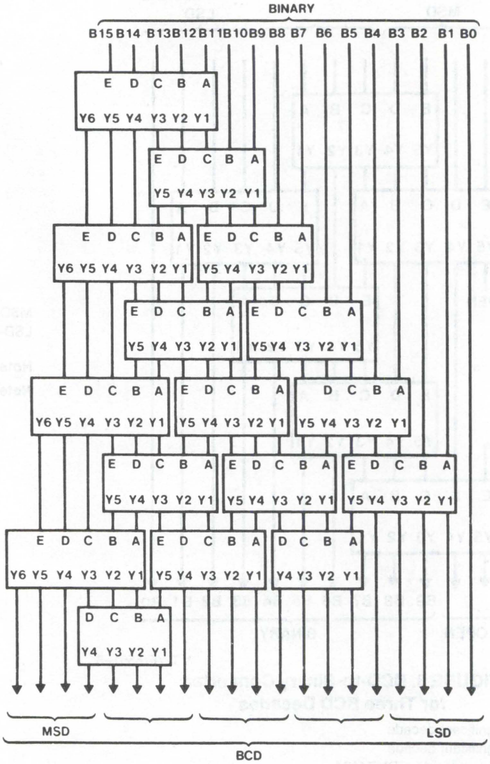
Note B: All unused E inputs are grounded.

Typical Applications (Continued)


BINARY
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
E D C B A
Y6 Y5 Y4 Y3 Y2 Y1
Y5 Y4 Y3 Y2 Y1
D C B A
Y4 Y3 Y2 Y1
MSD
LSD
BCD

TL/F/6561-13

FIGURE 7. 12-Bit Binary-to-BCD Converter (See Note B)


BINARY
B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
E D C B A
Y6 Y5 Y4 Y3 Y2 Y1
Y5 Y4 Y3 Y2 Y1
D C B A
Y4 Y3 Y2 Y1
MSD
LSD
BCD

TL/F/6561-14

FIGURE 8. 16-Bit Binary-to-BCD Converter (See Note B)

MSD—Most significant decade

LSD—Least significant decade

Note A: Each rectangle represents a DM74185A.

Note B: All unused E inputs are grounded.

National Semiconductor

54191/DM54191/DM74191 Synchronous Up/Down 4-Bit Binary Counter with Mode Control

General Description

This circuit is a synchronous, reversible, up/down counter. The 191 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

This counter is fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

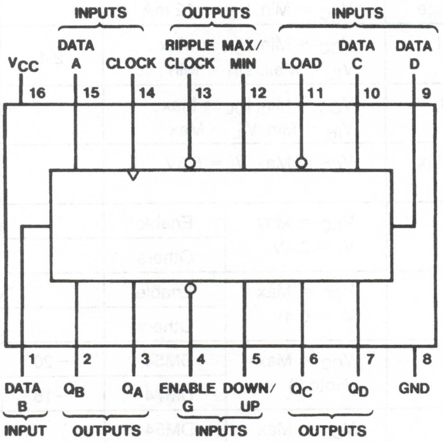
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications
- Alternate Military/Aerospace device (54191) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6562-1

Order Number 54191DMQB, 54191FMQB, DM54191J, DM54191W or DM74191N
See NS Package Number J16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54191			DM74191			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 4)		0		20	0		20	MHz
t_W	Pulse Width (Note 4)	Clock	25			25			ns
		Load	35			35			
t_{SU}	Data Setup Time (Note 4)		28			28			ns
t_H	Hold Time (Note 4)		0			0			ns
t_{REL}	Load Release Time (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Enable			120	µA
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Enable			−4.8	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−65	mA
			DM74	−18		−65	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		65	99	mA
			DM74		65	105	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

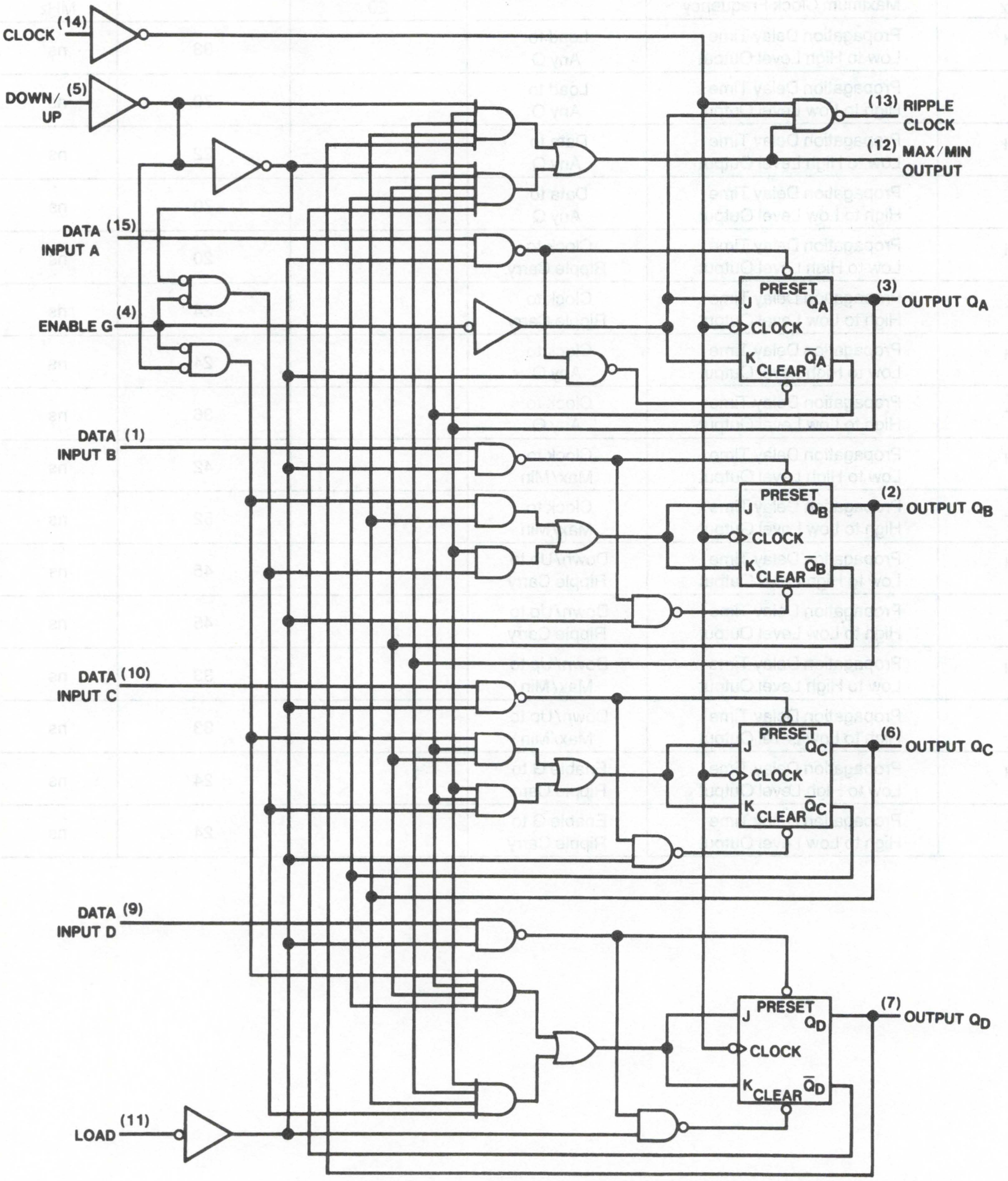
Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		70	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Any Q		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Any Q		70	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Max/Min		42	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Max/Min		52	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Down/Up to Ripple Carry		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Down/Up to Ripple Carry		45	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Down/Up to Max/Min		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Down/Up to Max/Min		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable G to Ripple Carry		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable G to Ripple Carry		24	ns

Logic Diagram

191 Binary Counter

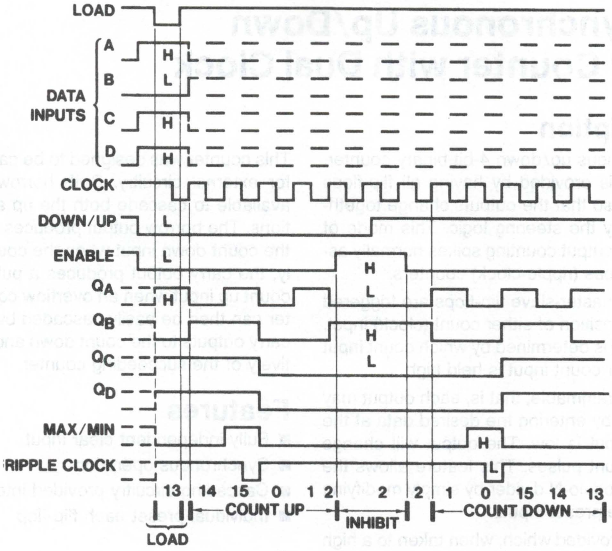

CLOCK (14)
DOWN/UP (5)
DATA INPUT A (15)
ENABLE G (4)
DATA INPUT B (1)
DATA INPUT C (10)
DATA INPUT D (9)
LOAD (11)
(13) RIPPLE CLOCK
(12) MAX/MIN OUTPUT
PRESET
J
K
CLOCK
CLEAR
Q_A
$\overline{Q}_A$
(3) OUTPUT Q_A
Q_B
$\overline{Q}_B$
(2) OUTPUT Q_B
Q_C
$\overline{Q}_C$
(6) OUTPUT Q_C
Q_D
$\overline{Q}_D$
(7) OUTPUT Q_D

TL/F/6562-2

Pin (16) = V_{CC}, Pin (8) = GND

Timing Diagrams

191 Decade Counter
Typical Load, Count, and Inhibit Sequences


LOAD
A
B
C
D
DATA INPUTS
H
L
H
H
CLOCK
DOWN/UP
L
ENABLE
L
H
Q_A
H
L
Q_B
H
Q_C
L
Q_D
MAX/MIN
H
RIPPLE CLOCK
L
13
14
15
0
1
2
2
2
1
0
15
14
13
LOAD
COUNT UP
INHIBIT
COUNT DOWN

TL/F/6562-3

National Semiconductor

DM54193 Synchronous Up/Down 4-Bit Binary Counter with Dual Clock

General Description

This circuit is a synchronous up/down 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

This counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counter to be used as modulo-N divider by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

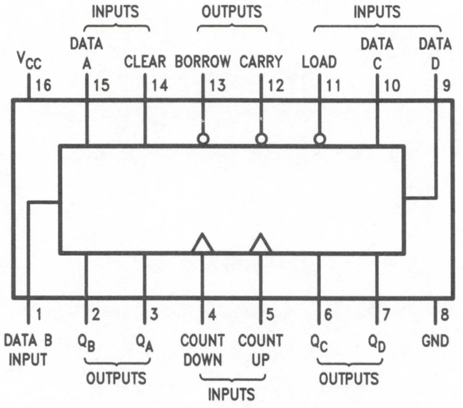
This counter was designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count up input when an overflow condition exists. The counter can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop

Connection Diagram

Dual-In-Line Package



TL/F/6563-1

Order Number DM54193J or DM54193W
See NS Package Number J16A or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				16	mA
f_{CLK}	Clock Frequency (Note 4)		0	25	20	MHz
t_W	Pulse Width (Note 4)	Clock Low	30			ns
		Clock, Clear High Load Low	20			
t_{SU}	Data Setup Time (Note 4)		20			ns
t_H	Hold Time (Note 4)		0			ns
T_A	Free Air Operating Temperature		−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−55	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)		65	89	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25° C.

Note 2: Not more than one output should be shorted at a time.

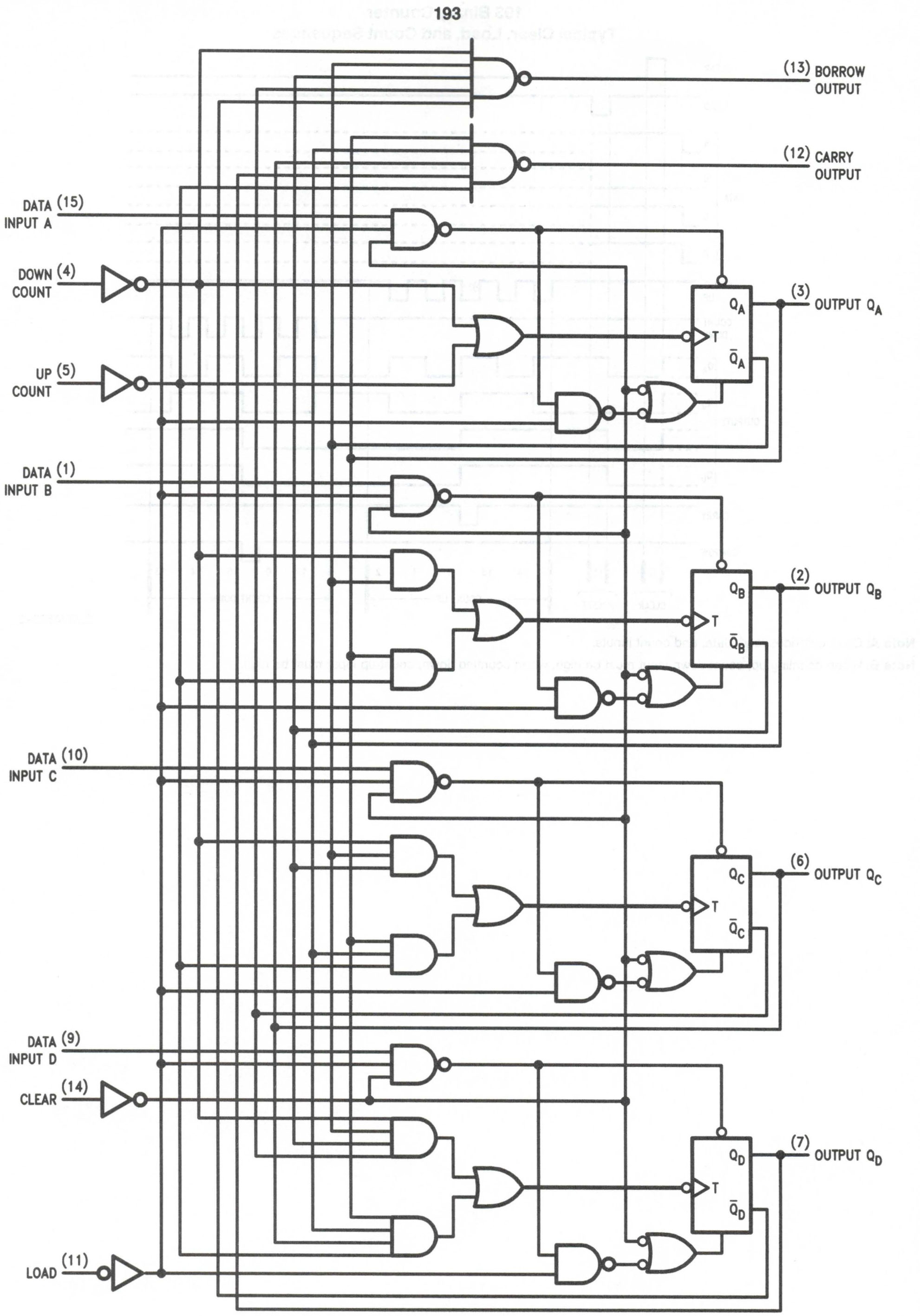
Note 3: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega, C_L = 15\ pF$ Min	Max	Units
f_{MAX}	Maximum Clock Frequency		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Count Up to Carry		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Count Up to Carry		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Count Down to Borrow		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Count Down to Borrow		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Either Count to Q		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Either Count to Q		47	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Q		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Q		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		35	ns

Logic Diagrams

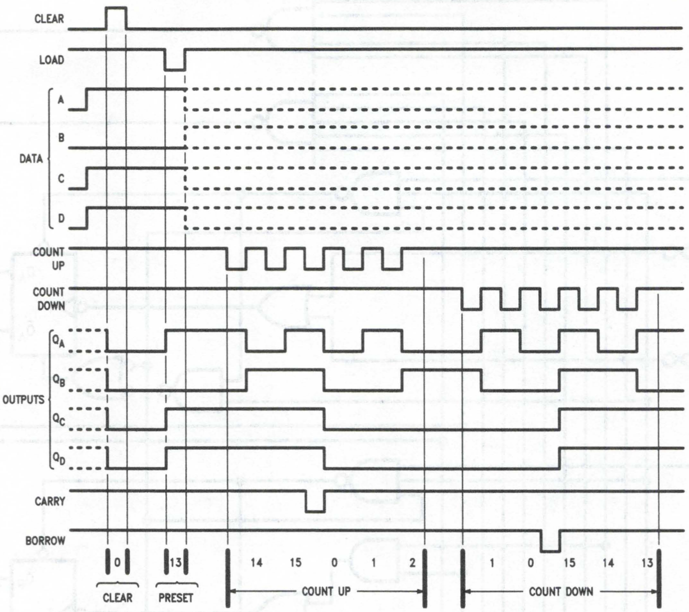

193
(13) BORROW OUTPUT
(12) CARRY OUTPUT
DATA INPUT A (15)
DOWN COUNT (4)
UP COUNT (5)
DATA INPUT B (1)
DATA INPUT C (10)
DATA INPUT D (9)
CLEAR (14)
LOAD (11)
Q_A
T
$\bar{Q}_A$
(3) OUTPUT Q_A
Q_B
T
$\bar{Q}_B$
(2) OUTPUT Q_B
Q_C
T
$\bar{Q}_C$
(6) OUTPUT Q_C
Q_D
T
$\bar{Q}_D$
(7) OUTPUT Q_D

TL/F/6563–2

Timing Diagram

193 Binary Counter

Typical Clear, Load, and Count Sequences


CLEAR
LOAD
DATA
A
B
C
D
COUNT UP
COUNT DOWN
OUTPUTS
Q_A
Q_B
Q_C
Q_D
CARRY
BORROW
0
13
14
15
0
1
2
1
0
15
14
13
CLEAR
PRESET
COUNT UP
COUNT DOWN

TL/F/6563-3

Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high, when counting down, count-up input must be high.

National Semiconductor

DM54194
4-Bit Bidirectional Universal Shift Registers

General Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register; it features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

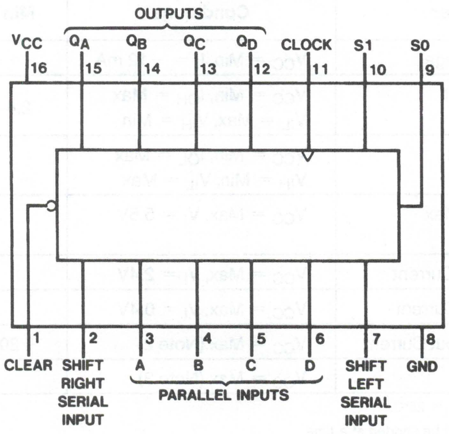
Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the DM54194/DM74194 should be changed only while the clock input is high.

Features

- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear
- Typical clock frequency 36 MHz
- Typical power dissipation 195 mW

Connection Diagram

Dual-In-Line Package



TL/F/6564–1

Order Number DM54194J or DM54194W
See NS Package Number J16A or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54194 Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.8	mA
I_{OL}	Low Level Output Current				16	mA
f_{CLK}	Clock Frequency (Note 4)		0	36	25	MHz
t_W	Pulse Width (Note 4)	Clock	20			ns
		Clear	20			
t_{SU}	Setup Time (Note 4)	Mode	30			ns
		Data	20			
t_H	Hold Time (Note 4)		0			ns
t_{REL}	Clear Release Time (Note 4)		25			ns
T_A	Free Air Operating Temperature		−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−57	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)		39	63	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CLOCK.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		30	ns

Function Table

Inputs										Outputs			
Clear	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S0		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

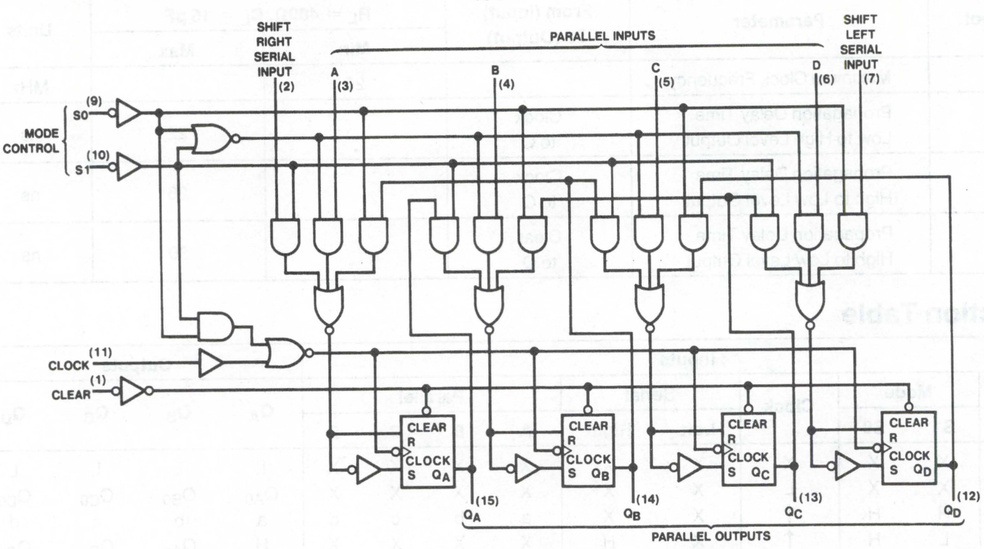
H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

↑ = Transition from low to high level; a, b, c, d = The level of steady state input at inputs A, B, C, or D, respectively

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent ↑ transition of the clock.

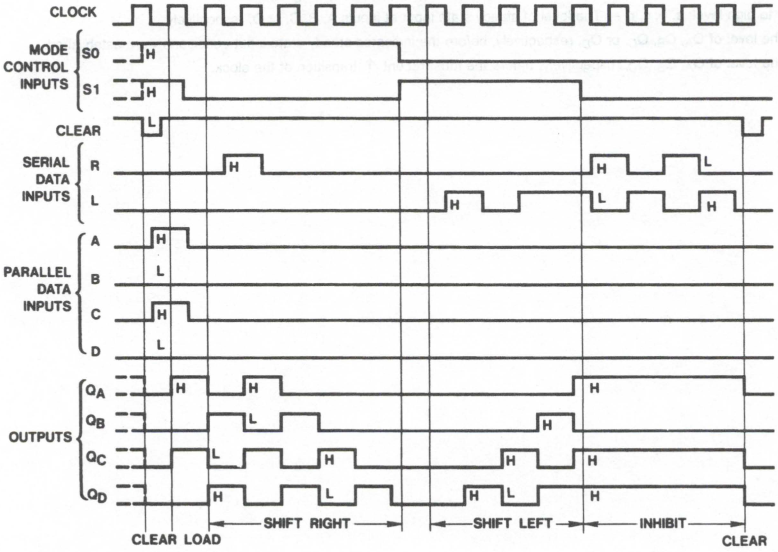
Logic Diagram


194
SHIFT RIGHT SERIAL INPUT
(2)
PARALLEL INPUTS
A (3)
B (4)
C (5)
D (6)
SHIFT LEFT SERIAL INPUT
(7)
MODE CONTROL
(9) S0
(10) S1
(11) CLOCK
(1) CLEAR
CLEAR R CLOCK S Q_A
CLEAR R CLOCK S Q_B
CLEAR R CLOCK S Q_C
CLEAR R CLOCK S Q_D
(15) Q_A
(14) Q_B
(13) Q_C
(12) Q_D
PARALLEL OUTPUTS

TL/F/6564-2

Timing Diagram

Typical Clear, Load, Right-Shift, Left-Shift, Inhibit and Clear Sequences


CLOCK
MODE CONTROL INPUTS
S0
S1
H
H
CLEAR
L
SERIAL DATA INPUTS
R
L
H
H
L
H
L
H
PARALLEL DATA INPUTS
A
B
C
D
H
L
H
L
OUTPUTS
Q_A
Q_B
Q_C
Q_D
H
H
H
L
H
L
H
H
H
H
L
H
CLEAR
LOAD
SHIFT RIGHT
SHIFT LEFT
INHIBIT
CLEAR

TL/F/6564-3

National Semiconductor

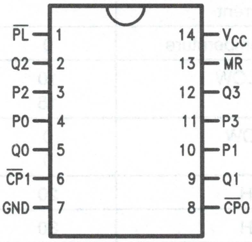
DM74197
Presettable Binary Counters

General Description

The '197 ripple counter contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. State changes are initiated by the falling edge of the clock. The '197 has a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuit usable as a programmable counter. The circuit can also be used as a 4-bit latch, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH.

Connection Diagram

Dual-In-Line Package



TL/F/9784-1

Order Number DM74197N
See NS Package Number N14A

Pin Names	Description
$\overline{CP0}$	÷ 2 Section Clock Input (Active Falling Edge)
$\overline{CP1}$	÷ 8 Section Clock Input (Active Falling Edge)
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
P0–P3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
Q0	÷ 2 Section Output*
Q1–Q3	÷ 8 Section Outputs

*Q0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP1}$ input.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74197			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.25	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n to $\overline{PL}$	10 15			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n to $\overline{PL}$	0 0			ns
t_w (H)	$\overline{CP}0$ Pulse Width HIGH	20			ns
t_w (H)	$\overline{CP}1$ Pulse Width HIGH	30			ns
t_w (L)	$\overline{PL}$ Pulse Width LOW	20			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	15			ns
t_{rec}	Recovery Time $\overline{PL}$ to $\overline{CP}_n$	20			ns
t_{rec}	Recovery Time $\overline{MR}$ to $\overline{CP}_n$	20			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 5.5V, $\overline{CP}_1$			1	mA
		V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−18		−57	mA
I_{CC}	Supply Current	V_{CC} = Max, All Inputs = GND			59	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

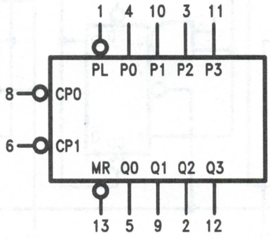
Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF		Units
		R_L = 400Ω		
		Min	Max	
f_{max}	Maximum Count Frequency at $\overline{CP}0$	50		MHz
f_{max}	Maximum Count Frequency at $\overline{CP}1$	25		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}0$ to Q0		12 15	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}1$ to Q1		18 21	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}1$ to Q2		36 42	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}1$ to Q3		54 63	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		24 38	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		33 36	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		37	ns

Logic Symbol



TL/F/9784-2

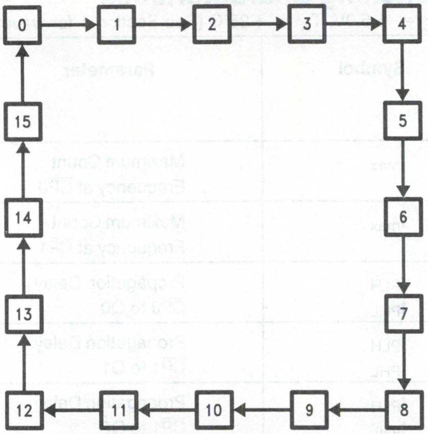
V_{CC} = Pin 14
GND = Pin 7

Mode Selection Table

Inputs			Response
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Q_n Forced LOW
H	L	X	$P_n \rightarrow Q_n$
H	H	↘	Count Up

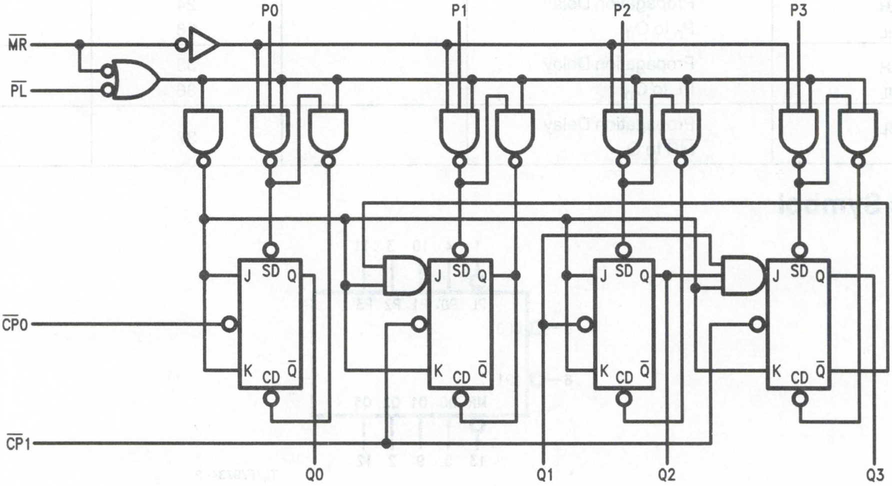
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

÷ 16 State Diagram


0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

TL/F/9784-3

Logic Diagram


P0
P1
P2
P3
$\overline{MR}$
$\overline{PL}$
$\overline{CP}0$
$\overline{CP}1$
J
SD
Q
K
CD
$\overline{Q}$
Q0
Q1
Q2
Q3

TL/F/9784-4

National Semiconductor

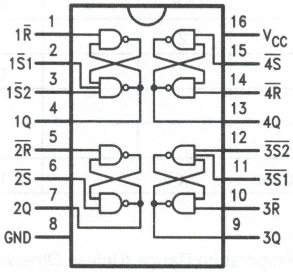
54279/DM74279 Quad Set-Reset Latch

General Description

This device contains four independent set-reset type flip-flops with one Q output each.

Connection Diagram

Dual-In-Line Package



TL/F/9785–1

Order Number 54279DMQB, 54279FMQB or DM74279N
NS Package Number J16A, N16E or W16A

Pin Names	Description
R_n	Reset Inputs (Active Low)
S_n	Set Inputs (Active Low)
Q	Outputs

Truth Table

Inputs			Output
S̄1	S̄2	R̄	Q
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
h = The output is HIGH as long as S̄1 or S̄2 is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54279			DM74279			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over Recommended Operating Free Air Temperature Range (Unless Otherwise Noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54	−20		−55	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max, $\overline{R}$ = 0V				30	mA

Switching Characteristics

Symbol	Parameter	54/DM74		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}$ to Q		22 15	ns
t_{PHL}	Propagation Delay $\overline{R}$ to Q		27	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

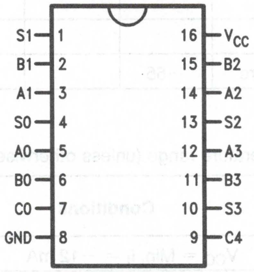
54283/DM74283
4-Bit Binary Full Adder (with Fast Carry)

General Description

The '283 high speed 4-bit binary full adders with internal carry lookahead accept two 4-bit binary words (A0–A3, B0–B3) and a Carry input (C0). They generate the binary Sum outputs (S0–S3) and the Carry output (C4) from the most significant bit. They operate with either active HIGH or active LOW operands (positive or negative logic).

Connection Diagram

Dual-In-Line Package



TL/F/9786-1

Order Number 54283DMQB, 54283FMQB or DM74283N
See NS Package Number J16A, N16E or W16A

Pin Names	Description
A0–A3	A Operand Inputs
B0–B3	B Operand Inputs
C0	Carry Input
S0–S3	Sum Outputs
C4	Carry Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54283			DM74283			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current at S_n	V_{CC} = Max (Note 2)	54	−20		−55	mA
			DM74	−20		−55	
I_{OS}	Short Circuit Output Current at C4	V_{CC} = Max (Note 2)	54	−20		−70	mA
			DM74	−18		−70	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max	54			99	mA
			DM74			110	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15$ pF, $R_L = 400\Omega$		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C0 or S_n		21 21	ns
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to S_n		24 24	ns
t_{PLH} t_{PHL}	Propagation Delay C0 to C4		14 16	ns
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to C4		14 16	ns

Functional Description

The '283 adds two 4-bit binary words (A plus B) plus the incoming carry C0. The binary sum appears on the Sum (S0–S3) and outgoing carry (C4 outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A0 + B0 + C0) + 2^1 (A1 + B1) + 2^2 (A2 + B2) + 2^3 (A3 + B3) = S0 + 2S1 + 4S2 + 8S3 + 16C4$$

Where (+) = plus

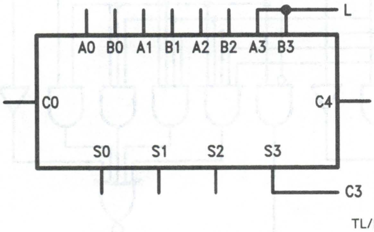
Interchanging inputs of equal weight does not affect the operation. Thus C0, A0, B0 can be arbitrarily assigned to pins 5, 6 and 7. Due to the symmetry of the binary add function, the '283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that if C0 is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

Example:

	C0	A0	A1	A2	A3	B0	B1	B2	B3	S0	S1	S2	S3	C4
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

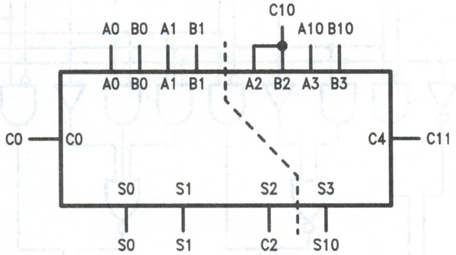
Active HIGH: 0 + 10 + 9 = 3 + 16   Active LOW: 1 + 5 + 6 = 12 + 0

Due to pin limitations, the intermediate carries of the '283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. *Figure a* shows a way of making a 3-bit adder. Tying the operand inputs of the fourth adder (A3, B3) LOW makes S3 dependent ony on, and equal to, the carry from the third adder. Using somewhat the same principle,*Figure b* shows a way of dividing the '283 into a 2-bit and a 1-bit adder. The third stage adder (A2, B2, S2) is used merely as a means of getting a carry (C10) signal into the fourth stage (via A2 and B2) and bringing out the carry from the second stage on S2. Note that as long as A2 and B2 are the same, whether HIGH or LOW, they do not infuence S2. Similarly, when A2 and B2 are the same the carry into the third stage does not influence they carry out of the third stage. *Figure c* shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S0, S1 and S2 present a binary number equal to the number of inputs I1–I5 that are true. *Figure d* shows one method of implementing a 5-input majority gate. When three or more of the inputs I1–I5 are true, the output M5 is true.



TL/F/9786-3

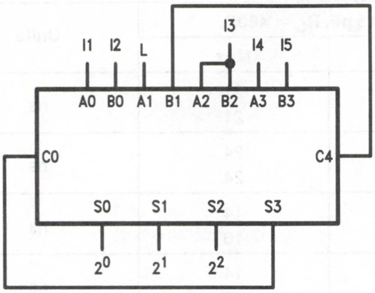
FIGURE a. 3-Bit Adder



TL/F/9786-4

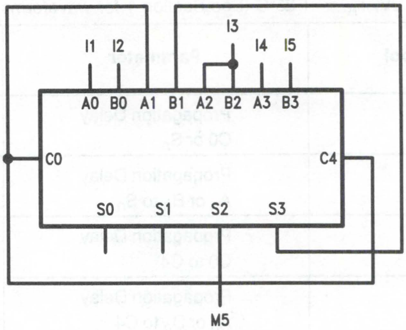
FIGURE b. 2-Bit and 1-Bit Adders

Functional Description (Continued)


I1
I2
L
I3
I4
I5
A0
B0
A1
B1
A2
B2
A3
B3
C0
C4
S0
S1
S2
S3
2^0
2^1
2^2

TL/F/9786-5

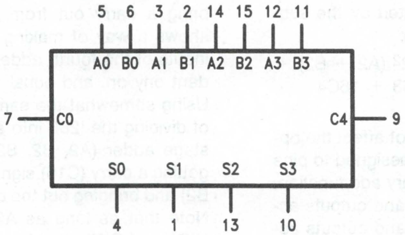
FIGURE c. 5-Input Encoder


I1
I2
I3
I4
I5
A0
B0
A1
B1
A2
B2
A3
B3
C0
C4
S0
S1
S2
S3
M5

TL/F/9786-6

FIGURE d. 5-Input Majority Gate

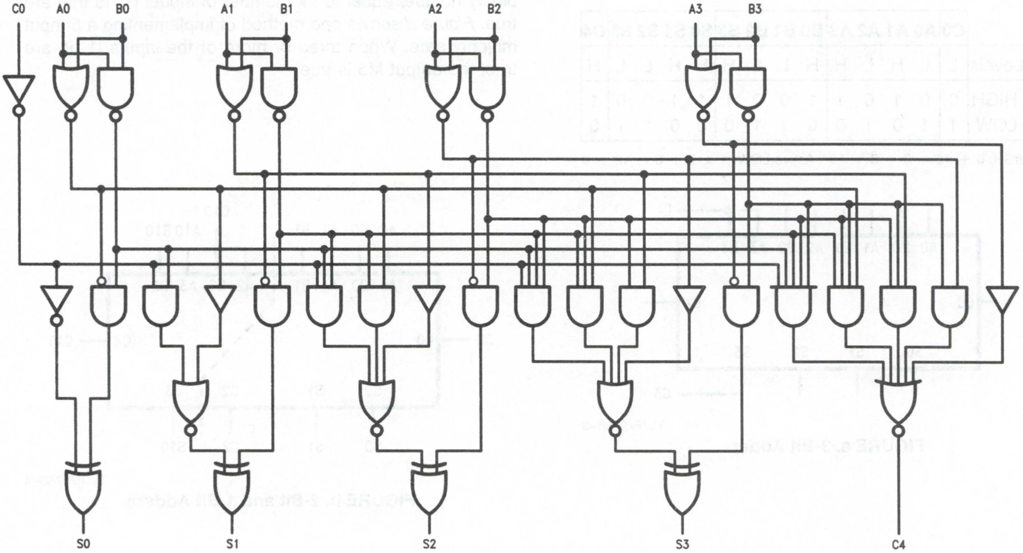
Logic Symbol


5
6
3
2
14
15
12
11
A0
B0
A1
B1
A2
B2
A3
B3
7
C0
C4
9
S0
S1
S2
S3
4
1
13
10

TL/F/9786-2

V_{CC} = Pin 16
GND = Pin 8

Logic Diagram


C0
A0
B0
A1
B1
A2
B2
A3
B3
S0
S1
S2
S3
C4

TL/F/9786-7

National Semiconductor

54298
Quad 2-Port Register (Multiplexer With Storage)

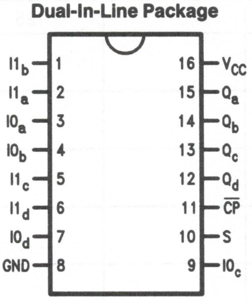
General Description

The '298 is a quad 2-port register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronous with the HIGH-to-LOW transition of the Clock input.

Features

- ■ Select from two data sources
- ■ Fully edge-triggered operation

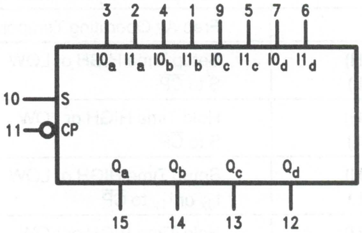
Connection Diagram


Dual-In-Line Package
I1b 1
I1a 2
I0a 3
I0b 4
I1c 5
I1d 6
I0d 7
GND 8
16 VCC
15 Qa
14 Qb
13 Qc
12 Qd
11 CP
10 S
9 I0c

TL/F/10215-1

Order Number 54298DMQB or 54298FMQB
See NS Package Number J16A or W16A

Logic Symbol


3 2 4 1 9 5 7 6
I0a I1a I0b I1b I0c I1c I0d I1d
10 S
11 CP
Qa Qb Qc Qd
15 14 13 12

TL/F/10215-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
S	Common Select Input
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)
I0a–I0d	Source 0 Data Inputs
I1a–I1d	Source 1 Data Inputs
Qa, Qd	Flip-Flop Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual operation.*

Recommended Operating Conditions

Symbol	Parameter	54298			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.8	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW S to $\overline{CP}$	25 25			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW S to $\overline{CP}$	0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW I_{0x} or I_{1x} to $\overline{CP}$	15 15			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW I_{0x} or I_{1x} to $\overline{CP}$	5.0 5.0			ns
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width HIGH or LOW	20 20			ns

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−57	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			65	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	$C_L = 15$ pF $R_L = 400\Omega$		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to Q_n		27 32	ns

Functional Description

This device is a high speed quad 2-port register. It selects four bits of data from two sources (ports) under the control of a Common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). The 4-bit output register is fully edge-triggered. The Data inputs (I_{nx}) and Select input (S) need be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

Truth Table

Inputs			Output
S	I_{0x}	I_{1x}	Q_x
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

l = LOW Voltage Level one setup time prior to the HIGH-to-LOWclock transition.

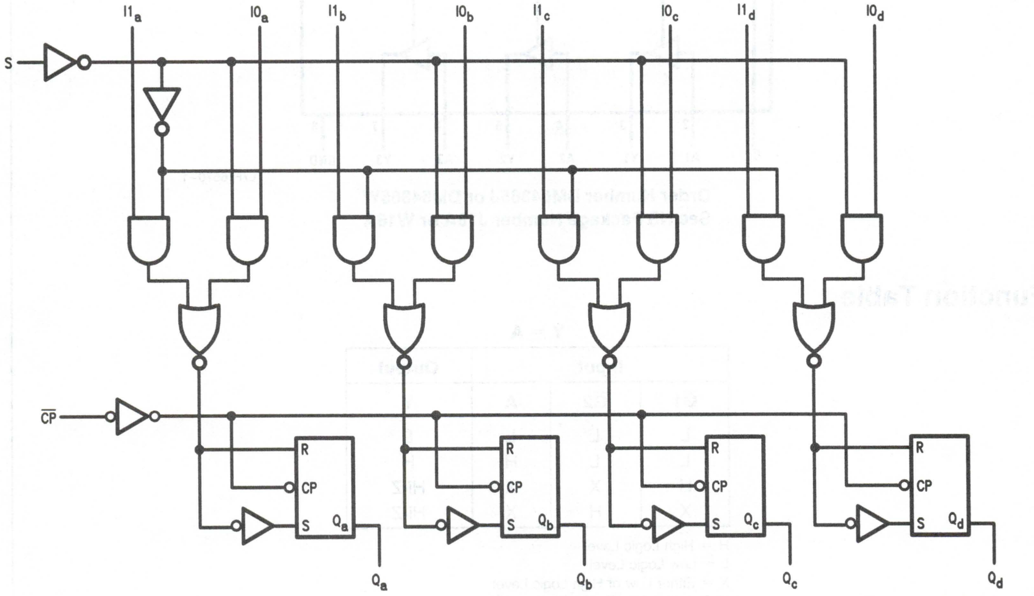
h = HIGH Voltage Level one setup time prior to the HIGH-to-LOW clock transition.

H = HIGH Voltage level

L = LOW Voltage level

X = Immaterial

Logic Diagram



TL/F/10215-3

National Semiconductor

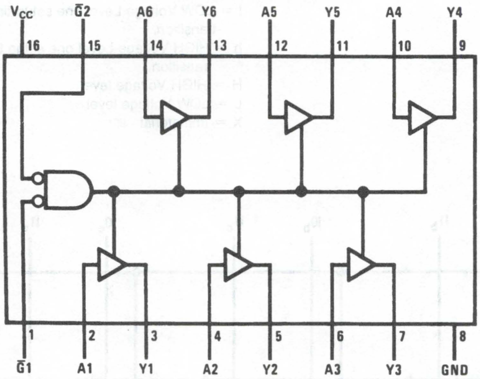
DM54365 Hex TRI-STATE® Buffers

General Description

This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6570–1

Order Number DM54365J or DM54365W
See NS Package Number J16A or W16A

Function Table

Y = A

Input			Output
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Hi-Z
X	H	X	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54365			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			32	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	A			−40	mA
		V_{CC} = Max V_I = 0.4V (Note 5)	A			−1.6	
		V_{CC} = Max V_I = 0.4V	$\overline{G}$			−1.6	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−40		−115	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			59	85	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the data inputs grounded, and the output controls at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs are at 0.4V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 400Ω				Units
		C_L = 5 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output				16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				22	ns
t_{PZH}	Output Enable Time to High Level Output				35	ns
t_{PZL}	Output Enable Time to Low Level Output				37	ns
t_{PHZ}	Output Disable Time from High Level Output		11			ns
t_{PLZ}	Output Disable Time from Low Level Output		27			ns

National Semiconductor

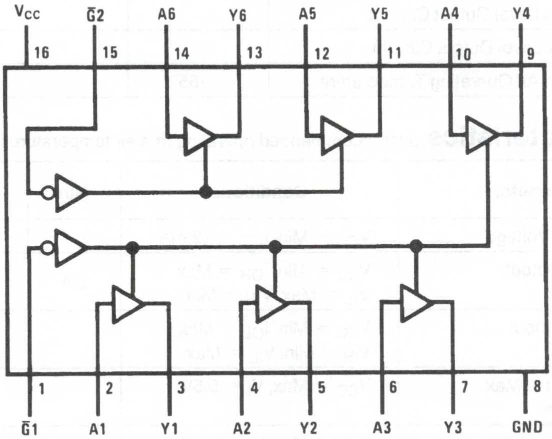
DM54367 Hex TRI-STATE® Buffers

General Description

This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a signficant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6572–1

Order Number DM54367J or DM54367W
See NS Package Number J16A or W16A

Function Table

Y = A

Input		Output
$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54367			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			32	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	A			−40	mA
		V_{CC} = Max V_I = 0.4V (Note 5)	A			−1.6	
		V_{CC} = Max V_I = 0.4V	$\overline{G}$			−1.6	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−40		−115	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			65	85	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the data inputs grounded and the output controls at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs are at 0.4V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 400\Omega$				Units
		$C_L = 5$ pF		$C_L = 50$ pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output				16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				22	ns
t_{PZH}	Output Enable Time to High Level Output				35	ns
t_{PZL}	Output Enable Time to Low Level Output				37	ns
t_{PHZ}	Output Disable Time from High Level Output		11			ns
t_{PLZ}	Output Disable Time from Low Level Output		27			ns

National Semiconductor

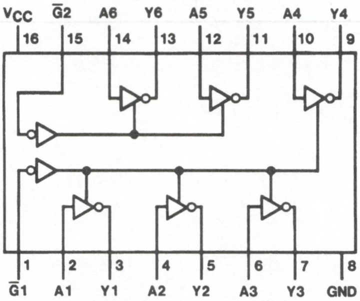
DM54368 Hex TRI-STATE® Inverting Buffers

General Description

This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6573-1

Order Number DM54368J or DM54368W
See NS Package Number J16A or W16A

Function Table

$Y = \overline{A}$

Inputs		Output
$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54368			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			32	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	A			−40	mA
		V_{CC} = Max V_I = 0.4V (Note 5)	A			−1.6	
		V_{CC} = Max V_I = 0.4V	$\overline{G}$			−1.6	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−40		−115	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			59	77	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the data inputs grounded, and the output controls at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs are at 0.4V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 400Ω				Units
		C_L = 5 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output				17	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				16	ns
t_{PZH}	Output Enable Time to High Level Output				35	ns
t_{PZL}	Output Enable Time to Low Level Output				37	ns
t_{PHZ}	Output Disable Time from High Level Output		11			ns
t_{PLZ}	Output Disable Time from Low Level Output		27			ns

National Semiconductor

DM7123 Quad 2-Input Data Selectors/Multiplexers

General Description

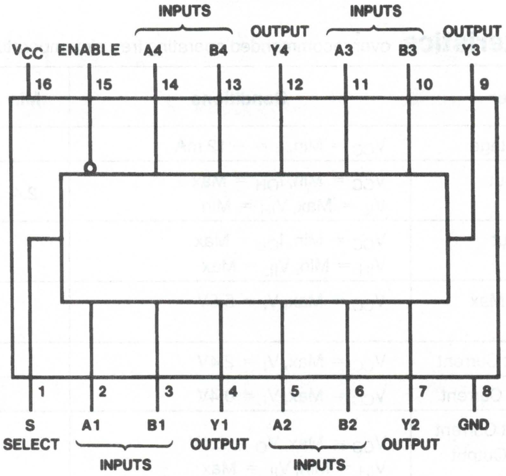
This device contains four 2-input multiplexers with common input select logic and common output disable circuitry. The DM7123 provides TRI-STATE® outputs. When the enable/strobe input is at a low logic level, the outputs of all devices are conventional TTL. However, when the enable/strobe input is raised to a high logic level, the outputs of the DM7123 go to the high-impedance third state. This device provides the designer with TRI-STATE and/or low power pin/pin replacements for the popular DM9322 and DM54/DM74157 multiplexers.

Features

- Pin equivalents popular DM9322 and DM54/DM74157 multiplexers
- Both conventional TTL and TRI-STATE outputs available
- Typical propagation delay 9.5 ns
- Typical power dissipation 200 mW

Connection Diagram

Dual-In-Line Package


INPUTS
OUTPUT
INPUTS
OUTPUT
VCC
ENABLE
A4
B4
Y4
A3
B3
Y3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
S
SELECT
A1
B1
Y1
OUTPUT
A2
B2
Y2
OUTPUT
GND
INPUTS
INPUTS

TL/F/6574-1

Order Number DM7123J or DM7123W
See NS Package Number J16A or W16A

Function Table

Enable	Select	Inputs A	Inputs B	Outputs Y
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Hi-Z

L = Low Logic Level, H = High Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range DM71	 −55°C to +125°C
Storage Temperature Range	−65°C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7123			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max			40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)		40	51	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

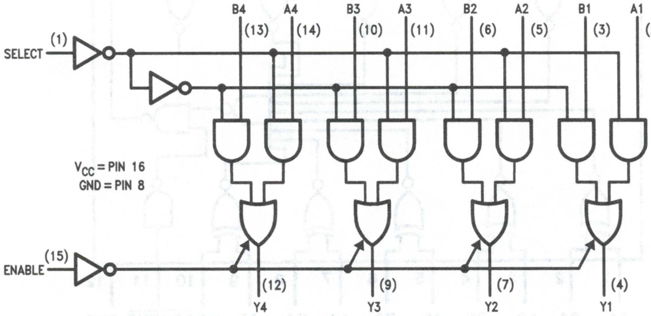
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the inputs grounded, and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω				Units
			C_L = 5 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output			4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output			5	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output			5	23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output			8	24	ns
t_{PZH}	Output Enable Time to High Level Output	Enable to Q			9	25	ns
t_{PZL}	Output Enable Time to Low Level Output	Enable to Q			10	30	ns
t_{PHZ}	Output Disable Time from High Level Output	Enable to Q	4	11			ns
t_{PLZ}	Output Disable Time from Low Level Output	Enable to Q	9	27			ns

Logic Diagram


B4
A4
B3
A3
B2
A2
B1
A1
(13)
(14)
(10)
(11)
(6)
(5)
(3)
(2)
SELECT
(1)
V_{CC} = PIN 16
GND = PIN 8
ENABLE
(15)
(12)
(9)
(7)
(4)
Y4
Y3
Y2
Y1

TL/F/6574–2

National Semiconductor

DM7130 Magnitude Comparators

General Description

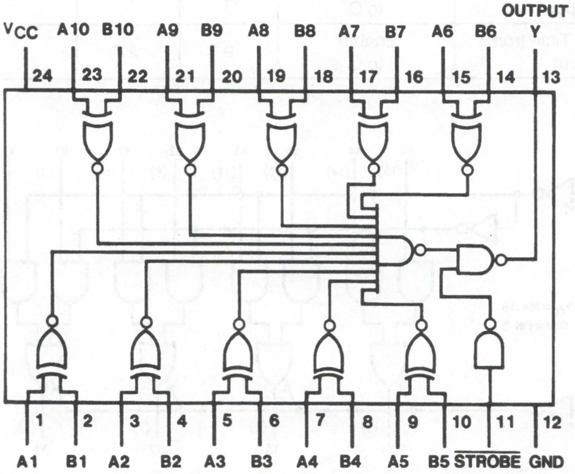
This device offers comparisons to determine equality between two binary words. The DM7130 compares two ten-bit words. A strobe override is provided. When the strobe is taken to a high logic level, the output is forced to a high logic level. The device also features open collector outputs for expansion.

Features

- Typical propagation delay 21 ns
- Typical power dissipation 240 mW
- Open-collector outputs for expansion

Connection Diagram

Dual-In-Line Package


OUTPUT
V_{CC}
A10
B10
A9
B9
A8
B8
A7
B7
A6
B6
Y
24
23
22
21
20
19
18
17
16
15
14
13
1
2
3
4
5
6
7
8
9
10
11
12
A1
B1
A2
B2
A3
B3
A4
B4
A5
B5
STROBE
GND

TL/F/6575–1

Order Number DM7130J
See NS Package Number J24A

Function Table

Condition	$\overline{\text{STROBE}}$ S	Output Y
A = B, A ≠ B	H	H
A = B	L	H
A ≠ B	L	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM71	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7130 Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Voltage			5.5	V
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IH} = Min			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)		48	70	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all inputs grounded and all outputs open.

National Semiconductor

DM7136 6-Bit Unified Bus Comparator with Open-Collector Outputs

General Description

The DM7136 compares two binary words of two-to-six bits in length and indicates matching (bit-for-bit) of the two words. Inputs for one word are 54/74 series-compatible TTL inputs, whereas those of the second word are high-impedance receivers driven by a terminated data bus. These bus inputs include 0.65V typical hysteresis which provides 1.4V noise immunity. The DM7136 has open-collector outputs which go to the high state upon equality and is expandable to n bits by collector-ORing. The device has an output latch which is strobe controlled.

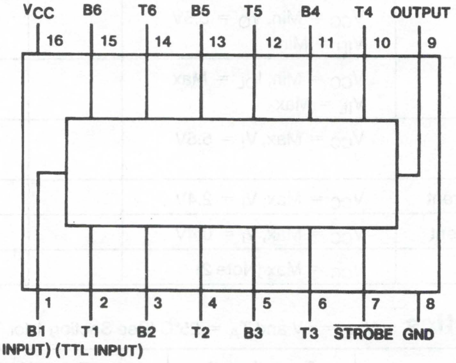
The transfer of information to the output occurs when the $\overline{\text{STROBE}}$ input goes from a logic "1" to a logic "0" state. Inputs may be changed while the $\overline{\text{STROBE}}$ is at the logic "1" level, without affecting the state of the output. These devices are useful as address comparators in computer systems utilizing unified data bus organization.

Features

- Low bus input current 15 μA typ
- High bus input noise immunity 1.4V typ
- Bus inputs comply with IEEE 488-1975
- TTL-compatible output
- Output latch provision

Connection Diagram

Dual-In-Line Package



TL/F/6577-1

Order Number DM7136J or DM7136W
See NS Package Number J16A or W16A

Function Table

Condition	$\overline{\text{STROBE}}$	Output DM71/8136
T = B, T ≠ B	H	Q_{N-1}*
T = B	L	H
T ≠ B	L	L

*Latched in previous state.

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM71	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7136			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{T+}	Positive-Going Input Threshold Voltage for Bus Inputs (Note 1)	1.4	1.75	2	V
V_{T-}	Negative-Going Input Threshold Voltage for Bus Inputs (Note 1)	0.9	1.1	1.35	V
V_{IH}	High Level Input Voltage for TTL and Strobe Inputs	2			V
V_{IL}	Low Level Input Voltage for TTL and Strobe Inputs			0.8	V
V_{OH}	High Level Output Voltage			5.5	V
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 5.5V	TTL			1	mA
			Strobe			2	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	TTL			40	μA
			Strobe			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	TTL			−1.6	mA
			Strobe			−2.4	
I_{IN}	Bus Input Current	V_I = 4V	V_{CC} = Max		15	50	μA
			V_{CC} = 0V		1	50	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			50	74	mA

Note 1: V_{CC} = 5V.

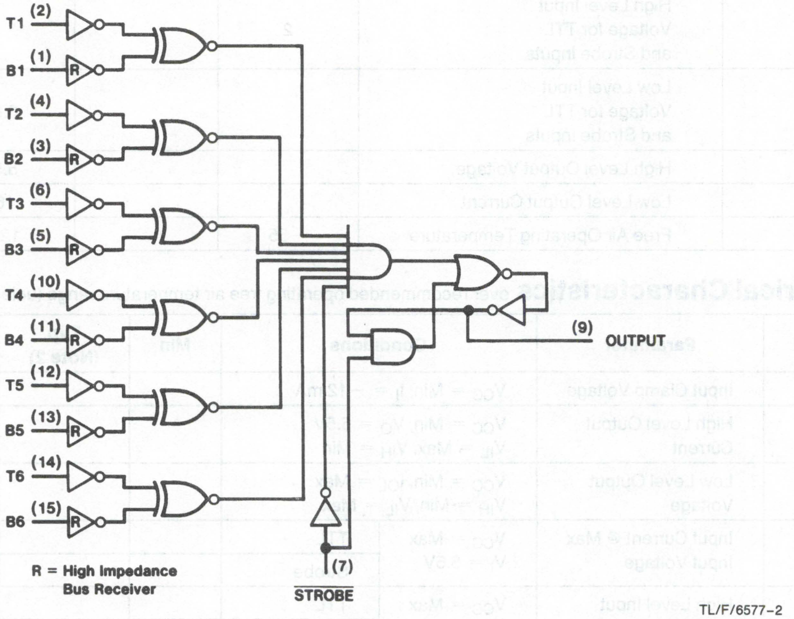
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	TTL to Output		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	TTL to Output		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Bus to Output		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Bus to Output		45	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		30	ns

Logic Diagram


(2)
T1
(1)
B1
R
(4)
T2
(3)
B2
R
(6)
T3
(5)
B3
R
(10)
T4
(11)
B4
R
(12)
T5
(13)
B5
R
(14)
T6
(15)
B6
R
(9)
OUTPUT
(7)
STROBE
R = High Impedance
Bus Receiver
TL/F/6577-2

National Semiconductor

DM7160 Magnitude Comparator

General Description

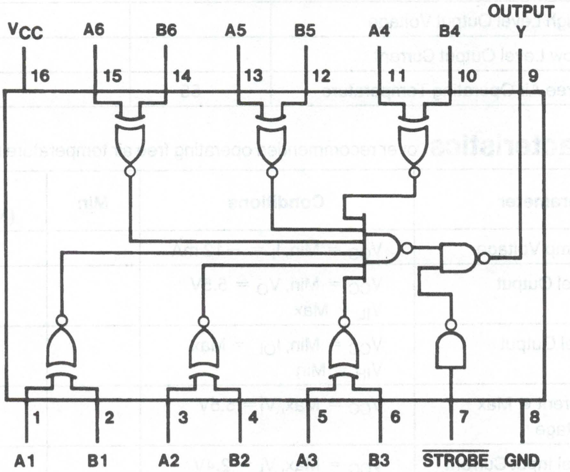
This device offers comparisons to determine equality between two binary words. The DM7160 compares two six-bit words. A strobe override is provided. When the strobe is taken to a high logic level, the output is forced to a high logic level. The device also features open-collector outputs for expansion.

Features

- Typical propagation delay 21 ns
- Typical power dissipation 205 mW
- Open-collector outputs for expansion

Connection Diagram

Dual-In-Line Package


OUTPUT
V_{CC}
A6
B6
A5
B5
A4
B4
Y
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
A1
B1
A2
B2
A3
B3
$\overline{\text{STROBE}}$
GND

TL/F/6578–1

Order Number DM7160J or DM7160W
See NS Package Number J16A or W16A

Function Table

Condition	STROBE S	Output Y
A = B, A ≠ B	H	H
A = B	L	H
A ≠ B	L	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM71	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7160 Min	DM7160 Nom	DM7160 Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Voltage			5.5	V
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			100	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)		41	60	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all inputs grounded and all outputs open.

National Semiconductor

9300/DM9300 4-Bit Parallel-Access Shift Register

General Description

The 9300 4-bit registers feature parallel inputs, parallel outputs, J$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load and shift (in direction Q_A toward Q_D).

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flops, and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

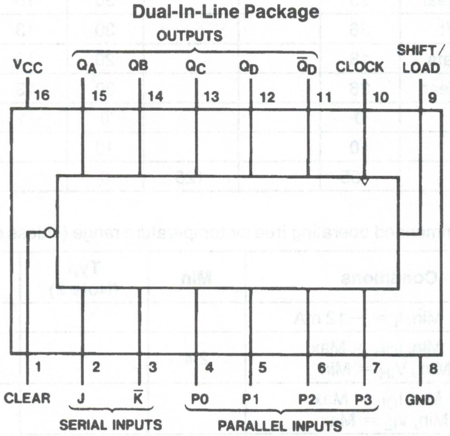
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J$\overline{K}$ inputs. These inputs permit the first stage to perform as a J$\overline{K}$, D or T-type flip-flop as shown in the function table.

These shift registers are fully compatible with most other TTL and DTL families. All inputs, including the clock, are buffered to lower the drive requirements to one normalized Series 54/74 load.

Features

- Fully buffered inputs
- Direct overriding clear
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Positive edge-triggered clocking
- J and $\overline{K}$ inputs to first stage
- Typical shift frequency—39 MHz

Connection Diagram



TL/F/6600–1

Order Number 9300DMQB, 9300FMQB or DM9300N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	P0	P1	P2	P3					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Bn}	$\overline{Q}_{Cn}$

H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
↑ = Transition from low-to-high level
a, b, c, d, = The level of steady state input at P0, P1, P2, or P3 respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent ↑ transition of the clock.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.48			−0.8	mA
I_{OL}	Low Level Output Current				9.6			16	mA
f_{CLK}	Clock Frequency (Note 5)		0		30	0		30	MHz
t_W	Pulse Width (Note 5)	Clock	17			16	11		ns
		Clear	25			30	15		
t_{SU}	Setup Time (Note 5)	S/L	36			30	13		ns
		Data	18			20	13		
		Clear	36			30	13		
t_H	Data Hold Time (Note 5)		0			0	−11		ns
t_{REL}	S/L Release Time (Notes 1 and 5)		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Input			40	μA
			CP Input			80	
			$\overline{PE}$ Input			92	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Input			−1.6	mA
			CP Input			−3.2	
			$\overline{PE}$ Input			−3.7	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	MIL	−20		−80	mA
			COM	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)	MIL			86	mA
			COM			92	

Note 1: RELEASE TIME: $t_{RELEASE}$ is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) *not* to respond.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, SHIFT/LOAD grounded, and 4.5V applied to J, K, and data inputs, I_{CC} is measured by applying momentary ground, then 4.5V to CLEAR, and then to CLOCK.

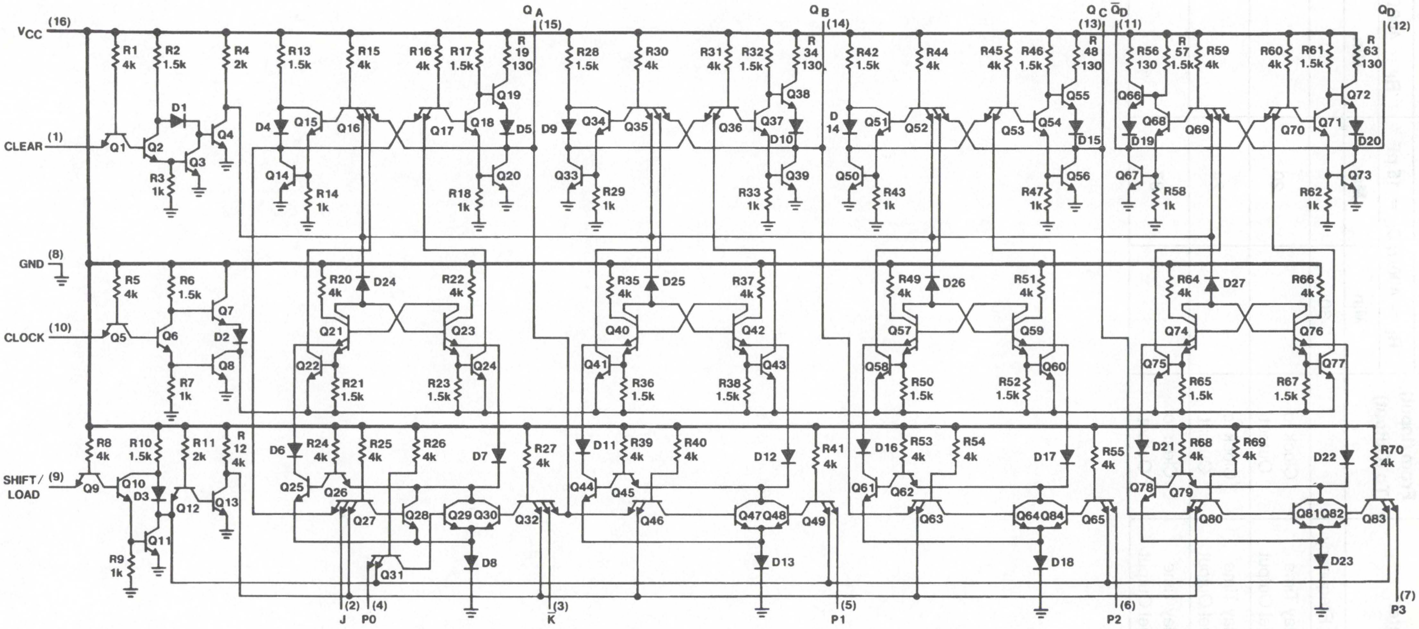
Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Military $R_L = 400\Omega, C_L = 15$ pF		Commercial $R_L = 400\Omega, C_L = 15$ pF		Units
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		20		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		24		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		37		30	ns

Schematic Diagram

DM9300


V_CC (16)
CLEAR (1)
GND (8)
CLOCK (10)
SHIFT/ LOAD (9)
Q_A (15)
Q_B (14)
Q_C (13)
Q̄_D (11)
Q_D (12)
(2) J
(4) P0
(3) K̄
(5) P1
(6) P2
(7) P3
R1 4k
R2 1.5k
R3 1k
R4 2k
R5 4k
R6 1.5k
R7 1k
R8 4k
R9 1k
R10 1.5k
R11 2k
R12 4k
R13 1.5k
R14 1k
R15 4k
R16 4k
R17 1.5k
R18 1k
R19 130
R20 4k
R21 1.5k
R22 4k
R23 1.5k
R24 4k
R25 4k
R26 4k
R27 4k
R28 1.5k
R29 1k
R30 4k
R31 4k
R32 1.5k
R33 1k
R34 130
R35 4k
R36 1.5k
R37 4k
R38 1.5k
R39 4k
R40 4k
R41 4k
R42 1.5k
R43 1k
R44 4k
R45 4k
R46 1.5k
R47 1k
R48 130
R49 4k
R50 1.5k
R51 4k
R52 1.5k
R53 4k
R54 4k
R55 4k
R56 130
R57 1.5k
R58 1k
R59 4k
R60 4k
R61 1.5k
R62 1k
R63 130
R64 4k
R65 1.5k
R66 4k
R67 1.5k
R68 4k
R69 4k
R70 4k
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q20 Q21 Q22 Q23 Q24 Q25 Q26 Q27 Q28 Q29 Q30 Q31 Q32 Q33 Q34 Q35 Q36 Q37 Q38 Q39 Q40 Q41 Q42 Q43 Q44 Q45 Q46 Q47 Q48 Q49 Q50 Q51 Q52 Q53 Q54 Q55 Q56 Q57 Q58 Q59 Q60 Q61 Q62 Q63 Q64 Q65 Q66 Q67 Q68 Q69 Q70 Q71 Q72 Q73 Q74 Q75 Q76 Q77 Q78 Q79 Q80 Q81 Q82 Q83 Q84

TL/F/6600-2

National Semiconductor

9301/DM9301
1-of-10 Decoders

General Description

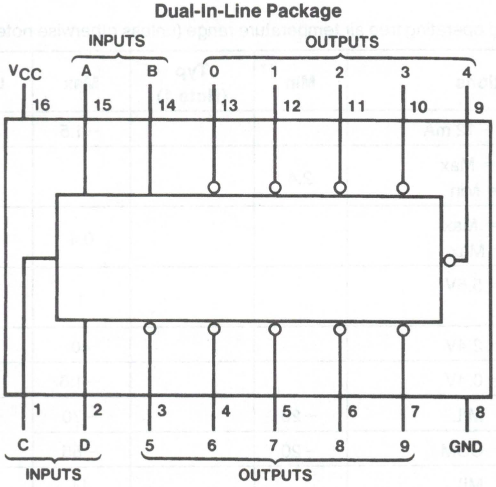
These BCD-to-decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain "OFF" for all invalid input conditions.

These circuits provide familiar TTL inputs and outputs which are compatible for use with other TTL and DTL circuits. DC noise margins are typically 1V and power dissipation is typically 125 mW. The diode-clamped, buffered inputs represent only one normalized Series 54/74 load.

Features

- Direct replacement for Signetics 8252
- Diode-clamped inputs
- All outputs are high for invalid BCD input conditions
- Typical power dissipation 125 mW
- Typical propagation delay 20 ns

Connection Diagram



TL/F/6601-1

Order Number 9301DMQB, 9301FMQB or DM9301N
See NS Package Number J16A, N16E or W16A

Function Table

No.	BCD Inputs				Decimal Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
I	H	L	H	L	H	H	H	H	H	H	H	H	H	H
N	H	L	H	H	H	H	H	H	H	H	H	H	H	H
V	H	H	L	L	H	H	H	H	H	H	H	H	H	H
A	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
I	H	H	H	H	H	H	H	H	H	H	H	H	H	H
D														

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	$-55°C$ to $+125°C$
Commercial	0°C to 70°C
Storage Temperature Range	$-65°C$ to $+150°C$

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			-0.8			-0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	-55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA				-1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				-1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	-20		-70	mA
			COM	-20		-55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	MIL			44	mA
			COM		25	41	

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

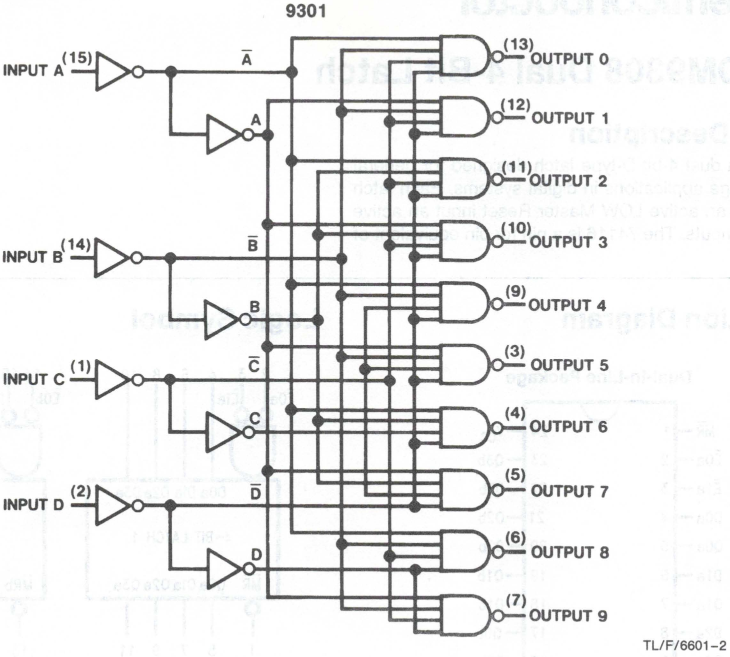
Symbol	Parameter	Conditions	Military		Commercial		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		35		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			30		30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the outputs open and all inputs grounded.

Logic Diagram


9301
INPUT A (15)
INPUT B (14)
INPUT C (1)
INPUT D (2)
$\overline{A}$
A
$\overline{B}$
B
$\overline{C}$
C
$\overline{D}$
D
(13) OUTPUT 0
(12) OUTPUT 1
(11) OUTPUT 2
(10) OUTPUT 3
(9) OUTPUT 4
(3) OUTPUT 5
(4) OUTPUT 6
(5) OUTPUT 7
(6) OUTPUT 8
(7) OUTPUT 9
TL/F/6601-2

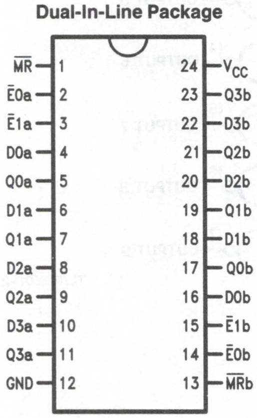
National Semiconductor

9308/DM9308 Dual 4-Bit Latch

General Description

The 9308 is a dual 4-bit D-type latch designed for general purpose storage applications in digital systems. Each latch contains both an active LOW Master Reset input an active LOW Enable inputs. The 74116 is a pin for pin equivalent of the 9308.

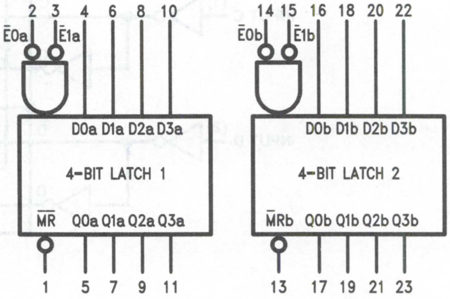
Connection Diagram


Dual-In-Line Package
$\overline{MR}$ 1
$\overline{E}$0a 2
$\overline{E}$1a 3
D0a 4
Q0a 5
D1a 6
Q1a 7
D2a 8
Q2a 9
D3a 10
Q3a 11
GND 12
24 V_{CC}
23 Q3b
22 D3b
21 Q2b
20 D2b
19 Q1b
18 D1b
17 Q0b
16 D0b
15 $\overline{E}$1b
14 $\overline{E}$0b
13 $\overline{MR}$b

TL/F/10208–1

Order Number 9308DMQB, 9308FMQB or DM9308N
See NS Package Number J24A, N24A or W24C

Logic Symbol


2
3
4
6
8
10
$\overline{E}$0a
$\overline{E}$1a
D0a D1a D2a D3a
4-BIT LATCH 1
$\overline{MR}$
Q0a Q1a Q2a Q3a
1
5
7
9
11
14
15
16
18
20
22
$\overline{E}$0b
$\overline{E}$1b
D0b D1b D2b D3b
4-BIT LATCH 2
$\overline{MR}$b
Q0b Q1b Q2b Q3b
13
17
19
21
23

TL/F/10208–2

V_{CC} = Pin 24
GND = Pin 12

Pin Names	Description
D_{0a}–D_{3a} D_{0b}–D_{3b}	Parallel Latch Inputs
$\overline{E}_{0a}$, $\overline{E}_{1a}$, $\overline{E}_{0b}$, $\overline{E}_{1b}$	AND Enable Inputs (Active LOW)
$\overline{MR}_a$, $\overline{MR}_b$	Master Reset Inputs (Active LOW)
$\overline{Q}_{0a}$–$\overline{Q}_{3a}$ $\overline{Q}_{0b}$–$\overline{Q}_{3b}$	Parallel Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
COM	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H)	Setup Time HIGH, D_n to $\overline{E}_n$	6			10			ns
t_h (H)	Hold Time HIGH, D_n to $\overline{E}_n$	4			−2.0			ns
t_s (L)	Setup Time LOW, D_n to $\overline{E}_n$	10			12			ns
t_h (L)	Hold Time LOW, D_n to $\overline{E}_n$	4			8			ns
t_w (L)	$\overline{E}_n$ Pulse Width LOW	18			18			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	18			18			ns
t_{rec}	Recovery Time, $\overline{MR}$ to $\overline{E}_n$	10			8			ns

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−70	mA
			COM	−20		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				100	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Functional Description

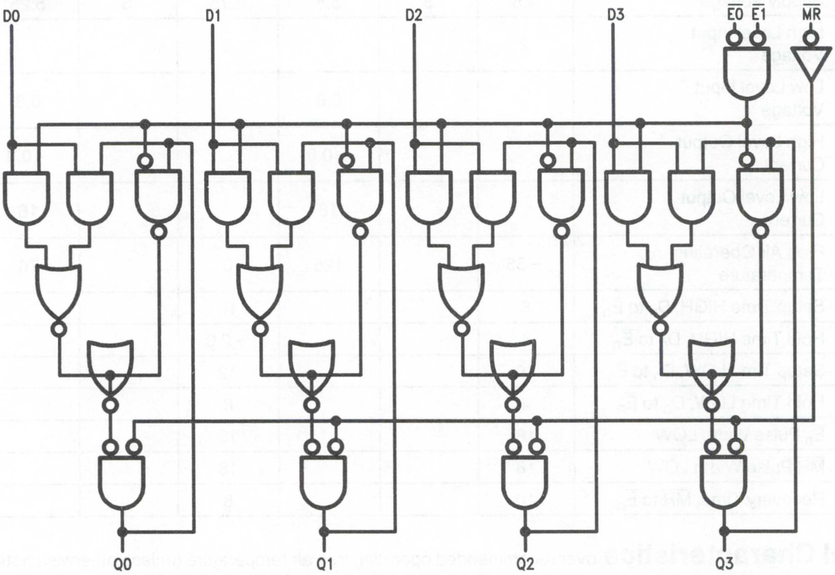
Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input. The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the Master Reset input.

Truth Table

$\overline{MR}$	$\overline{E0}$	$\overline{E1}$	D	Qn	Operation
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Qn−1	Hold
H	H	L	X	Qn−1	Hold
H	H	H	X	Qn−1	Hold
L	X	X	X	L	Reset

Q_{n-1} = Previous Output State
Q_n = Present Output State
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/10208-3

Switching Characteristics V_{CC} = +5.0V, T_A = +25°C (See Section 1 for test waveforms and output load.)

Symbol	Parameter	9308 C_L = 15 pF R_L = 400Ω Min	Max	Units
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$n to Qn		30 22	ns
t_{PLH} t_{PHL}	Propagation Delay Dn to Qn		15 18	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Qn		22	ns

National Semiconductor

9309/DM9309 Dual 4-Bit Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverter/drivers to supply full complementary, on-chip, binary decoded data selection.

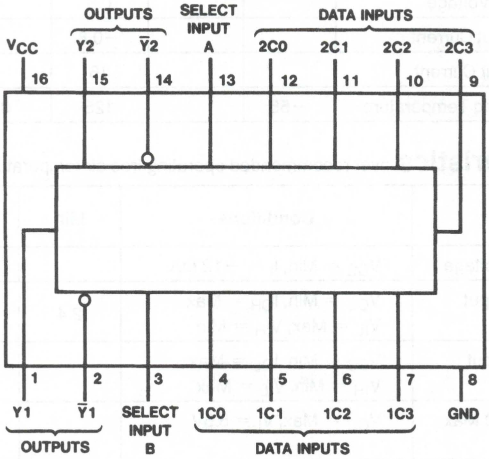
The 9309/DM9309 contains two separate 4-bit multiplexers with complementary Y and $\overline{Y}$ outputs; however, the two sections have common address select inputs.

Features

- Complementary outputs
- Dual one-of-four data selectors

Connection Diagram

Dual-In-Line Package


OUTPUTS
SELECT INPUT
DATA INPUTS
VCC
Y2
Y̅2
A
2C0
2C1
2C2
2C3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
Y1
Y̅1
SELECT INPUT B
1C0
1C1
1C2
1C3
GND
OUTPUTS
DATA INPUTS

TL/F/6602–1

Order Number 9309DMQB, 9309FMQB or DM9309N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs						Outputs	
Select		Data				Y	$\overline{Y}$
B	A	C0	C1	C2	C3		
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	H	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

Select inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -12\text{ mA}$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$		2.4	3.4		V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}, V_{IL} = \text{Max}$			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5V$				1	mA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4V$				40	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4V$				−1.6	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	MIL	−20		−70	mA
			COM	−30		−85	
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 3)			27	44	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

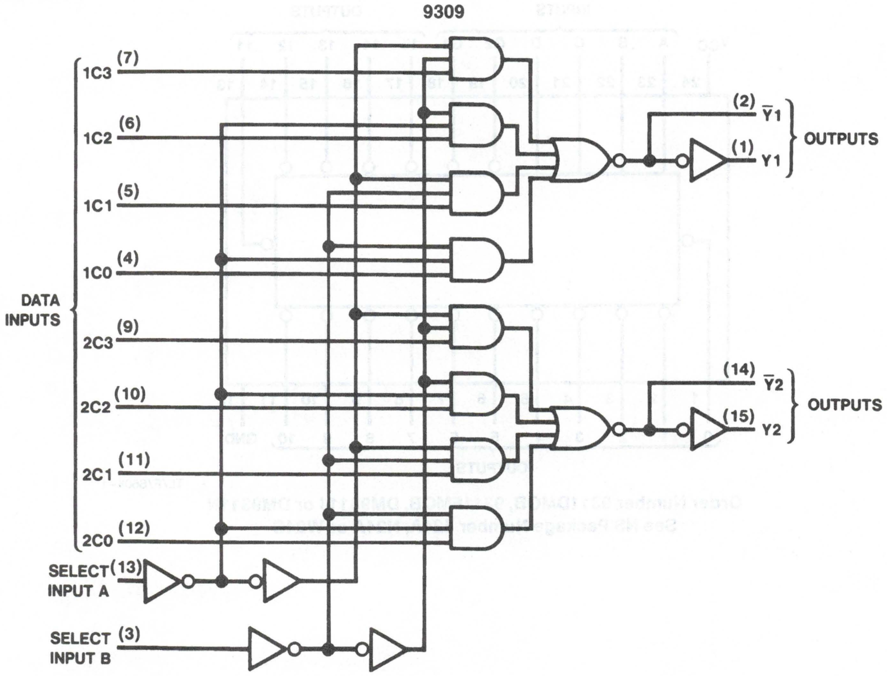
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the outputs open and all inputs at 4.5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Military		Commercial		Units
			R_L = 400Ω, C_L = 15 pF				
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		29		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		27		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to $\overline{Y}$		21		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to $\overline{Y}$		21		29	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		20		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		21		34	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to $\overline{Y}$		12		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to $\overline{Y}$		13		13	ns

Logic Diagram


9309
1C3 (7)
1C2 (6)
1C1 (5)
1C0 (4)
DATA INPUTS
2C3 (9)
2C2 (10)
2C1 (11)
2C0 (12)
SELECT INPUT A (13)
SELECT INPUT B (3)
(2) $\overline{Y}$1
(1) Y1
OUTPUTS
(14) $\overline{Y}$2
(15) Y2
OUTPUTS

TL/F/6602-2

National Semiconductor

9311/DM9311 4-Line to 16-Line Decoders/Demultiplexers

General Description

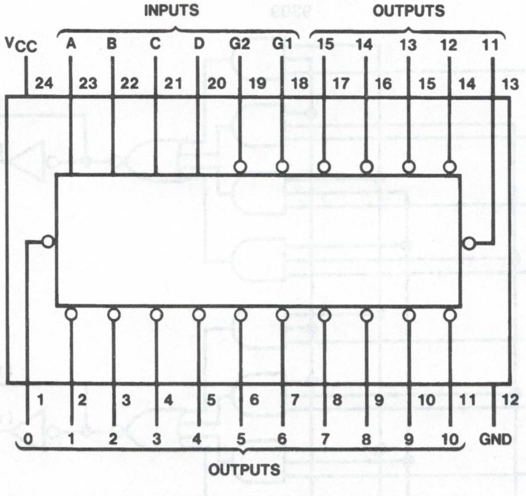
Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Pin for pin with popular DM54154/74154
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay 19 ns
- Typical power dissipation 170 mW
- Alternate Military/Aerospace device (9311) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6604-1

Order Number 9311DMQB, 9311FMQB, DM9311J or DM9311N
See NS Package Number J24A, N24A or W24C

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.25	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−55	mA
			COM	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	MIL		34	49	mA
			COM		34	56	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF Min	 Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		27	ns

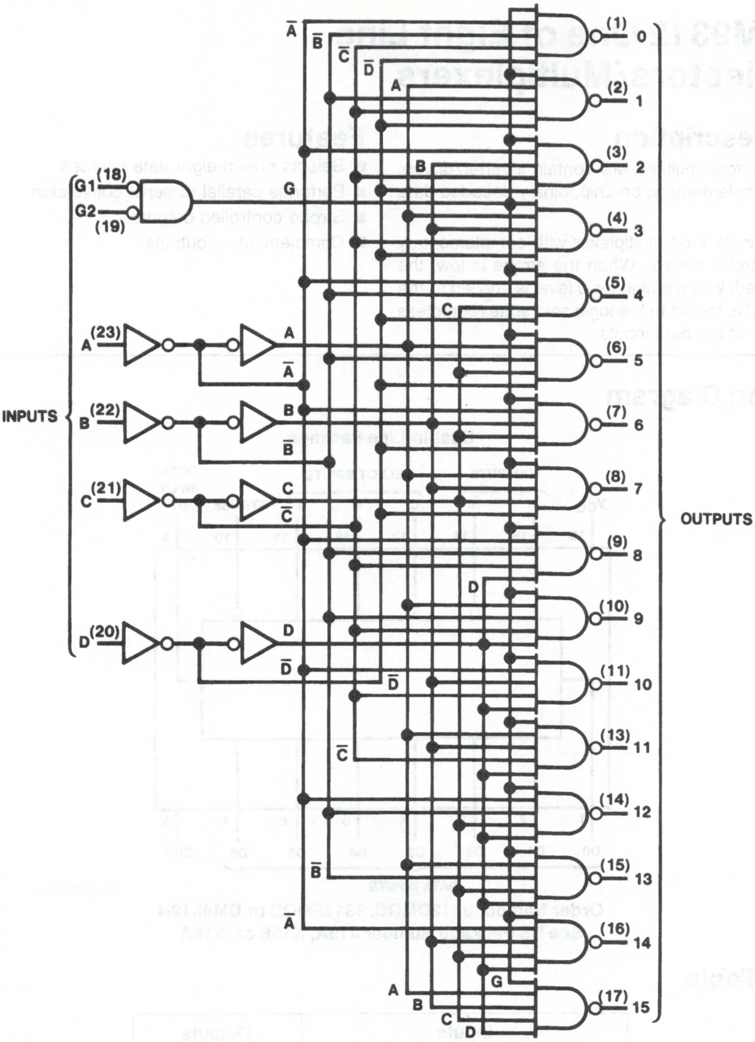
Function Table

Inputs						Outputs															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care.

Logic Diagram

DM9311


INPUTS
G1 (18)
G2 (19)
G
A (23)
B (22)
C (21)
D (20)
A
Ā
B
B̄
C
C̄
D
D̄
OUTPUTS
(1) 0
(2) 1
(3) 2
(4) 3
(5) 4
(6) 5
(7) 6
(8) 7
(9) 8
(10) 9
(11) 10
(13) 11
(14) 12
(15) 13
(16) 14
(17) 15

TL/F/6604-2

National Semiconductor

9312/DM9312 One of Eight Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverter/drivers to supply full complementary, on-chip, binary decoded data selection.

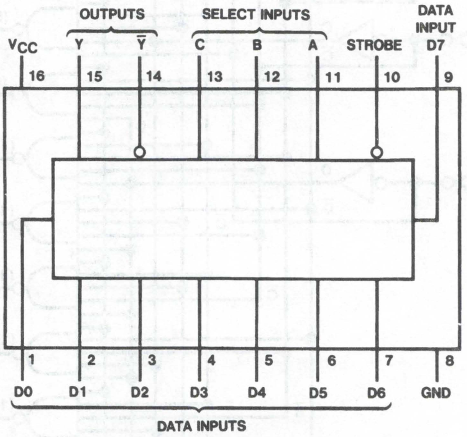
The 9312 is a single 8-bit multiplexer with complementary outputs and a strobe control. When the strobe is low, the function is enabled. When a high logic level is applied to the strobe, the output is forced to the logic zero state regardless of the logic level of the data inputs.

Features

- Selects one-of-eight data sources
- Performs parallel to serial conversion
- Strobe controlled outputs
- Complementary outputs

Connection Diagram

Dual-In-Line Package


OUTPUTS
SELECT INPUTS
DATA INPUT
V_{CC}
Y
$\overline{Y}$
C
B
A
STROBE
D7
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
D0
D1
D2
D3
D4
D5
D6
GND
DATA INPUTS

TL/F/6605-1

Order Number 9312DMQB, 9312FMQB or DM9312N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs				Outputs	
Select			Strobe	Y	$\overline{Y}$
C	B	A	G		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care.

D0, D1 . . . D7 = The level of the respective D input.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−70	mA
			COM	−30		−85	
I_{CC}	Supply Current	V_{CC} = Max, (Note 3)			27	44	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

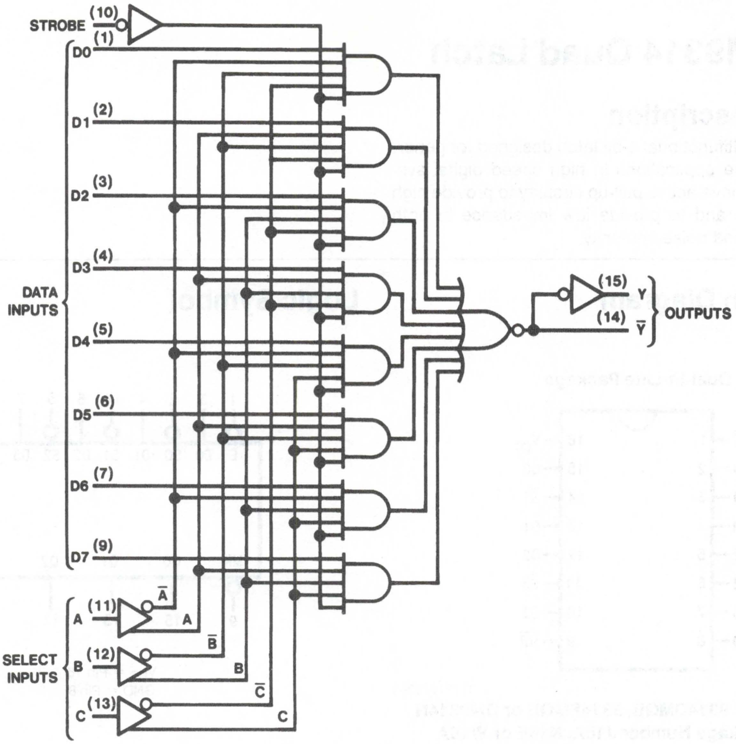
Note 3: I_{CC} is measured with the STROBE and DATA SELECT inputs 4.5V and all other inputs and outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Military		Commercial		Units
			R_L = 400Ω, C_L = 15 pF				
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Selectz to Y		34		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		34		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to $\overline{Y}$		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to $\overline{Y}$		26		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		24		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		24		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to $\overline{Y}$		14		13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to $\overline{Y}$		16		13	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		30		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		30		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to $\overline{Y}$		20		19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to $\overline{Y}$		23		21	ns

Logic Diagram

9312


STROBE
(10)
(1)
D0
(2)
D1
(3)
D2
(4)
D3
DATA INPUTS
(5)
D4
(6)
D5
(7)
D6
(9)
D7
(11)
A
$\overline{A}$
A
SELECT INPUTS
(12)
B
$\overline{B}$
B
(13)
C
$\overline{C}$
C
(15)
Y
(14)
$\overline{Y}$
OUTPUTS

TL/F/6605-2

National Semiconductor

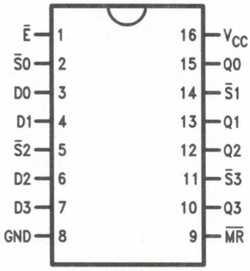
9314/DM9314 Quad Latch

General Description

The '9314 is a multifunctional 4-bit latch designed for general purpose storage applications in high speed digital systems. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good noise immunity.

Connection Diagram

Dual-In-Line Package

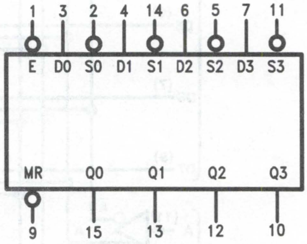


$\overline{E}$ 1
$\overline{S0}$ 2
D0 3
D1 4
$\overline{S2}$ 5
D2 6
D3 7
GND 8
16 V_{CC}
15 Q0
14 $\overline{S1}$
13 Q1
12 Q2
11 $\overline{S3}$
10 Q3
9 $\overline{MR}$

TL/F/9788-1

Order Number 9314DMQB, 9314FMQB or DM9314N
See NS Package Number J16A, N16E or W16A

Logic Symbol



1
3
2
4
14
6
5
7
11
E
D0
S0
D1
S1
D2
S2
D3
S3
MR
Q0
Q1
Q2
Q3
9
15
13
12
10

V_{CC} = Pin 16
GND = Pin 8

TL/F/9788-2

Pin Names	Description
$\overline{E}$	Enable Input (Active LOW)
D0–D3	Data Inputs
$\overline{S0}$–$\overline{S3}$	Set Inputs (Active LOW)
$\overline{MR}$	Master Reset Input (Active LOW)
Q0–Q3	Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to $\overline{E}$	5.0 18			5.0 18			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to $\overline{E}$	0 5.0			0 5.0			ns
t_s (H)	Setup Time HIGH, D_n to $\overline{S}_n$	8.0			8.0			ns
t_h (L)	Hold Time LOW, D_n to $\overline{S}_n$	8.0			8.0			ns
t_w (L)	$\overline{E}$ Pulse Width LOW	18			18			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	18			18			ns
t_{rec}	Recovery Time, $\overline{MR}$ to $\overline{E}$	0			0			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Min, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
		Data Inputs				60	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
		Data Inputs				−2.7	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−70	mA
			COM	−20		−70	
I_{CC}	Supply Current	V_{CC} = Max				55	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		24 24	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		12 24	ns
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n		18	ns
t_{PHL}	Propagation Delay $\overline{S}_n$ to Q_n		24	ns

Functional Description

The '9314 consists of four latches with a common active LOW Enable input and active LOW Master Reset input. When the Enable goes HIGH, data present in the latches is stored and the state of the latch is no longer affected by the $\overline{S}_n$ and D_n inputs. The Master Reset when activated overrides all other input conditions forcing all latch outputs LOW. Each of the four latches can be operated in one of two modes:

D-TYPE LATCH—For D-type operation the $\overline{S}$ input of a latch is held LOW. While the common Enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the Enable goes HIGH.

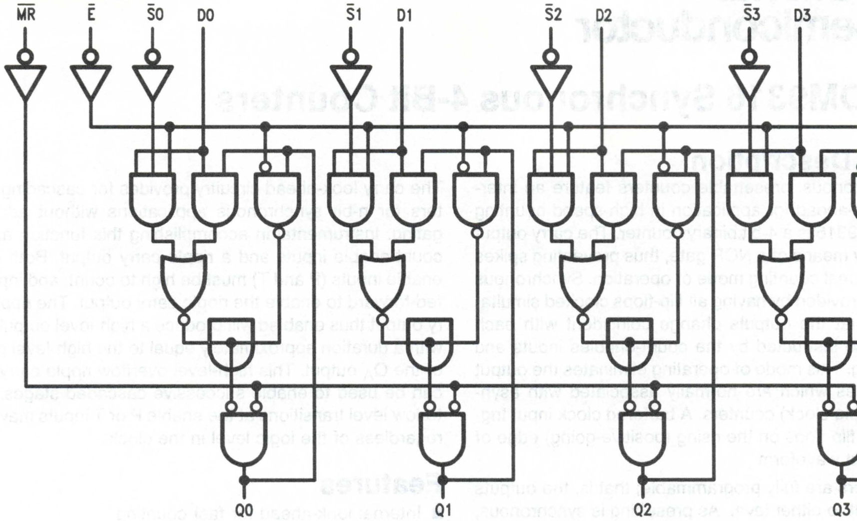
SET/RESET LATCH—During set/reset operation when the common Enable is LOW a latch is reset by a LOW on the D input, and can be set by a LOW on the $\overline{S}$ input if the D input is HIGH. If both $\overline{S}$ and D inputs are LOW, the D input will dominate and the latch will be reset. When the Enable goes HIGH, the latch remains in the last state prior to disablement. The two modes of latch operation are shown in the Truth Table.

Truth Table

$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_n	Operation
H	L	L	L	L	D Mode
H	L	H	L	H	
H	H	X	X	Q_{n-1}	
H	L	L	L	L	R/S Mode
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{n-1}	
H	H	X	X	Q_{n-1}	
L	X	X	X	L	Reset

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Q_{n-1} = Previous Output State
Q_n = Present Output State

Logic Diagram


$\overline{MR}$
$\overline{E}$
$\overline{S}0$
D0
$\overline{S}1$
D1
$\overline{S}2$
D2
$\overline{S}3$
D3
Q0
Q1
Q2
Q3

TL/F/9788-3

National Semiconductor

9316/DM9316 Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 9316 is a 4-bit binary counter. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enables inputs and internal gating. This mode of operating eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs. The clear function is asynchronous and a low level at the clear input sets of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs.

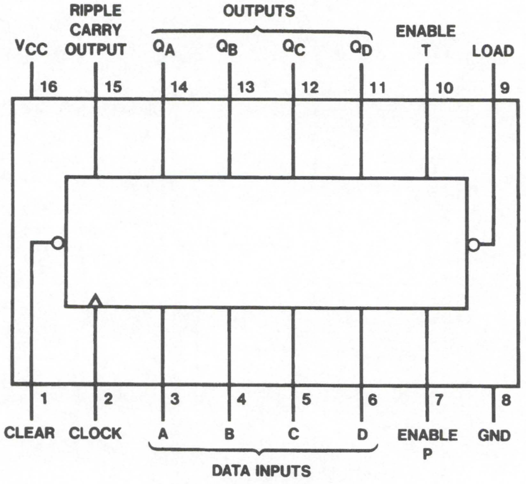
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed-forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur regardless of the logic level in the clock.

Features

- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical clock frequency 35 MHz
- Pin-for-pin replacements popular 54/74 counters 5416A/7416A (binary)
- Alternate Military/Aerospace device (9316) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6606–1

Order Number 9316DMQB, 9316FMQB, DM9316J
DM9316W or DM9316N
See NS Package Number J16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 6)		0		25	0		25	MHz
t_W	Pulse Width (Note 6)	Clock	25			25			ns
		Clear	20			20			
t_{SU}	Setup Time (Note 6)	Data	20			20			ns
		Enable P	20			20			
		Load	25			25			
		Clear	20			20			
t_H	Any Hold Time (Notes 1 & 6)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4 V	Clock			80	µA
			Enable T			80	
			Other			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Clock			−3.2	µA
			Enable T			−3.2	
			Other			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	MIL	−20		−57	mA
			COM	−18		−57	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 4)	MIL		59	85	mA
			COM		59	94	
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 5)	MIL		63	91	mA
			COM		63	101	

Note 1: The minimum HOLD time is as specified or as long as the CLOCK input takes to rise from 0.8V to 2V, whichever is longer.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: I_{CCH} is measured with the LOAD input high, then again with the LOAD input low, with all other inputs high and all outputs open.

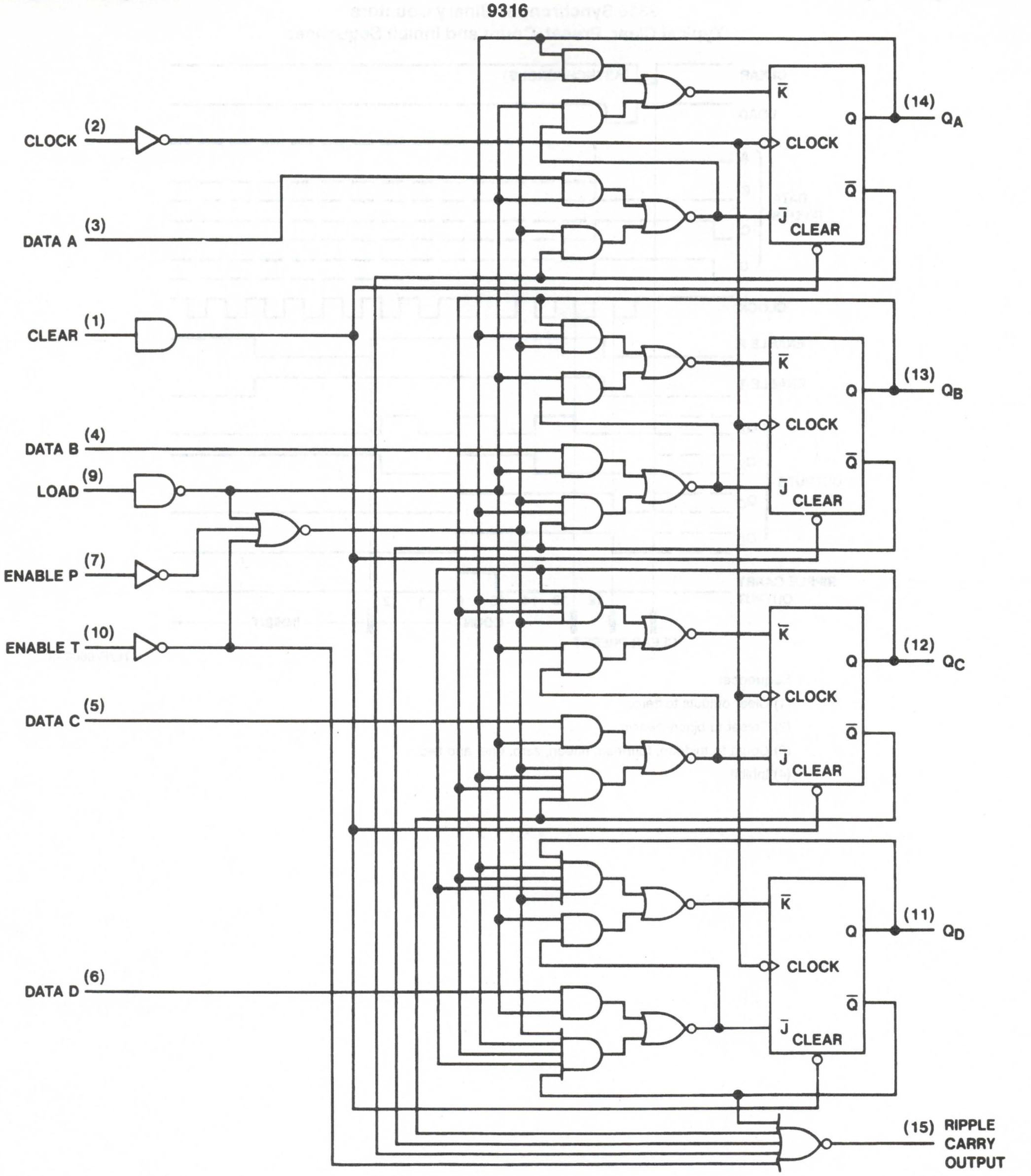
Note 5: I_{CCL} is measured with the CLOCK input high, then again with the CLOCK input low, with all other inputs low and all outputs open.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF Min	$R_L = 400\Omega$, $C_L = 15$ pF Max	Units
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to RC		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to RC		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	ENT to RC		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	ENT to RC		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		36	ns

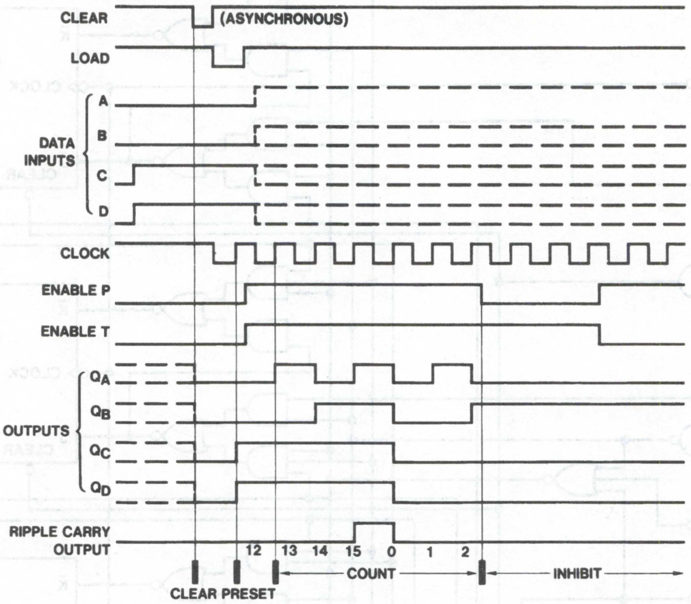
Logic Diagram


9316
CLOCK (2)
DATA A (3)
CLEAR (1)
DATA B (4)
LOAD (9)
ENABLE P (7)
ENABLE T (10)
DATA C (5)
DATA D (6)
K̄
Q
CLOCK
Q̄
J̄
CLEAR
(14) Q_A
(13) Q_B
(12) Q_C
(11) Q_D
(15) RIPPLE CARRY OUTPUT

TL/F/6606-2

Timing Diagram

9316 Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences


CLEAR
(ASYNCHRONOUS)
LOAD
DATA INPUTS
A
B
C
D
CLOCK
ENABLE P
ENABLE T
OUTPUTS
Q_A
Q_B
Q_C
Q_D
RIPPLE CARRY OUTPUT
12
13
14
15
0
1
2
COUNT
INHIBIT
CLEAR PRESET

TL/F/6606–3

Sequence:

(1) Clear outputs to zero.

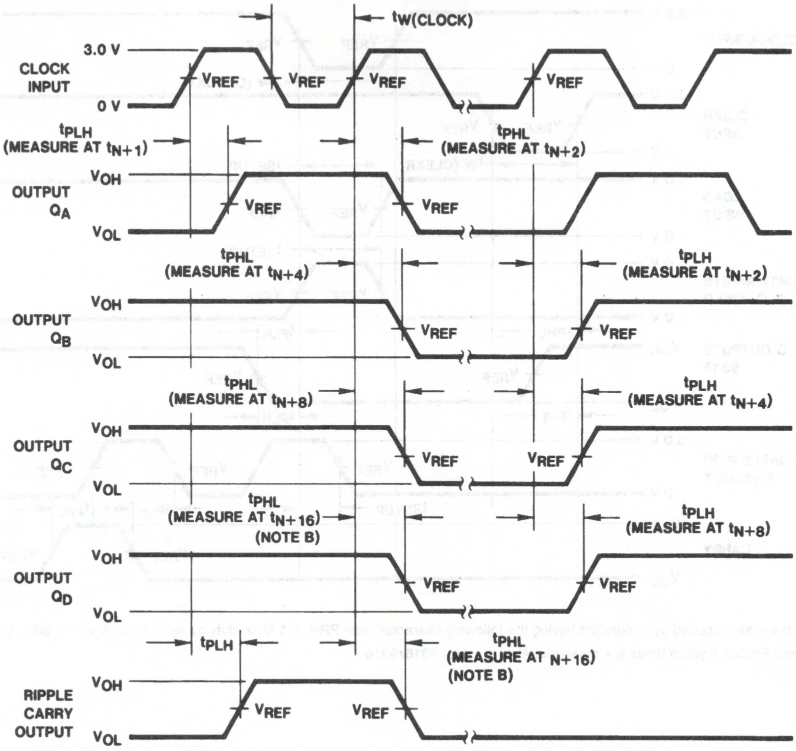
(2) Preset to binary twelve.

(3) Count to thirteen, fourteen, fifteen, zero, one, and two.

(4) Inhibit

Parameter Measurement Information

Switching Time Waveforms


tW(CLOCK)
3.0 V
CLOCK INPUT
0 V
VREF
tPLH (MEASURE AT tN+1)
tPHL (MEASURE AT tN+2)
VOH
OUTPUT QA
VOL
tPHL (MEASURE AT tN+4)
tPLH (MEASURE AT tN+2)
OUTPUT QB
tPHL (MEASURE AT tN+8)
tPLH (MEASURE AT tN+4)
OUTPUT QC
tPHL (MEASURE AT tN+16) (NOTE B)
tPLH (MEASURE AT tN+8)
OUTPUT QD
tPLH
tPHL (MEASURE AT N+16) (NOTE B)
RIPPLE CARRY OUTPUT

TL/F/6606–4

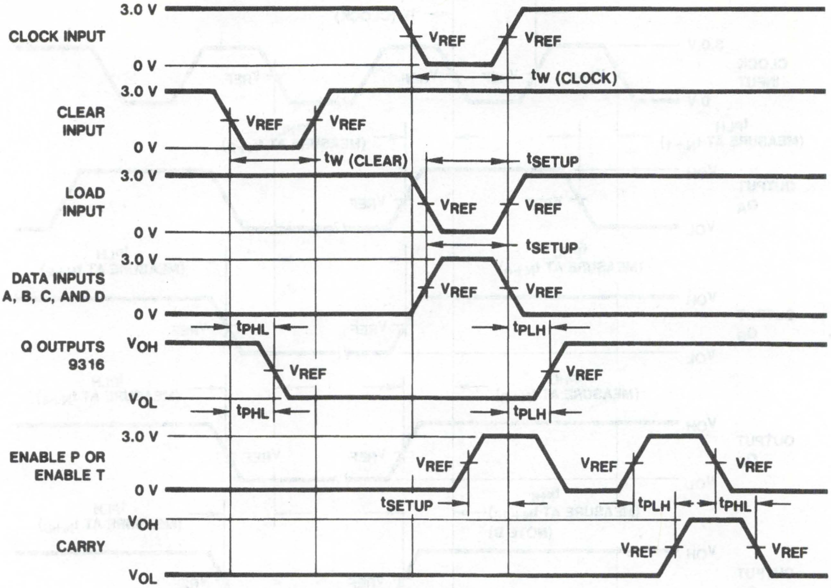
Note A: The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+16} for 9316/8316, where t_n is the bit time when all outputs are low.

Note C: $V_{REF} = 1.5V$.

Parameter Measurement Information (Continued)

Switching Time Waveforms


CLOCK INPUT
3.0 V
0 V
VREF
VREF
tW (CLOCK)
CLEAR INPUT
3.0 V
0 V
VREF
VREF
tW (CLEAR)
tSETUP
LOAD INPUT
3.0 V
0 V
VREF
VREF
tSETUP
DATA INPUTS A, B, C, AND D
3.0 V
0 V
VREF
VREF
tPHL
tPLH
Q OUTPUTS 9316
VOH
VOL
VREF
VREF
tPHL
tPLH
ENABLE P OR ENABLE T
3.0 V
0 V
VREF
VREF
VREF
tSETUP
tPLH
tPHL
CARRY
VOH
VOL
VREF
VREF

TL/F/6606-5

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Note B: Enable P and Enable T setup times are measured at t_{n+16} for 8316/9316.

Note C: $V_{REF} = 1.5V$.

National Semiconductor

DM9318 Priority Encoders

General Description

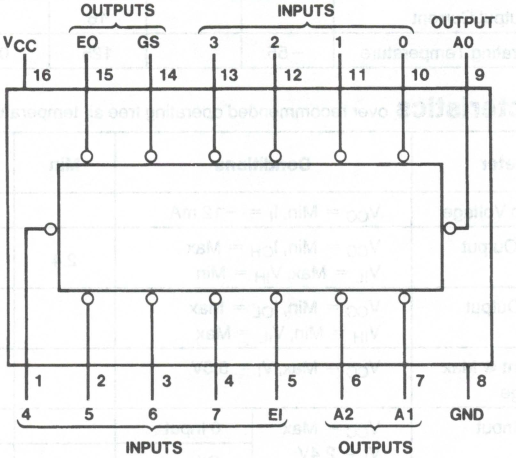
These TTL encoders feature priority decoding of the input data to ensure that only the highest-order data line is encoded. All inputs are buffered to represent one normalized Series 54/74 load. The DM9318 and DM8318 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output E0) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

Features

- Pin for pin with popular DM54148/74148
- Encodes 8 data lines to 3-line binary (octal)
- Applications include:
  - N-bit encoding
  - Code converters and generators
- Typical data delay 10 ns
- Typical power dissipation 190 mW

Connection Diagram

Dual-In-Line Package



TL/F/6607–1

Order Number DM9318J, DM9318N or DM9318W
See NS Package Number J16A, N16E or W16A

Function Table

Inputs									Outputs				
E1	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**A2**	**A1**	**A0**	**GS**	**EO**
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = High Logic Level, L = Low Logic Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	0 Input			40	μA
			Others			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	0 Input			−1.6	mA
			Others			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−35		−85	mA
			COM	−35		−85	
I_{CC1}	Supply Current Condition 1	V_{CC} = Max, (Note 3)			35	55	mA
I_{CC2}	Supply Current Condition 2	V_{CC} = Max, (Note 4)			40	60	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

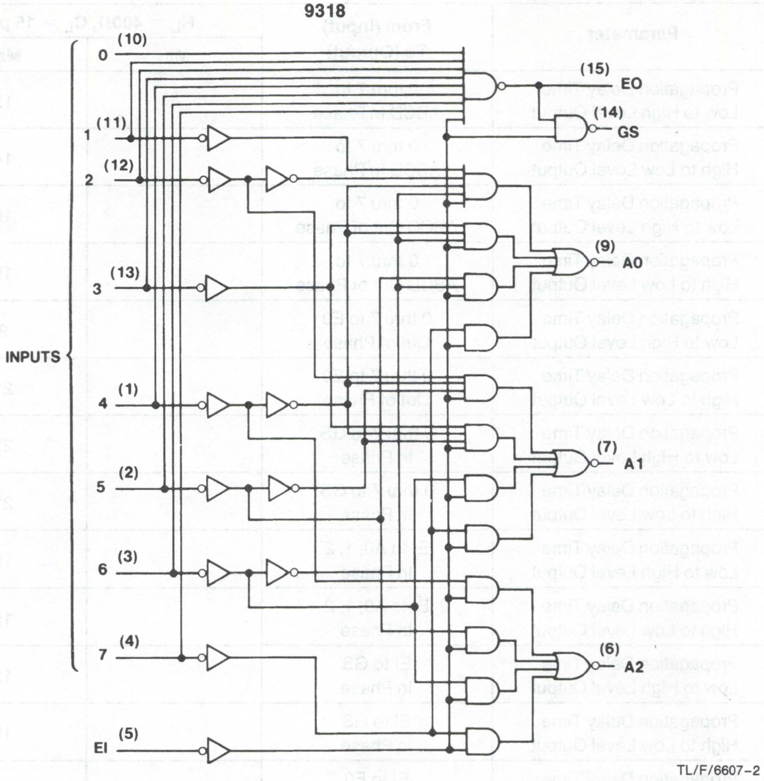
Note 3: I_{CC1} is measured with all inputs and outputs open.

Note 4: I_{CC2} is measured with inputs 7 and EI grounded and outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega, C_L = 15$ pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to ABCD In Phase		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to ABCD In Phase		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to ABCD Out of Phase		19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to ABCD Out of Phase		19	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to E0 Out of Phase		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to E0 Out of Phase		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to GS In Phase		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to GS In Phase		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	El to A0, 1, 2 In Phase		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	El to A0, 1, 2 In Phase		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	El to GS In Phase		12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	El to GS In Phase		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	El to E0 In Phase		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	El to E0 In Phase		26	ns

Logic Diagram


9318
INPUTS
0
(10)
1
(11)
2
(12)
3
(13)
4
(1)
5
(2)
6
(3)
7
(4)
EI
(5)
(15)
EO
(14)
GS
(9)
A0
(7)
A1
(6)
A2
TL/F/6607-2

National Semiconductor

9321/DM9321
Dual 1-of-4 Decoder

General Description

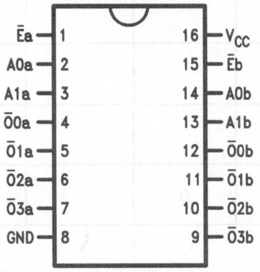
The 9321 consists of two independent multipurpose decoders, each designed to accept two inputs and provide four mutually exclusive outputs. In addition an active LOW enable input, which gives demultiplexing capability, is provided for each decoder.

Features

- Multifunction capability
- Mutually exclusive outputs
- Demultiplexing capability
- Active low enable for each decoder

Connection Diagram

Dual-In-Line Package

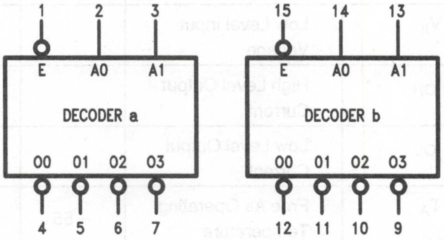


$\overline{E}$a 1
A0a 2
A1a 3
$\overline{O}$0a 4
$\overline{O}$1a 5
$\overline{O}$2a 6
$\overline{O}$3a 7
GND 8
16 V_{CC}
15 $\overline{E}$b
14 A0b
13 A1b
12 $\overline{O}$0b
11 $\overline{O}$1b
10 $\overline{O}$2b
9 $\overline{O}$3b

TL/F/10209–1

Order Number 9321DMQB, 9321FMQB or DM9321N
See NS Package Number J16A, N16E or W16A

Logic Symbol



1
2
3
E
A0
A1
DECODER a
00
01
02
03
4
5
6
7
15
14
13
E
A0
A1
DECODER b
00
01
02
03
12
11
10
9

TL/F/10209–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{E}$a, $\overline{E}$b	Enable Inputs (Active LOW)
A0a, A1a, A0b, A1b	Address Inputs
$\overline{O}$0a–$\overline{O}$3a $\overline{O}$0b–$\overline{O}$3b	Decoder Outputs (Active LOW)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
COMM	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−70	mA
			COM	−1.3		−3.7	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				50	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH}	Propagation Delay, An to $\overline{\text{O}}$n		20	ns
t_{PHL}			21	
t_{PLH}	Propagation Delay, $\overline{\text{E}}$ to $\overline{\text{O}}$n		14	ns
t_{PHL}			18	

Functional Description

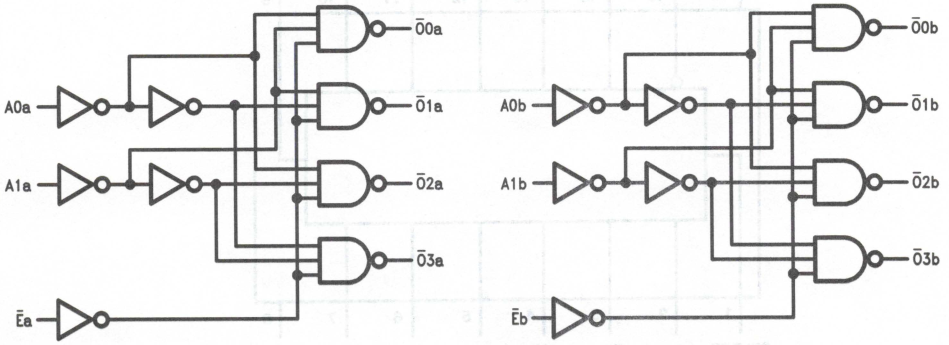
The 9321 consists of two separate decoders each designed to accept two binary weighted inputs and provide four mutually exclusive active LOW outputs as shown in the logic symbol. Each decoder can be used as a 4-output demultiplexer by using the enable as a data input.

Truth Table (Each Decoder)

Inputs			Outputs			
$\overline{\text{E}}$	A0	A1	$\overline{\text{O}}$0	$\overline{\text{O}}$1	$\overline{\text{O}}$2	$\overline{\text{O}}$3
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



$\overline{\text{O}}$0a
A0a
$\overline{\text{O}}$1a
A1a
$\overline{\text{O}}$2a
$\overline{\text{O}}$3a
$\overline{\text{E}}$a
$\overline{\text{O}}$0b
A0b
$\overline{\text{O}}$1b
A1b
$\overline{\text{O}}$2b
$\overline{\text{O}}$3b
$\overline{\text{E}}$b

TL/F/10209-3

National Semiconductor

9322/DM9322 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. True data is presented at the outputs.

Features

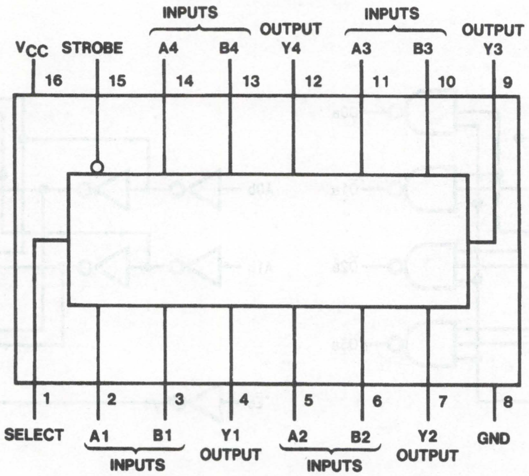
- Pin-for-pin with popular DM54157/74157
- Buffered inputs and outputs

Applications

- Expand any data input point
- Multiplex dual-data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters
- Alternate Military/Aerospace device (9322) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package


INPUTS
OUTPUT
INPUTS
OUTPUT
V_{CC}
STROBE
A4
B4
Y4
A3
B3
Y3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
SELECT
A1
B1
Y1
A2
B2
Y2
GND
INPUTS
OUTPUT
INPUTS
OUTPUT

TL/F/6608–1

Order Number 9322DMQB, 9322FMQB, DM9322J, DM9322W or DM8322N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs				Output
Strobe	Select	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Level, L = Low Level, X = Don't Care.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−55	mA
			COM	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	48	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

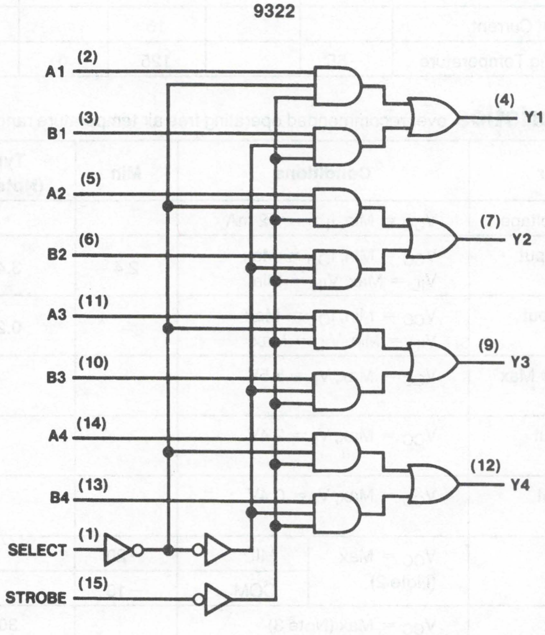
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		27	ns

Logic Diagram


9322
(2) A1
(3) B1
(5) A2
(6) B2
(11) A3
(10) B3
(14) A4
(13) B4
(1) SELECT
(15) STROBE
(4) Y1
(7) Y2
(9) Y3
(12) Y4

TL/F/6608–2

National Semiconductor

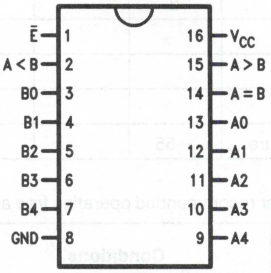
9324/DM9324 5-Bit Comparator

General Description

The 9324 expandable comparators provide comparison between two 5-bit words and give three outputs—"less than", "greater than" and "equal to". A HIGH on the active LOW Enable Input forces all three outputs LOW.

Connection Diagram

Dual-In-Line Package



$\overline{E}$ 1
A < B 2
B0 3
B1 4
B2 5
B3 6
B4 7
GND 8
16 V_{CC}
15 A > B
14 A = B
13 A0
12 A1
11 A2
10 A3
9 A4

TL/F/9792–1

Order Number 9324DMQB, 9324FMQB, or DM9324N
See NS Package Number J16A, N16E or W16A

Pin Names	Description
$\overline{E}$	Enable Input (Active LOW)
A0–A4	Word A Parallel Inputs
B0–B4	Word B Parallel Inputs
A < B	A Less than B Output (Active HIGH)
A > B	A Greater than B Output (Active HIGH)
A = B	A Equal to B Output (Active HIGH)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−70	mA
			COM	−20		−70	
I_{CC}	Supply Current	V_{CC} = Max				81	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to A = B		14 14	ns
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to A > B		25 22	ns
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to A < B		26 21	ns
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to A = B		30 32	ns

Functional Description

The '24 5-bit comparators use combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW Enable Input ($\overline{E}$).

Tying the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion.

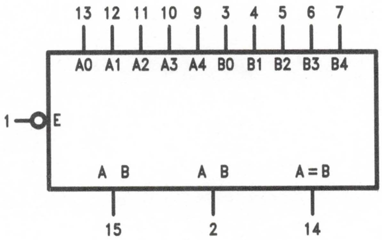
The A4 and B4 inputs are the most significant inputs and A0, B0 the least significant. Thus if A4 is HIGH and B4 is LOW, the A > B output will be HIGH regardless of all other inputs except $\overline{E}$.

Truth Table

Inputs			Outputs		
$\overline{E}$	A_n	B_n	A < B	A > B	A = B
H	X	X	L	L	L
L	Word A = Word B		L	L	H
L	Word A > Word B		L	H	L
L	Word B > Word A		H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

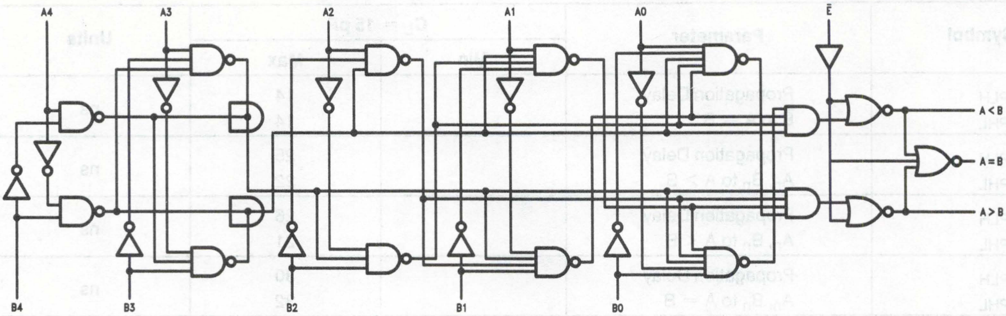
Logic Symbol



TL/F/9792-2

V_{CC} = Pin 16
GND = Pin 6

Logic Diagram


A4
A3
A2
A1
A0
Ē
A<B
A=B
A>B
B4
B3
B2
B1
B0

TL/F/9792-3

National Semiconductor

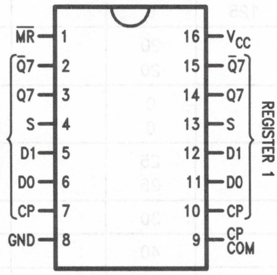
9328/DM9328 Dual 8-Bit Shift Register

General Description

The '9328 is a high speed serial storage element providing 16 bits of storage in the form of two 8-bit registers. The multifunctional capability of this device is provided by several features: 1) additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources; 2) the clock of each register may be provided separately or together; 3) both the true and complementary outputs are provided from each 8-bit register, and both registers may be master cleared from a common input.

Connection Diagram

Dual-In-Line Package

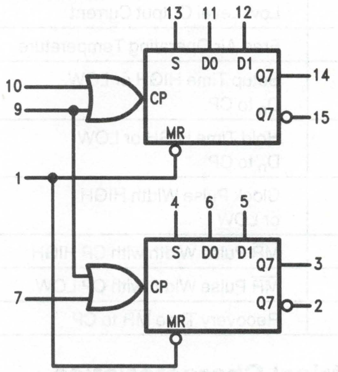


$\overline{MR}$ 1
$\overline{Q7}$ 2
Q7 3
S 4
D1 5
D0 6
CP 7
GND 8
REGISTER 2
16 V_{CC}
15 $\overline{Q7}$
14 Q7
13 S
12 D1
11 D0
10 CP
9 CP COM
REGISTER 1

TL/F/9793-1

Order Number 9328DMQB, 9328FMQB or DM9328N
See NS Package Number J16A, N16E or W16A

Logic Symbol



13
11
12
S
D0
D1
Q7
14
10
9
CP
$\overline{Q7}$
15
$\overline{MR}$
1
4
6
5
S
D0
D1
Q7
3
7
CP
$\overline{Q7}$
2
$\overline{MR}$

TL/F/9793-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
S	Data Select Input
D0, D1	Data Inputs
CP	Clock Pulse Input (Active HIGH) Common (Pin 9) Separate (Pins 7 and 10)
$\overline{MR}$	Master Reset Input (Active LOW)
Q7	Last Stage Output
$\overline{Q7}$	Complementary Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H)	Setup Time HIGH or LOW	20			20			ns
t_s (L)	D_n to CP	20			20			
t_h (H)	Hold Time HIGH or LOW	0			0			ns
t_h (L)	D_n to CP	0			0			
t_w (H)	Clock Pulse Width HIGH	25			25			ns
t_w (L)	or LOW	25			25			
t_w (L)	$\overline{MR}$ Pulse Width with CP HIGH	30			30			ns
t_w (L)	$\overline{MR}$ Pulse Width with CP LOW	40			40			ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	33			33			ns

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range (Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V $\overline{MR}$, D_n Inputs			40	µA
		CP Inputs			60	
		S Inputs			80	
		CP (COM) Inputs			120	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V $\overline{MR}$, D_n Inputs			−1.6	mA
		CP Inputs			−2.4	
		S Inputs			−3.2	
		CP (COM) Input			−4.8	

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range (Unless Otherwise Noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−70	mA
			COMM	−20		−70	
I_{CC}	Supply Current	V_{CC} = Max				77	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF, R_L = 400Ω		Units
		Min	Max	
f_{max}	Maximum Shift Right Frequency	20		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q7 or $\overline{Q}$7		20 35	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q7		50	ns

Functional Description

The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW-to-HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH-to-LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal.

Each 8-bit shift register has a 2-input multiplexer in front of the serial data input. The two data inputs D0 and D1 are controlled by the data select input (S) following the Boolean expression:

Serial data in: $S_D = \overline{S}D0 + SD1$

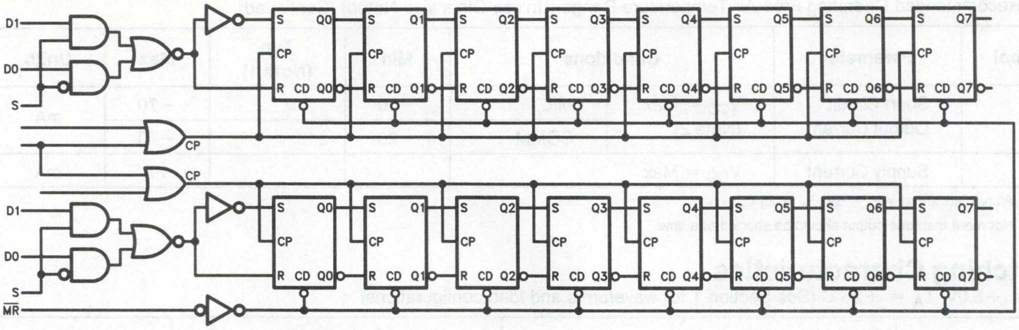
An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all 16 stages independently of any other input signal.

Shift Select Table

INPUTS			OUTPUT
S	D0	D1	Q7 (t_{n+8})
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
n + 8 = indicates state after eight clock pulse

Logic Diagram


D1
D0
S
CP
CP
D1
D0
S
MR
S
CP
R
CD
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7

TL/F/9793-3

National Semiconductor

9334/DM9334 8-Bit Addressable Latch

General Description

The DM9334 is a high speed 8-bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level high outputs. The device also incorporates an active level low common clear for resetting all latches, as well as an active level low enable.

The DM9334 has four modes of operation which are shown in the mode selection table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the low state. In the clear mode all outputs are low and unaffected by the address and data inputs.

When operating the device as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

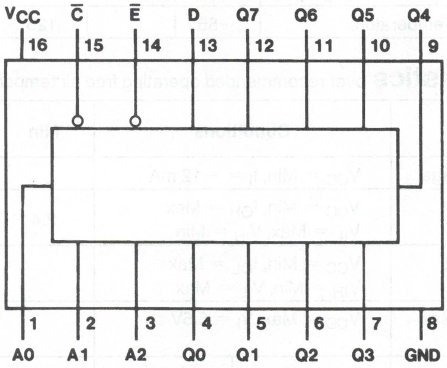
The function tables summarize the operation of the product.

Features

- Common clear
- Easily expandable
- Random (addressable) data entry
- Serial to parallel capability
- 8 bits of storage/output of each bit available
- Active high demultiplexing/decoding capability
- Alternate Military/Aerospace device (9334) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6609-1

Order Number 9334DMQB, 9334FMQB, DM9334J or DM9334N
See NS Package Number J16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0° to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
t_W	ENABLE Pulse Width (Fig. 1) (Note 4)		19	13		19	13		ns
t_{SU}	Setup Time (Note 4)	Data 1 (Fig. 4)	20	13		20	13		ns
		Data 0 (Fig. 4)	20	14		20	14		
		Address (Fig. 6) (Note 1)	10	5		10	5		
t_H	Hold Time (Note 4)	Data 1 (Fig. 4)	0	−10		0	−10		ns
		Data 0 (Fig. 4)	0	−13		0	−13		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	$\overline{E}$ Input			60	μA
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	$\overline{E}$ Input			−2.4	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	MIL	−30		−100	mA
			COM	−30		−100	
I_{CC}	Supply Current	V_{CC} = Max			56	86	mA

Note 1: The ADDRESS setup time is the time before the negative ENABLE transition that the ADDRESS must be stable so that the correct latch is addressed without affecting the other latches.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega, C_L = 15\ pF$		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output, Fig. 1		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output, Fig. 1		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output, Fig. 2		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output, Fig. 2		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Address to Output, Fig. 3		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Address to Output, Fig. 3		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output, Fig. 5		31	ns

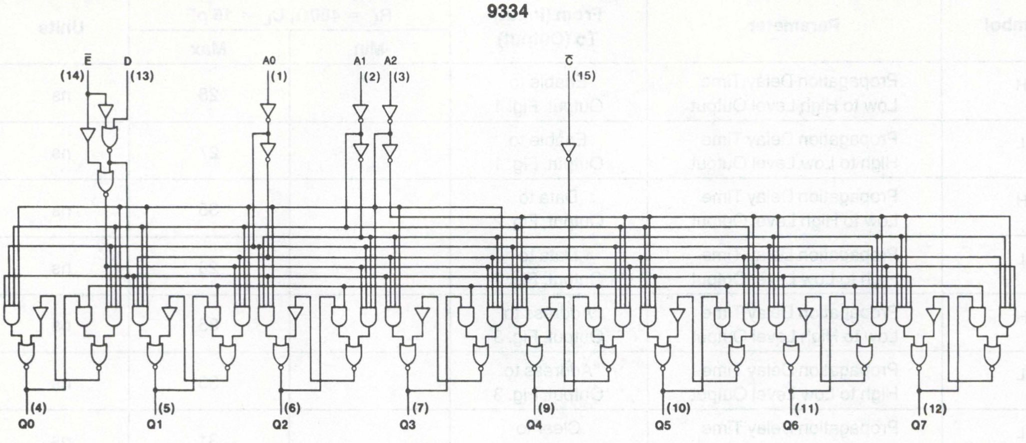
Function Tables

$\overline{E}$	$\overline{C}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active High Eight Channel Demultiplexer
H	L	Clear

Inputs						Present Output States								Mode
$\overline{C}$	$\overline{E}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1}								Memory
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}					Addressable Latch
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1}						
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1}						
•	•	•		•				•						
•	•	•		•				•						
•	•	•		•				•						
H	L	L	H	H	H	Q_{N-1}						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1}						Q_{N-1}	H	

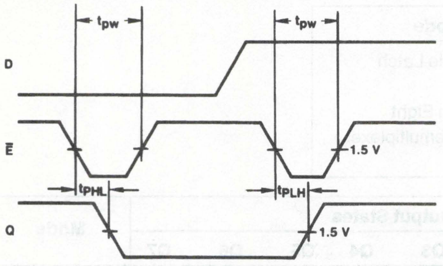
X = Don't Care Condition
L = Low Voltage Level
H = High Voltage Level
Q_{N-1} = Previous Output State

Logic Diagram


9334
Ē
D
A0
A1
A2
C̄
(14)
(13)
(1)
(2)
(3)
(15)
(4)
Q0
(5)
Q1
(6)
Q2
(7)
Q3
(9)
Q4
(10)
Q5
(11)
Q6
(12)
Q7

TL/F/6609-2

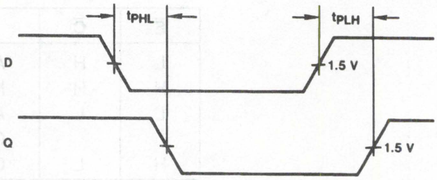
Switching Time Waveforms


t_{pw}
t_{pw}
D
Ē
1.5 V
t_{PHL}
t_{PLH}
Q
1.5 V

TL/F/6609-3

Other Conditions: C = H, A = Stable

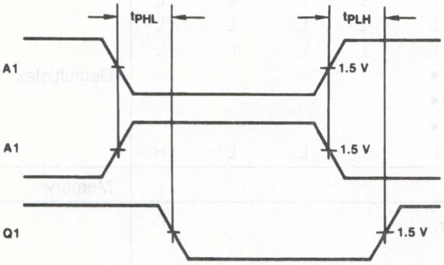
Figure 1


t_{PHL}
t_{PLH}
D
1.5 V
Q
1.5 V

TL/F/6609-4

Other Conditions: Ē = L, C̄ = H, A = Stable

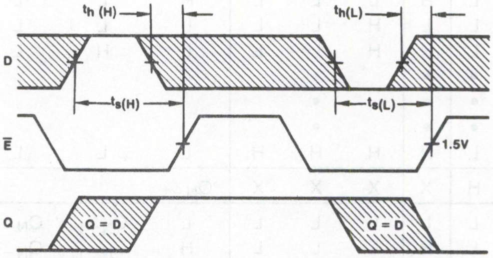
Figure 2


t_{PHL}
t_{PLH}
A1
1.5 V
A1
1.5 V
Q1
1.5 V

TL/F/6609-5

Other Conditions: Ē = L, C̄ = L, D = H

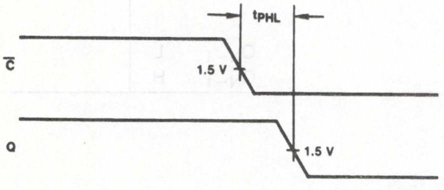
Figure 3


t_h (H)
$t_{h(L)}$
D
t_s(H)
$t_{s(L)}$
Ē
1.5V
Q
Q = D
Q = D

TL/F/6609-6

Other Conditions: C = H, A = Stable

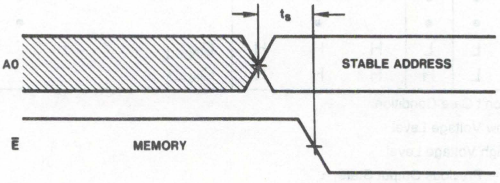
Figure 4


t_{PHL}
C̄
1.5 V
Q
1.5 V

TL/F/6609-7

Other Conditons: Ē = H

Figure 5


t_s
A0
STABLE ADDRESS
Ē
MEMORY

TL/F/6609-8

Other Conditions: C̄ = H

Figure 6

Note: The shaded areas indicate when the inputs are permitted to change for predictable output performance.

National Semiconductor

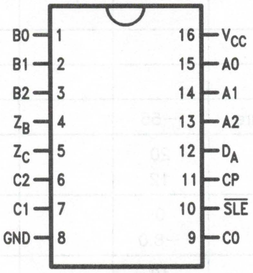
9338/DM9338 8-Bit Multiple Port Register

General Description

The DM9338 is an 8-bit multiple port register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the eight bits and read from any two of the eight bits simultaneously.

Connection Diagrams

Dual-In-Line Package



TL/F/9794-1

Order Number 9338DMQB, 9338FMQB or DM9338N
See NS Package Number J16A, N16E or W16A

Pin Names	Description
A0–A2	Write Address Inputs
D_A	Data Input
B0–B2	B Read Address Inputs
C0–C2	C Read Address Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{SLE}$	Slave Enable Input (Active LOW)
Z_B	B Output
Z_C	C Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_A to CP	20 12			20 12			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_A to CP	0 −8.0			0 −8.0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to CP	10 10			10 10			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to CP	0 0			0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	23 13			23 13			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				27	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.1	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−10		−70	mA
			COM	−10		−70	
I_{CC}	Supply Current	V_{CC} = Max				135	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15$ pF				Units
		9338 (MIL)		DM9338 (COM)		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay B_n or C_n to Z_n		40	13	40	ns
t_{PHL}			35	18	35	
t_{PLH}	Propagation Delay D_A to Z_n		45	25	45	ns
t_{PHL}			50	25	50	
t_{PLH}	Propagation Delay CP to Z_n		35	18	35	ns
t_{PHL}			30	13	30	

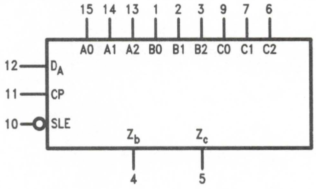
Functional Description

The 9338 8-bit multiple port register can be considered a 1-bit slice of eight high speed working registers. Data can be written into any one and read from any two of the eight locations simultaneously. Master/slave operation eliminates all race problems associated with simultaneous read/write activity from the same location. When the clock input (CP) is LOW data applied to the data input line (D_A) enters the selected master. This selection is accomplished by coding the three write input select lines (A0–A2) appropriately. Data is stored synchronously with the rising edge of the clock pulse.

The information for each of the two slaved (output) latches is selected by two sets of read address inputs (B0–B2 and C0–C2). The information enters the slave while the clock is HIGH and is stored while the clock is LOW. If Slave Enable is LOW ($\overline{SLE}$), the slave latches are continuously enabled. The signals are available on the output pins (Z_B and Z_C). The input bit selection and the two output bit selections can be accomplished independently or simultaneously. The data flows into the device, is demultiplexed according to the state of the write address lines and is clocked into the selected latch. The eight latches function as masters and store the input data. The two output latches are slaves and hold the data during the read operation. The state of each slave is determined by the state of the master selected by its associated set of read address inputs.

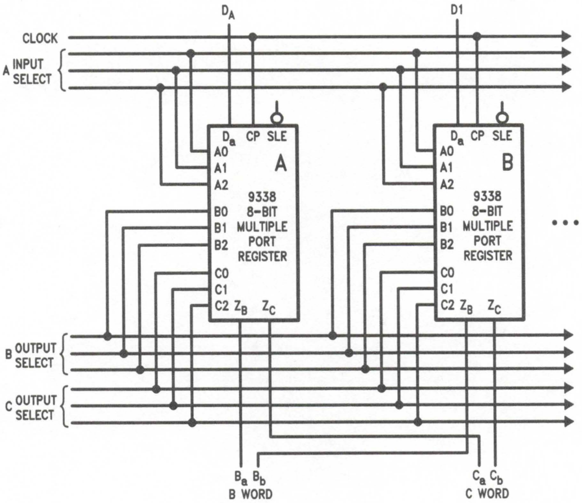
The method of parallel expansion is shown in *Figure a*. One 9338 is needed for each bit of the required word length. The read and write input lines should be connected in common on all of the devices. This register configuration provides two words of n-bits each at one time, where n devices are connected in parallel.

Logic Symbol



TL/F/9794-2

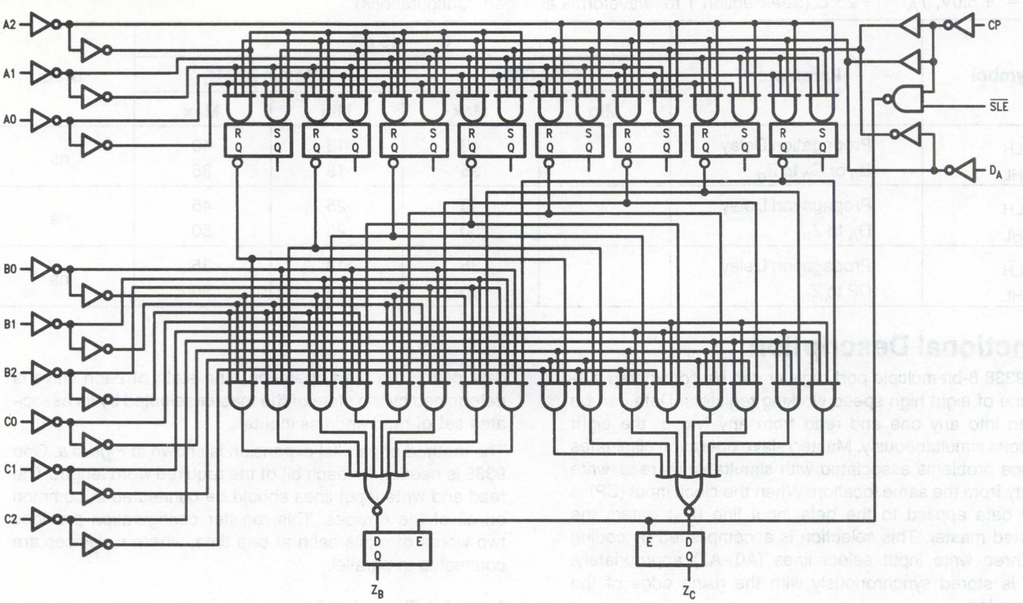
V_{CC} = Pin 16
GND = Pin 8



TL/F/9794-4

FIGURE a. Parallel Expansion

Logic Diagram



A2
A1
A0
B0
B1
B2
C0
C1
C2
CP
SLE
D_A
R Q
S Q
D Q E
E D Q
Z_B
Z_C

TL/F/9794–3

National Semiconductor

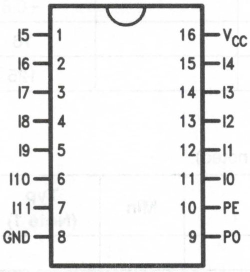
9348
12-Input Parity Checker/Generator

General Description

The 9348 is a 12-input parity checker/generator generating odd and even parity outputs. It can be used in high speed error detection applications.

Connection Diagram

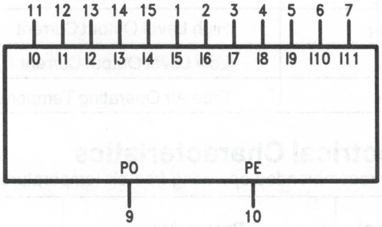
Dual-In-Line Package


I5 1
I6 2
I7 3
I8 4
I9 5
I10 6
I11 7
GND 8
16 VCC
15 I4
14 I3
13 I2
12 I1
11 I0
10 PE
9 PO

TL/F/9795-1

Order Number 9348DMQB or 9348FMQB
See NS Package Number J16A or W16A

Logic Symbol


11 12 13 14 15 1 2 3 4 5 6 7
I0 I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11
PO
PE
9
10

TL/F/9795-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
I0–I11	Parity Inputs
PO	Odd Parity Output
PE	Even Parity Output

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	9348			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.8	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−70	mA
I_{CC}	Supply Current	V_{CC} = Max			82	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configuration)

Symbol	Parameter	Conditions	C_L = 15 pF R_L = 400Ω		Units
			Min	Max	
t_{PLH} t_{PHL}	Propagation Delay I4 to PO	I2, I3, I7, I8 = GND; Other Inputs (except I4) HIGH		46 42	ns
t_{PLH} t_{PHL}	Propagation Delay I4 to PE	I2, I3, I7, I8 = GND; Other Inputs (except I4) HIGH		51 48	ns
t_{PLH}	Propagation Delay I3 to PO	I7 = HIGH; Other Inputs (except I3) = GND		27	ns
t_{PHL}	Propagation Delay I4 to PO	All Inputs (except I4) = GND		25	ns

Functional Description

The 9348 is a 12-input parity generator. It provides odd and even parity for up to 12 data bits. The Even Parity output (PE) will be HIGH if an even number of logic ones are present on the inputs. The Odd Parity output (PO) will be HIGH if an odd number of logic ones are present on the inputs. The logic equations for the outputs are shown below.

$$PO = I0 \oplus I1 \oplus I2 \oplus I3 \oplus I4 \oplus I5 \oplus I6 \oplus I7 \oplus I8 \oplus I9 \oplus I10 \oplus I11$$
$$PE = \overline{I0 \oplus I1 \oplus I2 \oplus I3 \oplus I4 \oplus I5 \oplus I6 \oplus I7 \oplus I8 \oplus I9 \oplus I10 \oplus I11}$$

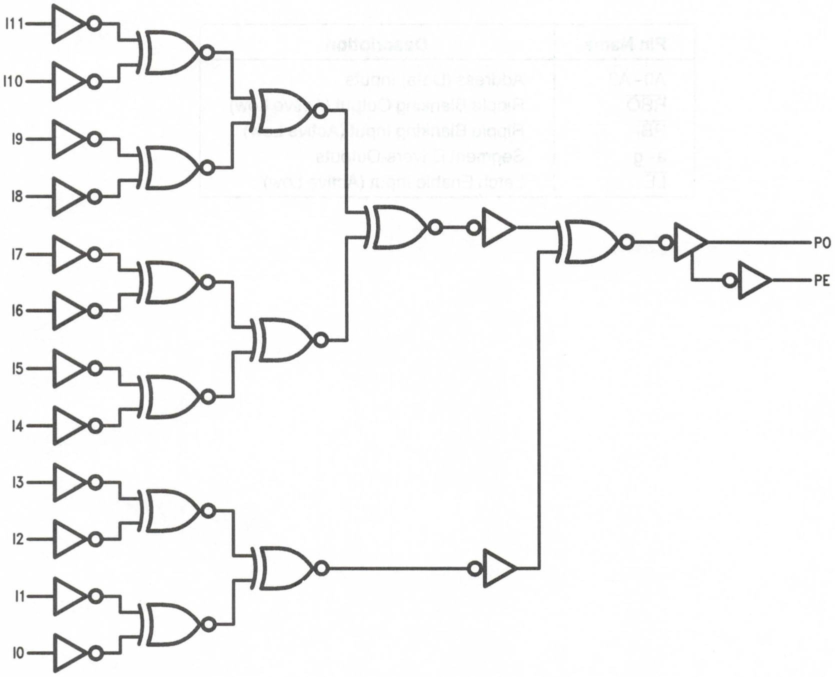
Note: Less through delay is encountered from the I0, I1, I2 and I3 inputs than I4 thru I11 inputs. Therefore, if some signals are slower than others, the slower signals should be applied to these four inputs for maximum speed.

Truth Table

Inputs		Outputs	
I0–I11		PO	PE
All Twelve	Inputs LOW	L	H
Any One	Inputs HIGH	H	L
Any Two	Inputs HIGH	L	H
Any Three	Inputs HIGH	H	L
Any Four	Inputs HIGH	L	H
Any Five	Inputs HIGH	H	L
Any Six	Inputs HIGH	L	H
Any Seven	Inputs HIGH	H	L
Any Eight	Inputs HIGH	L	H
Any Nine	Inputs HIGH	H	L
Any Ten	Inputs HIGH	L	H
Any Eleven	Inputs HIGH	H	L
Any Twelve	Inputs HIGH	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram



TL/F/9795-3

National Semiconductor

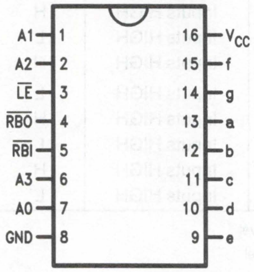
DM9368 7-Segment Decoder/Driver/Latch with Constant Current Source Outputs

General Description

The DM9368 is a 7-segment decoder driver incorporating input latches and constant current output circuits to drive common cathode type LED displays directly.

Connection Diagram

Dual-In-Line Package



TL/F/9796-1

Order Number DM9368N
See NS Package Number N16E

Pin Name	Description
A0–A3	Address (Data) Inputs
$\overline{RBO}$	Ripple Blanking Output (Active Low)
$\overline{RBI}$	Ripple Blanking Input (Active Low)
a–g	Segment Drivers-Outputs
$\overline{LE}$	Latch Enable Input (Active Low)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM9368			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−80	μA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C
$t_s(H)$	Setup Time High A_n to $\overline{LE}$	30			ns
$t_h(H)$	Hold Time HIGH A_n to $\overline{LE}$	0			ns
$t_s(L)$	Setup Time LOW A_n to $\overline{LE}$	20			ns
$t_h(L)$	Hold Time LOW A_n to $\overline{LE}$	0			ns
$t_w(L)$	$\overline{LE}$ Pulse Width LOW	45			ns
I_{OH}	Segment Output HIGH Current	−16		−22	mA
I_{OL}	Segment Output LOW Current	−250		250	μA

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−18		−57	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open, Data & Latch Inputs = 0V			67	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

V_{CC} = 5.0V, T_A = 25°C (See Section 1 for Waveforms and Load Configuations)

Symbol	Parameter	C_L = 15 pF R_L = 100Ω		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A_n to a–g		40 70	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$ to a–g		70 90	ns

Functional Description

The '68 is a 7-segment decoder driver designed to drive 7-segment common cathode LED displays. The '68 drives any common cathode LED display rated at a nominal 20 mA at 1.7V per segment without need for current limiting resistors.

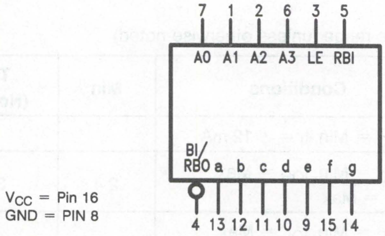
This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a hexadecimal decode format which produces numeric codes "0" thru "9" and alpha codes "A" through "F" using upper and lower case fonts.

Latches on the four data inputs are controlled by an active LOW latch enable $\overline{LE}$. When the $\overline{LE}$ is LOW, the state of the outputs is determined by the input data. When the $\overline{LE}$ goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The $\overline{LE}$ pulse width necessary to accept and store data is typically 30 ns which allows data to be strobed into the '68 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

Another feature of the '68 is that the unit loading on the data inputs is very low (−100 μA Max) when the latch enable is HIGH. This allows '68s to be driven from an MOS device in multiplex mode without the need for drivers on the data lines.

The '68 also has provision for automatic blanking of the leading and/or trailing edge zeros in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeros. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

Logic Symbol



TL/F/9796-2

Truth Table

BINARY STATE	INPUTS $\overline{\text{LE}}$	$\overline{\text{RBI}}$	A3	A2	A1	A0	OUTPUTS a	b	c	d	e	f	g	$\overline{\text{RBO}}$	DISPLAY
—	H	*	X	X	X	X	← STABLE →							H	STABLE
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
0	L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
1	L	X	L	L	L	H	L	H	H	L	L	L	L	H	1
2	L	X	L	L	H	L	H	H	L	H	H	L	H	H	2
3	L	X	L	L	H	H	H	H	H	H	L	L	H	H	3
4	L	X	L	H	L	L	L	H	H	L	L	H	H	H	4
5	L	X	L	H	L	H	H	L	H	H	L	H	H	H	5
6	L	X	L	H	H	L	H	L	H	H	H	H	H	H	6
7	L	X	L	H	H	H	H	H	H	L	L	L	L	H	7
8	L	X	H	L	L	L	H	H	H	H	H	H	H	H	8
9	L	X	H	L	L	H	H	H	H	L	L	H	H	H	9
10	L	X	H	L	H	L	H	H	H	L	H	H	H	H	A
11	L	X	H	L	H	H	L	L	H	H	H	H	H	H	b
12	L	X	H	H	L	L	H	L	L	H	H	H	L	H	C
13	L	X	H	H	L	H	L	H	H	H	H	L	H	H	d
14	L	X	H	H	H	L	H	L	L	H	H	H	H	H	E
15	L	X	H	H	H	H	H	L	L	L	H	H	H	H	F
X	X	X	X	X	X	X	L	L	L	L	L	L	L	L**	BLANK

TL/F/9796-8

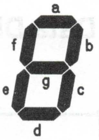
*The $\overline{\text{RBI}}$ will blank the display only if a binary zero is stored in the latches.

**The $\overline{\text{RBO}}$ used as an input overrides all other input conditions.

H = HIGH Voltage Level

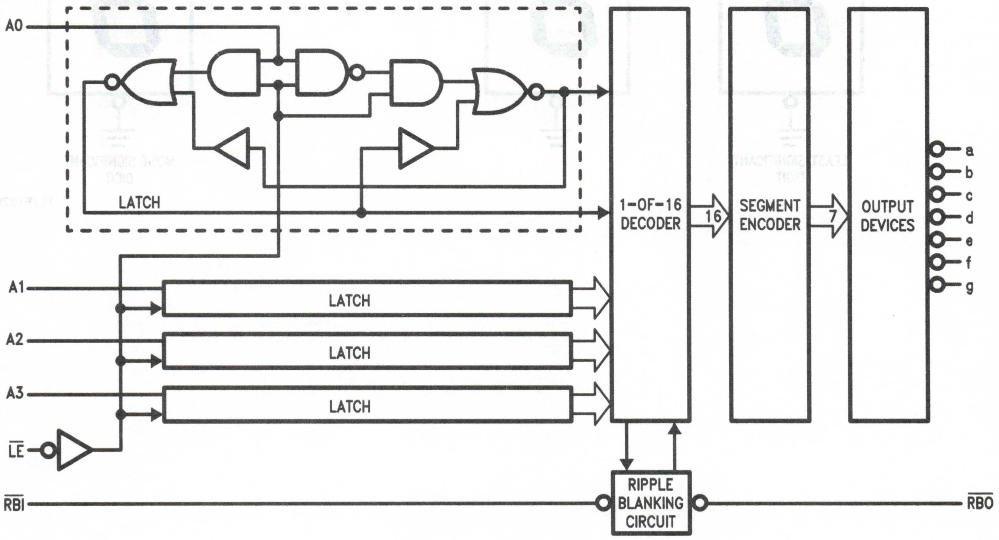
L = LOW Voltage Level

X = Immaterial



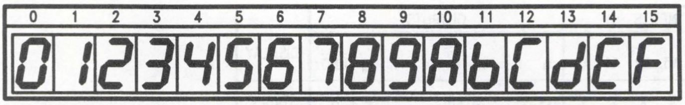
TL/F/9796-4

Logic Diagram


A0
LATCH
A1
LATCH
A2
LATCH
A3
LATCH
LE
RBI
1-OF-16 DECODER
16
SEGMENT ENCODER
7
OUTPUT DEVICES
a
b
c
d
e
f
g
RIPPLE BLANKING CIRCUIT
RBO

TL/F/9796-3

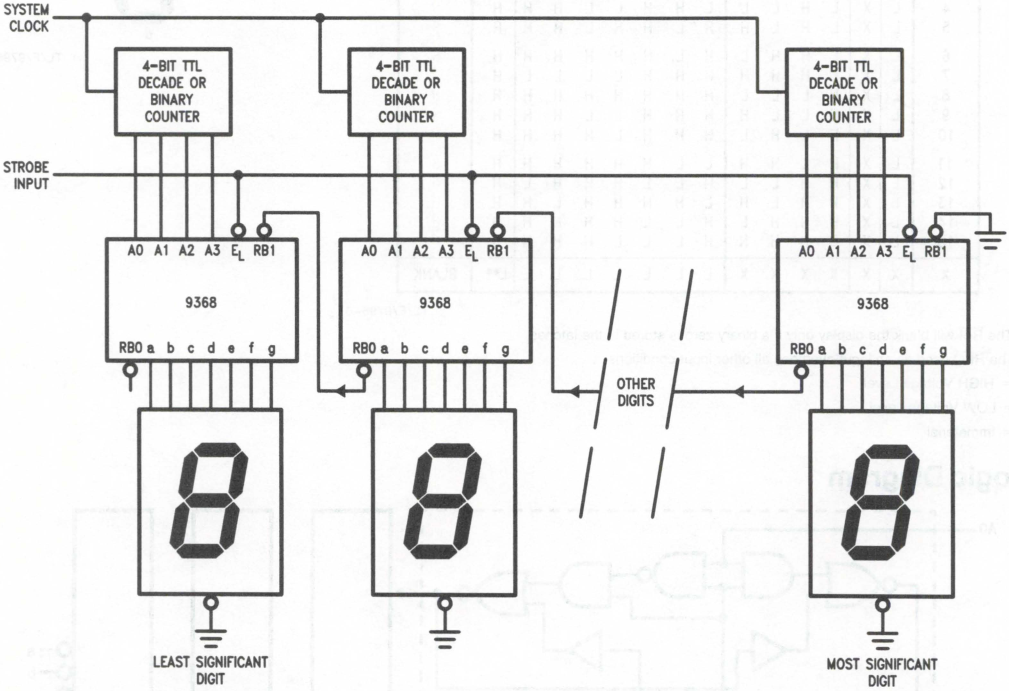
Numerical Designations


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
0 1 2 3 4 5 6 7 8 9 A b C d E F

TL/F/9796-5

Parallel Data Display System with Ripply Blanking

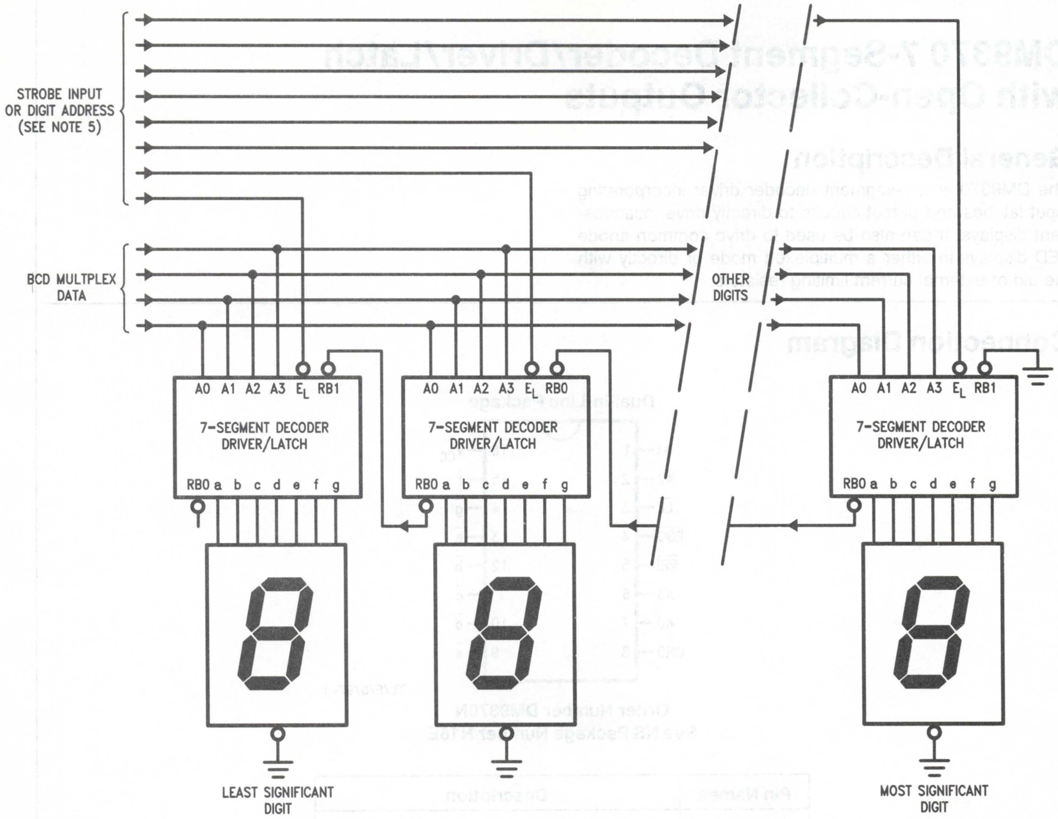
Common Cathode LED Display


SYSTEM CLOCK
STROBE INPUT
4-BIT TTL DECADE OR BINARY COUNTER
4-BIT TTL DECADE OR BINARY COUNTER
4-BIT TTL DECADE OR BINARY COUNTER
A0 A1 A2 A3 E_L RBI
9368
RBO a b c d e f g
A0 A1 A2 A3 E_L RBI
9368
RBO a b c d e f g
A0 A1 A2 A3 E_L RBI
9368
RBO a b c d e f g
OTHER DIGITS
LEAST SIGNIFICANT DIGIT
MOST SIGNIFICANT DIGIT

TL/F/9796-6

Display Demultiplexing System with Ripple Blanking

Common Cathode LED Display


STROBE INPUT OR DIGIT ADDRESS (SEE NOTE 5)
BCD MULTIPLEX DATA
OTHER DIGITS
A0 A1 A2 A3 $\overline{E}_L$ RBI
7-SEGMENT DECODER DRIVER/LATCH
RBO a b c d e f g
A0 A1 A2 A3 $\overline{E}_L$ RBO
7-SEGMENT DECODER DRIVER/LATCH
RBO a b c d e f g
A0 A1 A2 A3 $\overline{E}_L$ RBI
7-SEGMENT DECODER DRIVER/LATCH
RBO a b c d e f g
LEAST SIGNIFICANT DIGIT
MOST SIGNIFICANT DIGIT

TL/F/9796–7

Note: Digit address data must be non-overlapping. Standard TTL decoders like the 9301, 9311, 7442 or 74155 must be strobed, since the address decoding glitches could cause erroneous data to be strobed into the latches.

National Semiconductor

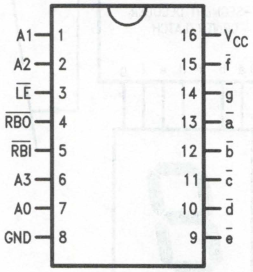
DM9370 7-Segment Decoder/Driver/Latch with Open-Collector Outputs

General Description

The DM9370 is a 7-segment decoder driver incorporating input latches and output circuits to directly drive incandescent displays. It can also be used to drive common anode LED displays in either a multiplexed mode or directly with the aid of external current limiting resistors.

Connection Diagram

Dual-in-Line Package



TL/F/9797-1

Order Number DM9370N
See NS Package Number N16E

Pin Names	Description
A0–A3	Address Inputs
$\overline{LE}$	Latch Enable Input (Active LOW)
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{RBO}$	Ripple Blanking as Output (Active LOW) as Input (Active LOW)
$\overline{a}$–$\overline{g}$	Segment Outputs (Active LOW)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The devic should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM9370			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−80	μA
I_{OL}	Low Level Output Current			3.2	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to $\overline{LE}$			30 20	ns
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to $\overline{LE}$			0 0	ns
t_w (L)	$\overline{LE}$ Pulse Width LOW			45	ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter		Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage		V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage		V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage		V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current		V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current		V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current		V_{CC} = Max (Note 2)	DM74	−20		−70	mA
V_{OH}	Output HIGH Voltage	$\overline{RBO}$	V_{CC} = Min, I_{OH} −80 μA		2.4			V
V_{OL}	Output LOW Voltage	$\overline{RBO}$	I_{OL} = 3.2 mA	V_{CC} = Min			0.4	V
		$\overline{a}-\overline{g}$	I_{OL} = 25 mA				0.4	
I_{OH}	Output HIGH Current, $\overline{a}-\overline{g}$						250	μA
I_{CC}	Power Supply Current		V_{CC} = Max				105	μA
			A_1, A_2, A_3, $\overline{LE}$ = GND V_{CC} = Max, Outputs Open				105	mA
			A_0, A_1, A_2, $\overline{LE}$ = GND V_{CC} = Max, Outputs Open				94	

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 PF R_L = 500Ω Min	C_L = 15 PF R_L = 500Ω Max	Units
t_{PLH}	Propagation Delay A_n to $\overline{a}-\overline{g}$		75	ns
t_{PHL}			50	
t_{PLH}	Propagation Delay $\overline{LE}$ to $\overline{a}-\overline{g}$		90	ns
t_{PHL}			70	

Functional Description

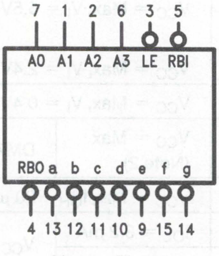
The '70 has active LOW outputs capable of sinking in excess of 25 mA which allows it to drive a wide variety of 7-segment incandescent displays directly. It may also be used to drive common anode LED displays, multiplexed or directly with the aid of suitable current limiting resistors. This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a hexadecimal decode format which produces numeric codes "0" through "9" and alpha codes "A" through "F" using upper and lower case fonts.

Latches on the four data inputs are controlled by an active LOW latch enable $\overline{LE}$. When the $\overline{LE}$ is LOW, the state of the outputs is determined by the input data. When the $\overline{LE}$ goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The $\overline{LE}$ pulse width necessary to accept and store data is typically 30 ns which allows data to be strobed into the '70 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

The latch/decoder combination is a simple system which drives incandescent displays with multiplexed data inputs from MOS time clocks, DVMs, calculator chips, etc. Data inputs are multiplexed while the displays are in static mode. This lowers component and insertion costs since several circuits—seven diodes per display, strobe drivers, a separate display voltage source, and clock failure detect circuits—traditionally found in incandescent multiplexed display systems are eliminated. It also allows low strobing rates to be used without display flicker.

Another '70 feature is the reduced loading on the data inputs when the Latch Enable is HIGH (only 10 μA typ). This allows many '70s to be driven from a MOS device in multiplex mode without the need for drivers on the data lines. The '70 also provides automatic blanking of the leading and/or trailing-edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an 8-digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading-edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$ of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing-edge zeroes. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

Logic Symbol



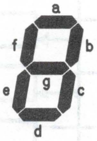
TL/F/9797-2

V_{CC} = Pin 16
GND = Pin 8

Truth Table

BINARY STATE	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	A3	A2	A1	A0	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	$\overline{RBO}$	
--	H	*	X	X	X	X	← STABLE →							H	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	H	H	L	L	H	9
10	L	X	H	L	H	L	L	L	L	H	L	L	L	H	A
11	L	X	H	L	H	H	H	H	L	L	L	L	L	H	b
12	L	X	H	H	L	L	L	H	H	L	L	L	H	H	C
13	L	X	H	H	L	H	H	L	L	L	L	H	L	H	d
14	L	X	H	H	H	L	L	H	H	L	L	L	L	H	E
15	L	X	H	H	H	H	L	H	H	H	L	L	L	H	F
X	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	BLANK

TL/F/9797-6



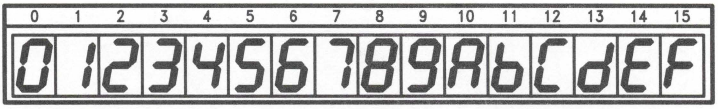
TL/F/9797-4

*The $\overline{RBI}$ will blank the display only if binary zero is stored in the latches.

**$\overline{RBO}$ used as an input overdrives all other input conditions.

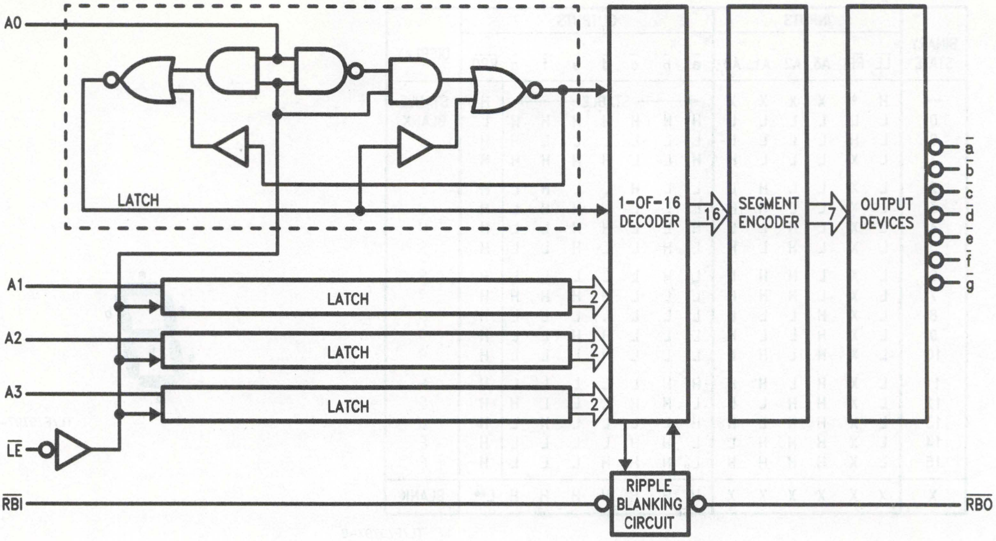
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Numerical Designation



TL/F/9797-5

Logic Diagram


A0
LATCH
A1
LATCH
A2
LATCH
A3
LATCH
LE
2
2
2
1-OF-16 DECODER
16
SEGMENT ENCODER
7
OUTPUT DEVICES
a
b
c
d
e
f
g
RBI
RIPPLE BLANKING CIRCUIT
RBO

TL/F/9797-3

National Semiconductor

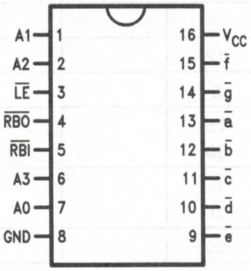
DM9374 7-Segment Decoder/Driver/Latch with Constant Current Sink Outputs

General Description

The '74 is a 7-segment decoder driver incorporating input latches and output circuits to directly drive common anode LED displays.

Connection Diagram

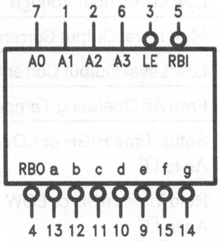
Dual-In-Line Package


A1 1
A2 2
$\overline{LE}$ 3
$\overline{RBO}$ 4
$\overline{RBI}$ 5
A3 6
A0 7
GND 8
16 V_{CC}
15 $\overline{f}$
14 $\overline{g}$
13 $\overline{a}$
12 $\overline{b}$
11 $\overline{c}$
10 $\overline{d}$
9 $\overline{e}$

TL/F/10210-1

Order Number DM9374N
See NS Package Number N16E

Logic Symbol


7 1 2 6 3 5
A0 A1 A2 A3 LE RBI
RBO a b c d e f g
4 13 12 11 10 9 15 14

TL/F/10210-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A3	Address (Data Inputs)
$\overline{LE}$	Latch Enable Input (Active LOW)
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{RBO}$	Ripple Blanking as Output (Active LOW) as Input (Active LOW)
$\overline{a}$–$\overline{g}$	Constant Current Outputs (Active LOW)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{OUT}	Output Voltage Applied	OFF			10	V
		ON			*(Figure A)*	
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current, $\overline{a}-\overline{g}$, $V_{OUT} = 5.5V$				250	µA
I_{OL}	Low Level Output Current, $\overline{a}-\overline{g}$, $V_{OL} = 3.0V$		12		18	mA
T_A	Free Air Operating Temperature		0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW An to $\overline{LE}$		75 30			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW An to $\overline{LE}$		0 0			ns
t_w (L)	$\overline{LE}$ Pulse Width LOW		85			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -12$ mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−18		−57	mA
I_{CCH}	Supply Current	V_{CC} = Max, V_{IN} = 0V, V_{OUT} = 3.0V			50	mA

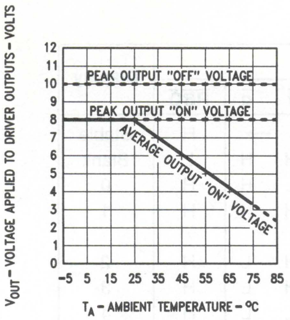
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

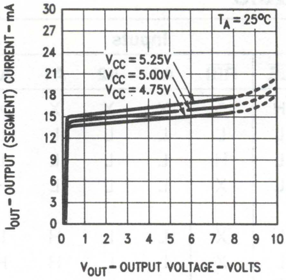
V_{CC} = +5.0V, T_A = +25°C (See Section 1 for test waveforms and output load)

Symbol	Parameter	C_L = 15 pF, R_L = 1 kΩ Min	Max	Units
t_{PLH} t_{PHL}	Propagation Delay An to $\overline{a}-\overline{g}$		140 140	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$ to $\overline{a}-\overline{g}$		140 140	ns



TL/F/10210-9

FIGURE A. Output Voltage Safe Operating Area



TL/F/10210-10

FIGURE B. Typical Constant Segment Current Versus Output Voltage

Functional Description

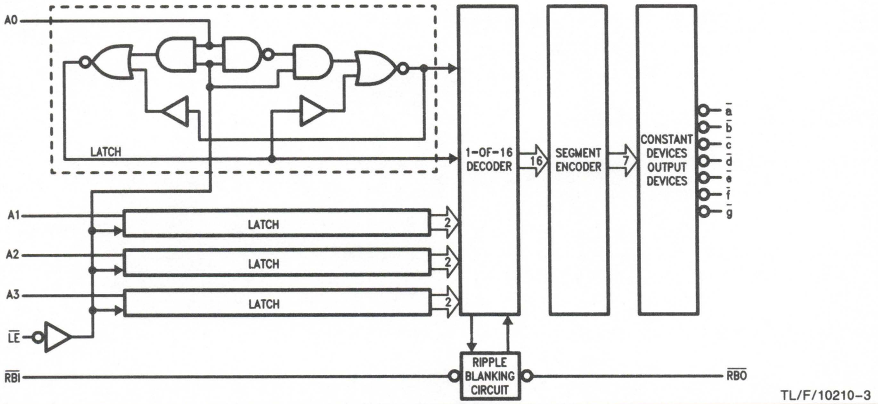
The '9374 is a 7-segment decoder/driver with latches on the address inputs and active LOW constant current outputs to drive LEDs directly. This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a decode format which produces numeric codes "0" through "9" and other codes.

Latches on the four data inputs are controlled by an active LOW Latch Enable, $\overline{\text{LE}}$. When $\overline{\text{LE}}$ is LOW, the state of the outputs is determined by the input data. When $\overline{\text{LE}}$ goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The $\overline{\text{LE}}$ pulse width necessary to accept and store data is typically 50 ns, which allows data to be strobed into the '74 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

The latch/decoder combination is a simple system which drives LED displays with multiplexed data inputs from MOS time clocks, DVMs, calculator chips, etc. Data inputs are multiplexed while the displays are in static mode. This lowers component and insertion costs, since several circuits—seven resistors per display, strobe drivers, a separate display voltage source, and clock failure detect circuits—traditionally found in multiplexed display systems are eliminated. It also allows low strobing rates to be used without display flicker.

Another '74 feature is the reduced loading on the data inputs when the Latch Enable is HIGH (only 10 μA typ). This allows many '74s to be driven from a MOS device in multiplex mode without the need for drivers on the data lines. The '74 also provides automatic blanking of the leading and/or trailing-edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an 8-digit mixed integer fraction decimal representation, using the automatic blanking capability 0060.0300 would be displayed as 60.03. Leading-edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{\text{RBO}}$) of a decoder to the Ripple Blanking Input ($\overline{\text{RBI}}$) of the next lower stage device. The most significant decoder stage should have the $\overline{\text{RIB}}$ input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the $\overline{\text{RBI}}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing-edge zeroes. The $\overline{\text{RBO}}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

Logic Diagram



TL/F/10210-3

Truth Table

Binary State	Inputs						Outputs								Display
	$\overline{LE}$	$\overline{RBI}$	A3	A2	A1	A0	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	$\overline{RBO}$	
—	H	*	X	X	X	X	←			STABLE			→	H	Stable
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	Blank
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	—
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	BLANK
X	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	BLANK

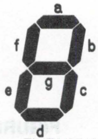
*The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.

**$\overline{RBO}$ used as an input overrides all other input conditions.

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial



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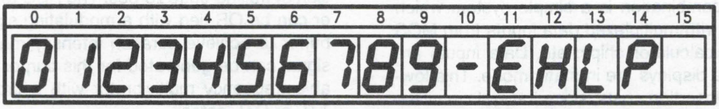
Numerical Designations



TL/F/10210-5

Applications

It is possible with common anode 7-segment LED displays and constant current sink decoder drivers to save substantial amounts of power by carefully choosing operating points on display supply voltage. First, examine the power used in the normal display driving method where the display and decoder driver are both operated from a +5.0V regulated supply ($V_{CC} = V_S$).

The power dissipated by the LED and the driver outputs is ($V_{CC} \times I_{seg} \times$ n Segments). The total power dissipated with a 15 mA LED displaying an eight (8) would be:

$$\begin{aligned} P_{TOT} &= 5.0V \times 15\ mA \times 7 \\ &= 525\ mW \end{aligned}$$

Of this 525 mW, the power actually required to drive the LED is dependent on the V_F drop of each segment. Most GaAsP LEDs exhibit either a 1.7V or a 3.4V forward voltage drop. Therefore, the required total power for seven segments would be:

$$\begin{aligned} P_{(1.7)} &= 1.7V \times 15\ mA \times 7 \\ &= 178.5\ mW \\ P_{(3.4)} &= 3.4V \times 15\ mA \times 7 \\ &= 357\ mW \end{aligned}$$

The remaining power is dissipated by the driver outputs which are maintaining the 15 mA constant current required by the LEDs. Most of this power is wasted, since the driver can maintain approximately 15 mA with as little as 0.5V across the output device. By using a separate power source (V_S, *Figure C*) for the LEDs, which is set to the LED V_F plus the offset voltage of the driver, as much as 280 mW can be saved per digit. i.e.,

$$\begin{aligned} V_S &= V_F\ (Max) + V_{offset} \\ &= 2.0V + 0.5V \\ &= 2.5V \\ P_T &= 2.5V \times 14\ mA\ (\text{from } \textit{Figure B}) \times 7 \\ &= 245\ mW \end{aligned}$$

These figures show that using a separate supply to drive the LEDs can offer significant display power savings. In battery powered equipment, two rechargeable nickle-cadmium cells in series would be sufficient to drive the display, while four such cells would be needed to operate the logic units.

Another method to save power is to apply intensity modulation to the displays *(Figure D)*. It is well known that LED displays are more efficient when operated in pulse mode. There are two reasons: one, the quantum efficiency of the LED material is better; secondly the eye tends to peak detect. Typically a 20% off duty cycle to displays (GaAsP) will produce the same brightness as operating under dc conditions.

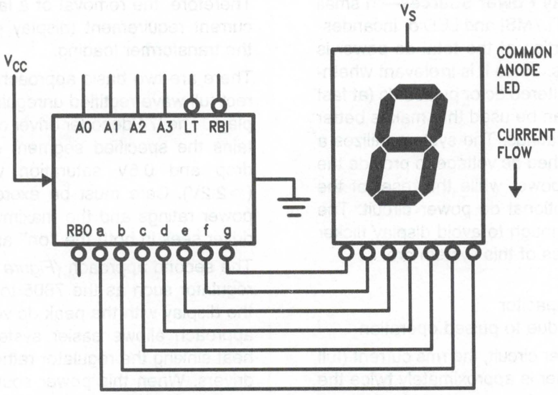


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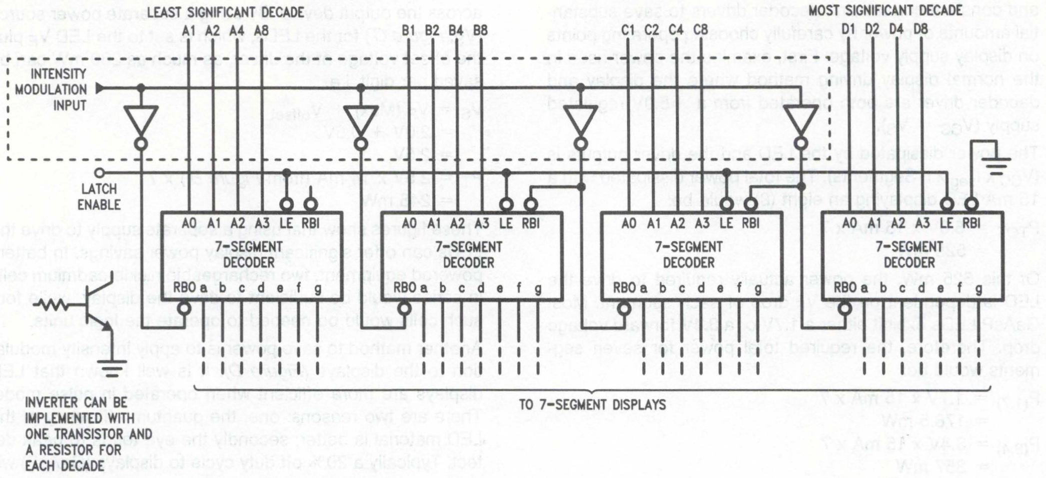
FIGURE C. Separate Supply for LED Displays

Applications (Continued)


LEAST SIGNIFICANT DECADE
A1 A2 A4 A8
B1 B2 B4 B8
C1 C2 C4 C8
MOST SIGNIFICANT DECADE
D1 D2 D4 D8
INTENSITY MODULATION INPUT
LATCH ENABLE
A0 A1 A2 A3 LE RBI
7-SEGMENT DECODER
RBO a b c d e f g
INVERTER CAN BE IMPLEMENTED WITH ONE TRANSISTOR AND A RESISTOR FOR EACH DECADE
TO 7-SEGMENT DISPLAYS

TL/F/10210-6

All Inverters are DTL 9936 or Open Collector TTL 7405

FIGURE D. Intensity Control by $\overline{\text{RBO}}$ Pulse Duty Cycle

Low Power, Low Cost Display Power Sources—In small line operated systems using TTL/MSI and LED or incandescent displays, a significant portion of the total dc power is consumed to drive the displays. Since it is irrelevant whether displays are driven from unfiltered dc or pulsed dc (at fast rates), a dual power system can be used that makes better utilization of transformer rms ratings. The system utilizes a full wave rectified but unsmoothed dc voltage to provide the displays with 120 Hz pulsed power while the reset of the system is driven by a conventional dc power circuit. The frequency of 120 Hz is high enough to avoid display flicker problems. The main advantages of this system are:

- Reduced transformer rating
- Much smaller smoothing capacitor
- Increased LED light output due to pulsed operation

With the standard capacitor filter circuit, the rms current (full wave) loading of the transformer is approximately twice the dc output. Most commercial transformer manufacturers rate transformers with capacitive input filters as follows:

Full Wave Bridge Rectifier Circuit
  Transformer rms current = 1.8 x dc current required

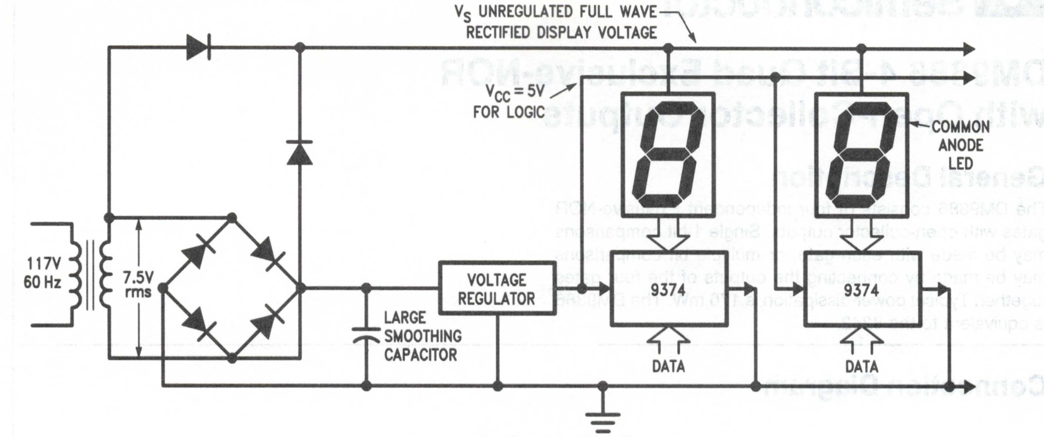
Full Wave Center Tapped Rectifier Circuit
  Transformer rms current = 1.2 x dc current required

Therefore, the removal of a large portion of the filtered dc current requirement (display power) substantially reduces the transformer loading.

There are two basic approaches. First *(Figure E)* is the direct full wave rectified unregulated supply to power the displays. The '74 decoder driver constant current feature maintains the specified segment current after the LED diode drop and 0.5V saturation voltage has been reached (≅2.2V). Care must be exercised not to exceed the '74 power ratings and the maximum voltage that the decoder driver sees in both the "on" and "off" modes.

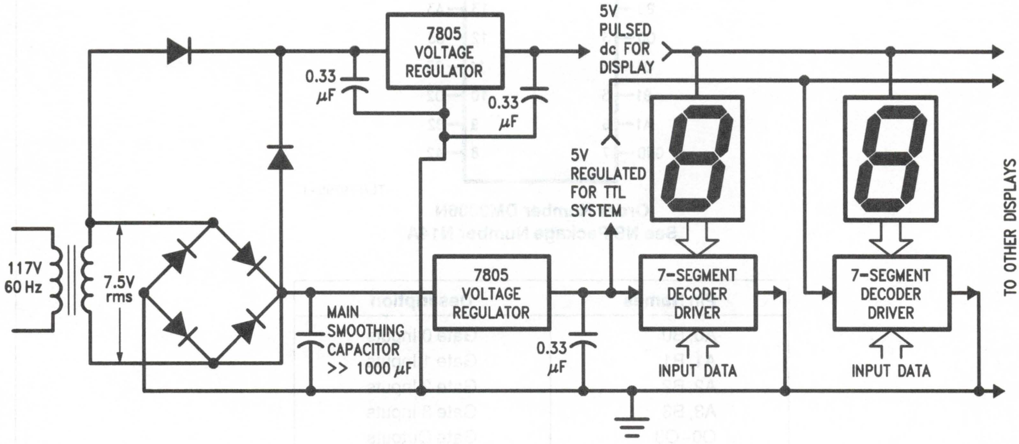
The second approach *(Figure F)* uses a 3-terminal voltage regulator such as the 7805 to provide dc pulsed power to the display with the peak dc voltage limited to +5.0V. This approach allows easier system thermal management by heat sinking the regulator rather than the display or display drivers. When this power source is used with an intensity modulation scheme or with a multiplexed display system, the frequencies must be chosen such that they do not beat with the 120 Hz full wave rectified power frequency.

Applications (Continued)


V$_S$ UNREGULATED FULL WAVE RECTIFIED DISPLAY VOLTAGE
V$_{CC}$ = 5V FOR LOGIC
COMMON ANODE LED
117V 60 Hz
7.5V rms
VOLTAGE REGULATOR
LARGE SMOOTHING CAPACITOR
9374
DATA
9374
DATA

TL/F/10210-7

FIGURE E. Direct Unregulated Display Supply


7805 VOLTAGE REGULATOR
0.33 μF
0.33 μF
5V PULSED dc FOR DISPLAY
5V REGULATED FOR TTL SYSTEM
117V 60 Hz
7.5V rms
MAIN SMOOTHING CAPACITOR >> 1000 μF
7805 VOLTAGE REGULATOR
0.33 μF
7-SEGMENT DECODER DRIVER
INPUT DATA
7-SEGMENT DECODER DRIVER
INPUT DATA
TO OTHER DISPLAYS

TL/F/10210-8

FIGURE F. Pulsed Regulated Display Supply

National Semiconductor

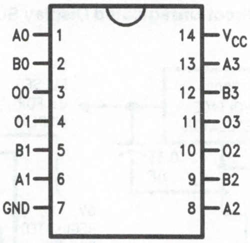
DM9386 4-Bit Quad Exclusive-NOR with Open-Collector Outputs

General Description

The DM9386 consists of four independent Exclusive-NOR gates with open-collector outputs. Single 1-bit comparisons may be made with each gate, or multiple bit comparisons may be made by connecting the outputs of the four gates together. Typical power dissipation is 170 mW. The DM9386 is equivalent to the 8242.

Connection Diagram

Dual-In-Line Package



TL/F/9798-1

Order Number DM9386N
See NS Package Number N14A

Pin Names	Description
A0, B0	Gate 0 Inputs
A1, B1	Gate 1 Inputs
A2, B2	Gate 2 Inputs
A3, B3	Gate 3 Inputs
O0–O3	Gate Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current	−0.150		−0.150	mA
I_{OL}	Low Level Output Current			25	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			80	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−18		−57	mA
I_{CC}	Supply Curent	V_{CC} = Max, V_{IN}(A), V_{IN}(B) = 0.4V			47.5	mA

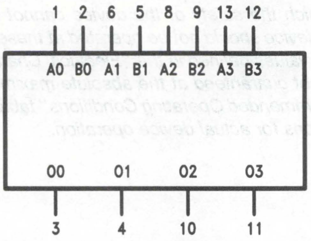
Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 30 pF R_L = 530Ω		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			25	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Logic Symbol


1
2
6
5
8
9
13
12
A0
B0
A1
B1
A2
B2
A3
B3
O0
O1
O2
O3
3
4
10
11

TL/F/9798-2

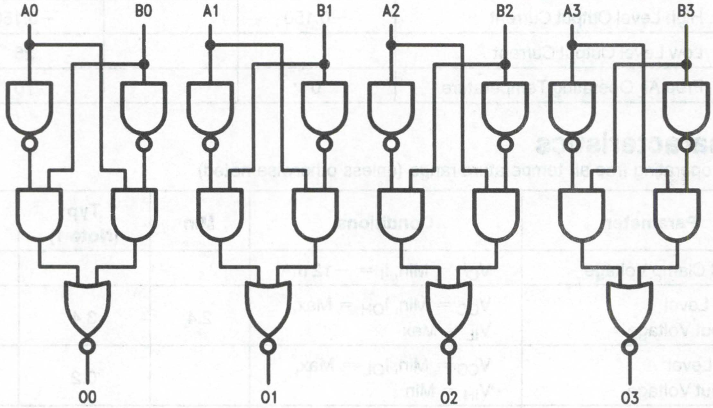
V_{CC} = Pin 14
GND = Pin 7

Truth Table

Inputs		Output
An	**Bn**	**On**
L	L	H
H	L	L
L	H	L
H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram


A0
B0
A1
B1
A2
B2
A3
B3
O0
O1
O2
O3

TL/F/9798-3

National Semiconductor

9601/DM9601 Retriggerable One Shot

General Description

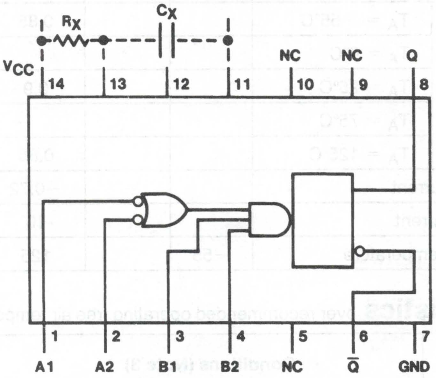
These retriggerable one shots provide the designer with four inputs; two active high and two active low. This permits a choice of either leading-edge or trailing-edge triggering, independent of input transition times. When input conditons for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge again. The retriggerable feature allows for output pulse widths to be expanded. In fact a continuous true output can be maintained by having an input cycle time which is shorter than the output cycle time. Retriggering may be inhibited by tying the $\overline{Q}$ output to an active low input.

Features

- High speed operation—input repetition rate > 10 MHz
- Flexibility of operation—optional retriggering/lock-out capability
- Output pulse width range—50 ns to ∞
- Leading or trailing edge triggering
- Complementary outputs/inputs
- Input clamping diodes
- DTL/TTL compatible logic levels
- Alternate Military/Aerospace device (9601) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6610-1

Order Number 9601DMQB, 9601FMQB, DM9601J, DM9601W or DM9601N
See NS Package Number J14A, N14A or W14B

Function Table

Inputs				Outputs	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⊓	⊔
L	X	H	↑	⊓	⊔
X	L	H	H	L	H
X	L	↑	H	⊓	⊔
X	L	H	↑	⊓	⊔
H	↓	H	H	⊓	⊔
↓	↓	H	H	⊓	⊔
↓	H	H	H	⊓	⊔

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
↑ = Low to High Level Transition
↓ = High to Low Level Transition
⊓ = Positive Pulse
⊔ = Negative Pulse

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0° to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	$T_A = -55°C$	2						V
		$T_A = 0°C$				1.9			
		$T_A = 25°C$	1.7			1.8			
		$T_A = 75°C$				1.6			
		$T_A = 125°C$	1.5						
V_{IL}	Low Level Input Voltage	$T_A = -55°C$			0.85				V
		$T_A = 0°C$						0.85	
		$T_A = 25°C$			0.9			0.85	
		$T_A = 75°C$						0.85	
		$T_A = 125°C$			0.85				
I_{OH}	High Level Output Current				−0.72			−0.96	mA
I_{OL}	Low Level Output Current				10			12.8	mA
T_A	Free Air Operating Temperature		−55		125	0		75	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (Note 3)		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min, (Note 4)		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min (Note 4)	MIL			0.4	V
			COM			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V				60	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	MIL V_{IN} = 0.40V			−1.6	mA
			COM V_{IN} = 0.45V			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Notes 2 and 4)	MIL	−10		−40	mA
			COM	−10		−40	
I_{CC}	Supply Current	V_{CC} = Max				25	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: Unless otherwise noted, R_X = 10k between PIN 13 and V_{CC} on all tests.

Note 4: Ground PIN 11 for V_{OL} test on PIN 6, V_{OH} and I_{OS} tests on PIN 8. Open PIN 11 for V_{OL} test on PIN 8, V_{OH} and I_{OS} tests on PIN 6.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Negative Trigger Input to True Output	C_L = 15 pF C_X = 0 R_X = 5 kΩ		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Negative Trigger Input to Complement Output			40	ns
$t_{PW(MIN)}$	Minimum True Output Pulse Width				65	ns
t_{PW}	Pulse Width		R_X = 10 kΩ C_X = 1000 pF	3.08	3.76	μs
C_{STRAY}	Maximum Allowable Wiring Capacitance		Pin 13 to GND		50	pF
R_X	External Timing Resistor		DM96		25	kΩ
R_X	External Timing Resistor		DM86		50	kΩ

Operating Rules

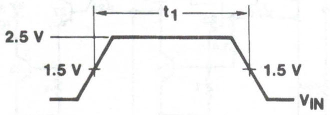
1. An external resistor R_X and an external capacitor C_X are required for operation. The value of R_X can vary between the limits shown in switching characteristics. The value of C_X is optional and may be adjusted to achieve the required output pulse width.
2. Output pulse width t_{PW} may be calculated as follows:

   $$t_{PW} = K R_X C_X \left[1 + \frac{0.7}{R_X}\right] \text{(for } C_X > 10^3 \text{ pF)} \quad K \approx 0.34$$

   R_X in kΩ, C_X in pF and t_{PW} in ns.

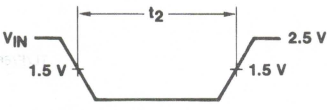
   (For $C_X < 10^3$ pF, see curve.)
3. R_X and C_X must be kept as close as possible to the circuit in order to minimize stray capacitance and noise pickup. If remote trimming is required, R_X may be split up such that at least $R_{X(MIN)}$ must be as close as possible to the circuit and the remote portion of the trimming resistor $R < R_{X(MAX)} - R_X$.
4. Set-up time (t_1) for input trigger pulse must be > 40 ns. (See *Figure 1*).

   Release time (t_2) for input trigger pulse must be > 40 ns. (See *Figure 2*).



TL/F/6610–2

FIGURE 1

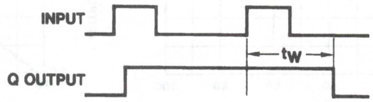


TL/F/6610–3

FIGURE 2

5. Retrigger pulse width (see *Figure 3*) is calculated as follows:

   $$t_W = t_{PW} + t_{PLH} = K R_X C_X \left[1 + \frac{0.7}{R_X}\right] + t_{PLH}$$

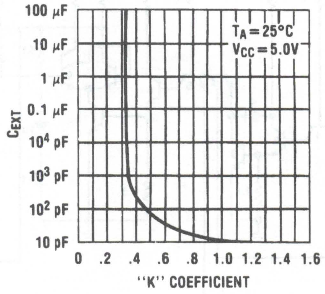


TL/F/6610–4

FIGURE 3

Typical "K" Coefficient Variation vs Timing Capacitance

The multiplicative factor "K" varies as a function of the timing capacitor, C_X. The graph below details this characteristic:

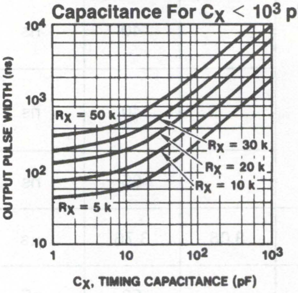


TL/F/6610–5

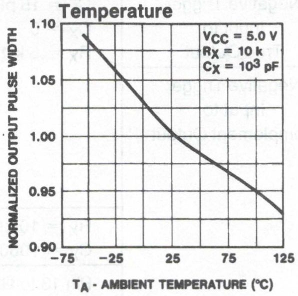
*For further detailed device characteristics and output performance, please refer to the NSC one-shot application note, AN-366.

Typical Performance Characteristics

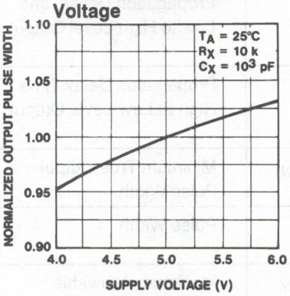
Output Pulse Width vs Timing Resistance And Capacitance For $C_X < 10^3$ pF



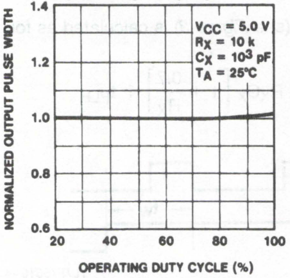
Normalized Output Pulse Width vs Ambient Temperature



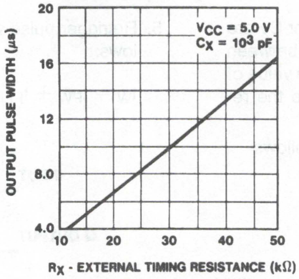
Normalized Output Pulse Width vs Supply Voltage



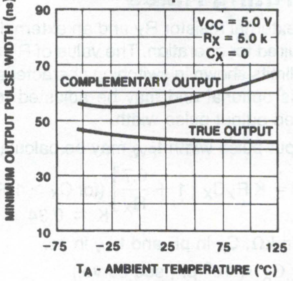
Normalized Output Pulse Width vs Operating Duty Cycle



Pulse Width vs Timing Resistance

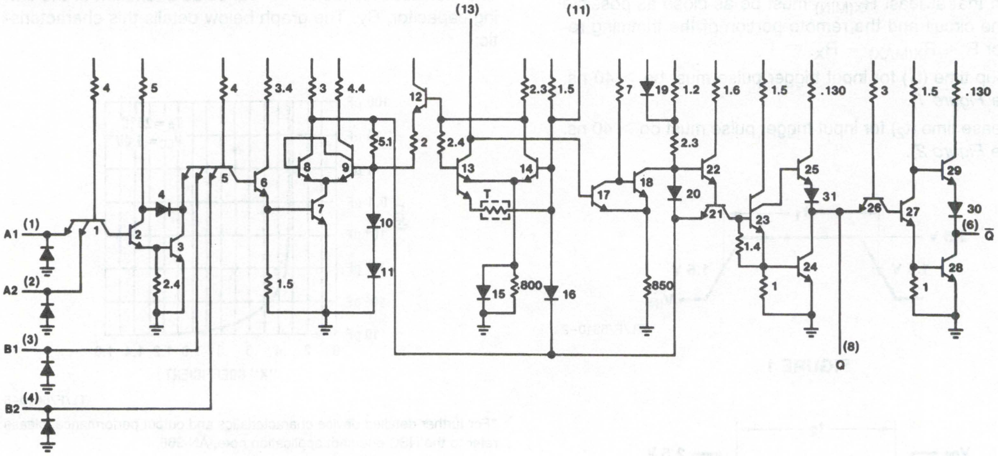


Output Pulse Width vs Ambient Temperature



TL/F/6610-6

Schematic Diagram



(13)
(11)
A1 (1)
A2 (2)
B1 (3)
B2 (4)
(6) $\overline{Q}$
(8) Q
4
5
4
3.4
3
4.4
5.1
2
2.4
2.3
1.5
7
19
1.2
1.6
1.5
.130
3
1.5
.130
2.4
1.5
800
850
2.3
1.4
1
1
1
2
3
4
5
6
7
8
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TL/F/6610-7

National Semiconductor

9602/DM9602 Dual Retriggerable, Resettable One Shots

General Description

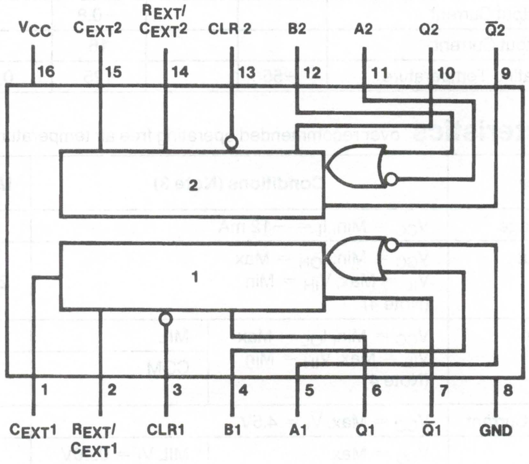
These dual resettable, retriggerable one shots have two inputs per function; one which is active high, and one which is active low. This allows the designer to employ either leading-edge or trailing-edge triggering, which is independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is allowed to rapidly discharge and then charge again. The retriggerable feature permits output pulse widths to be extended. In fact a continuous true output can be maintained by having an input cycle time which is shorter than the output cycle time. The output pulse may then be terminated at any time by applying a low logic level to the RESET pin. Retriggering may be inhibited by either connecting the Q output to an active high input, or the $\overline{Q}$ output to an active low input.

Features

- 70 ns to ∞ output width range
- Resettable and retriggerable—0% to 100% duty cycle
- TTL input gating—leading or trailing edge triggering
- Complementary TTL outputs
- Optional retrigger lock-out capability
- Pulse width compensated for V_{CC} and temperature variations
- Alternate Military/Aerospace device (54xxx) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6611–1

Order Number 9602DMQB, 9602FMQB or DM9602N
See NS Package Number J16A, N16E or W16A

Function Table

Pin No's.			Operation
A	B	CLR	
H → L	L	H	Trigger
H	L → H	H	Trigger
X	X	L	Reset

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	$T_A = -55°C$	2						V
		$T_A = 0°C$				1.9			
		$T_A = 25°C$	1.7			1.8			
		$T_A = 75°C$				1.65			
		$T_A = 125°C$	1.5						
V_{IL}	Low Level Input Voltage	$T_A = -55°C$			0.85				V
		$T_A = 0°C$						0.85	
		$T_A = 25°C$			0.9			0.85	
		$T_A = 75°C$						0.85	
		$T_A = 125°C$			0.85				
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
T_A	Free Air Operating Temperature		−55		125	0		75	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (Note 3)		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -12\text{ mA}$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$ (Note 4)		2.4			V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$ (Note 4)	MIL			0.4	V
			COM			0.45	
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 4.5V$				60	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}$	MIL $V_I = 0.40V$			−1.6	mA
			COM $V_I = 0.45V$			−1.6	
		$V_{CC} = \text{Min}$	MIL $V_I = 0.40V$			−1.24	
			COM $V_I = 0.45V$			−1.41	
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}, V_{OUT} = 1V$ (Notes 2 and 4)	MIL			−25	mA
			COM			−35	
I_{CC}	Supply Current	$V_{CC} = \text{Max}$	MIL		39	45	mA
			COM		39	50	

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time.

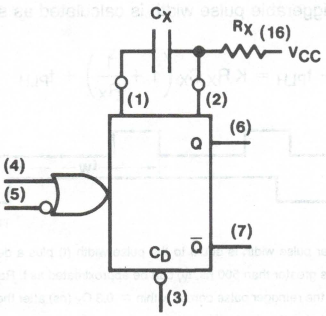
Note 3: Unless otherwise noted, $R_X = 10k$ for all tests.

Note 4: Ground PIN 1(15) for V_{OL} on PIN 7(9) or V_{OH} and I_{OS} on PIN 6(10) and apply momentary ground to PIN 4(12). Open PIN 1(15) for V_{OL} on PIN 6(10) or V_{OH} and I_{OS} on PIN 7(9).

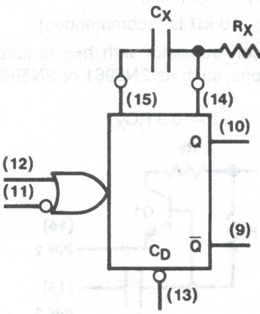
Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		Conditions	Military		Commercial		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Negative Trigger Input to True Output	$C_L = 15$ pF $C_X = 0$ $R_X = 5$ kΩ		35		40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Negative Trigger Input To Complement Output			43		48	ns
t_{PW}(MIN)	Minimum True Output Pulse Width				90		100	ns
	Minimum Complement Pulse Width				100		110	
t_{PW}	Pulse Width		$R_X = 10$ kΩ $C_X = 1000$ pF	3.08	3.76	3.08	3.76	μs
C_{STRAY}	Maximum Allowable Wiring Capacitance		Pins 2, 14 to GND		50		50	pF
R_X	External Timing Resistor			5	25	5	50	kΩ

Logic Diagrams



TL/F/6611–2



TL/F/6611–3

Operating Rules

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
3. The output pulse with (t) is defined as follows:

$$t = K R_X C_X \left[1 + \frac{1}{R_X}\right] \quad \text{for } C_X > 10^3 \text{ pF}, \; K \approx 0.34$$

where: R_X is in kΩ, C_X is in pF

t is in ns

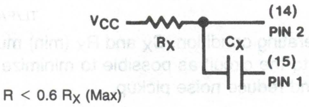
for $C_X < 10^3$ pF, see *Figure 1.*

for K vs C_X see *Figure 6.*

4. If electrolytic type capacitors are to be used, the following three configurations are recommended:

   A. Use with low leakage capacitors:

   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0V is less than 3 μA, and the inverse capacitor leakage at 1.0V is less than 5 μA over the operational temperature range.



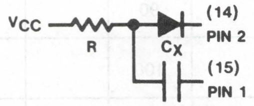
TL/F/6611–4

Operating Rules (Continued)

B. Use with high inverse leakage current electrolytic capacitors:

The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.

$t \approx 0.3\ RC_X$


VCC
R
CX
(14)
PIN 2
(15)
PIN 1

TL/F/6611-5

C. Use to obtain extended pulse widths:

This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.

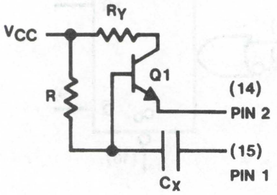
$R < R_X\ (0.7)\ (h_{FE}\ Q1)$ or $< 2.5\ M\Omega$, whichever is the lesser

$R_X\ (min) < R_Y < R_X\ (max)$

$(5\ k\Omega \le R_Y \le 10\ k\Omega$ is recommended)

Q1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962.

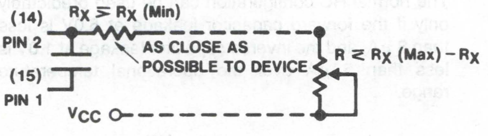
$t \approx 0.3\ RC_X$


RY
VCC
Q1
R
(14)
PIN 2
(15)
PIN 1
CX

TL/F/6611-6

This configuration is not recommended with retriggerable operation.

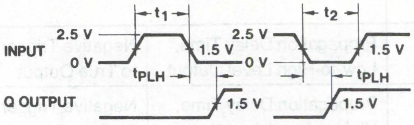
5. To obtain variable pulse width by remote trimming, the following circuit is recommended:


(14)
PIN 2
(15)
PIN 1
RX ≥ RX (Min)
AS CLOSE AS
POSSIBLE TO DEVICE
R ≤ RX (Max) − RX
VCC

TL/F/6611-7

6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

7. Input Trigger Pulse Rules (See Triggering Truth Table)


t1
t2
2.5 V
INPUT
0 V
1.5 V
2.5 V
0 V
1.5 V
tPLH
tPLH
Q OUTPUT
1.5 V
1.5 V

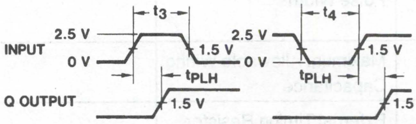
TL/F/6611-8

Input to Pin 5(11), (Pin 3(13) = HIGH)

Pin 4(12) = LOW

t_1, t_3 = Min. Positive Input Pulse Width > 40 ns

t_2, t_4 = Min. Negative Input Pulse Width > 40 ns


t3
t4
2.5 V
INPUT
0 V
1.5 V
2.5 V
0 V
1.5 V
tPLH
tPLH
Q OUTPUT
1.5 V
1.5 V

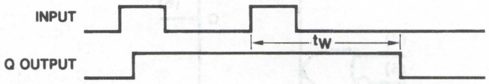
TL/F/6611-9

Input to Pin 4(12) (Pin 3(13) = HIGH)

Pin 5(11) = HIGH

8. The retriggerable pulse width is calculated as shown below:

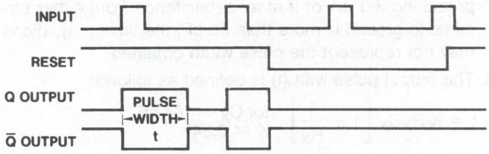
$$t_W = t + t_{PLH} = K\,R_X\,C_X\left(1 + \frac{1}{R_X}\right) + t_{PLH}$$


INPUT
tW
Q OUTPUT

TL/F/6611-10

The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, t_W can be approximated as t. Retriggering will not occur if the retrigger pulse comes within $\approx 0.3\ C_X$ (ns) after the initial trigger pulse (i.e., during the discharge cycle).

9. Reset Operation—An overriding clear (active LOW level) is provided on each one shot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.

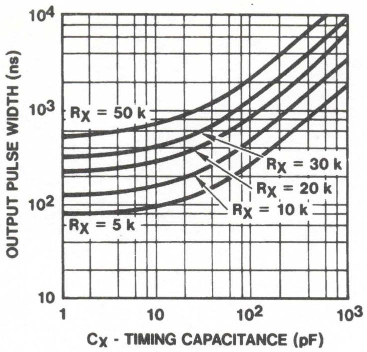

INPUT
RESET
Q OUTPUT
PULSE
WIDTH
t
Q̄ OUTPUT

TL/F/6611-11

10. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one shots. Use of a 0.01 to 0.1 µF bypass capacitor between V_{CC} and Ground located near the DM9602 is recommended.

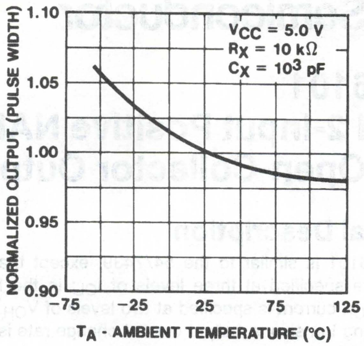
*For further detailed device characteristics and output performance, please refer to the NSC one-shot application note, AN-366.

Typical Performance Characteristics



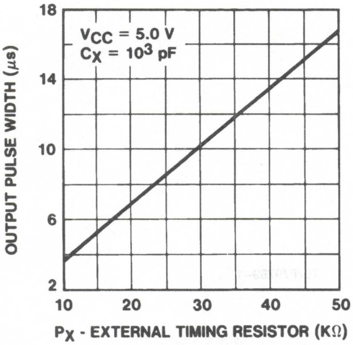
TL/F/6611-12

FIGURE 1. Output Pulse Width vs Timing Resistance and Capacitance for $C_X < 10^3$ pF



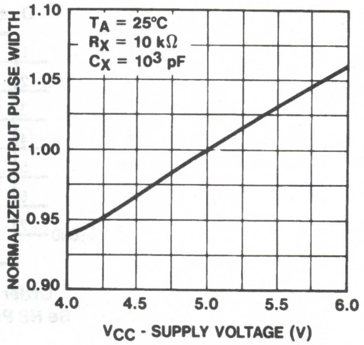
TL/F/6611-13

FIGURE 2. Normalized Output Pulse Width vs Ambient Temperature



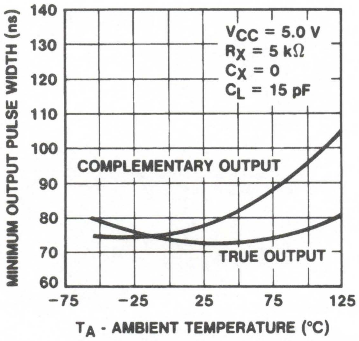
TL/F/6611-14

FIGURE 3. Pulse Width vs Timing Resistor



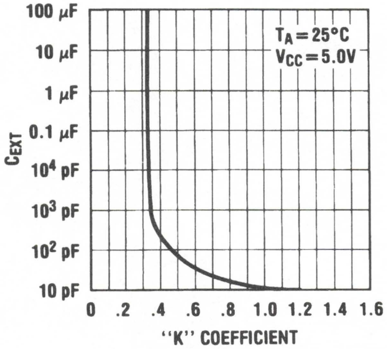
TL/F/6611-15

FIGURE 4. Normalized Output Pulse Width vs Supply Voltage



TL/F/6611-16

FIGURE 5. Minimum Output Pulse Width vs Ambient Temperature



TL/F/6611-17

FIGURE 6. Typical "K" Coefficient Variation vs Timing Capacitance

National Semiconductor

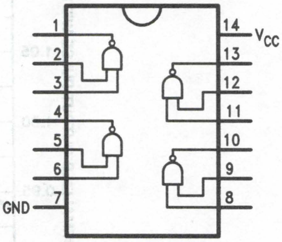
DM96101
Quad 2-Input Positive NAND Buffer with Open-Collector Output

General Description

The DM96101 is similar to the 54/7439, except that the outputs are specified at three levels of I_{OL}; in the HIGH state the I_{OH} current is specified at two levels of V_{OH}. During switching transitions, output current change rate is typically 4.0 mA/ns.

Connection Diagram

Dual-In-Line Package



TL/F/9799-1

Order Number DM96101N
Se NS Package Number N14A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.05	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = V_{IN}	I_{OL} = 48 mA			0.4	V
			I_{OL} = 60 mA			0.5	
			I_{OL} = 80 mA			0.6	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1000	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−18		−57	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max, V_{IN} = 0V				8.5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max, V_{IN} = Open				54	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF R_L = 120Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			25	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Section 5
TTL - Low Power

Section 5—TTL - Low Power

TTL (Low Power)—Mil/Aero

DM54L00 Quad 2-Input NAND Gate 5-3
DM54L02 Quad 2-Input NOR Gate 5-5
DM54L04 Hex Inverter 5-7
DM54L10 Triple 3-Input NAND Gate 5-9
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DM54L73 Dual J-K Flip-Flop with Clear and Complementary Outputs 5-14
DM54L74 Dual Positive-Edge-Triggered D Flip-Flop with Preset, Clear, and Complementary Outputs 5-17
DM54L93 4-Bit Binary Counter 5-20
DM54L95 4-Bit Parallel Access Shift Register 5-23
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National Semiconductor

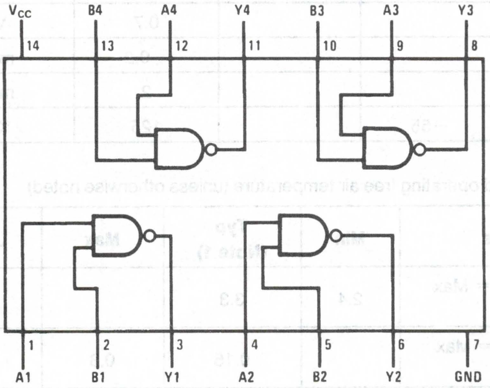
DM54L00
Quad 2-Input NAND Gates

General Description

This device contains four independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package


VCC
B4
A4
Y4
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
Y1
A2
B2
Y2
GND

TL/F/6654–1

Order Number DM54L00J or DM54L00W
See NS Package Number J14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range DM57L	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54L00			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−0.2	mA
I_{OL}	Low Level Output Current			2	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Ouput Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.15	0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−3		−15	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		0.44	0.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		1.16	2.04	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one should be shorted at a time.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Low to High Level Output	R_L = 4 kΩ C_L = 50 pF		60	ns
t_{PHL}	Propagation Delay High to Low Level Output			60	ns

National Semiconductor

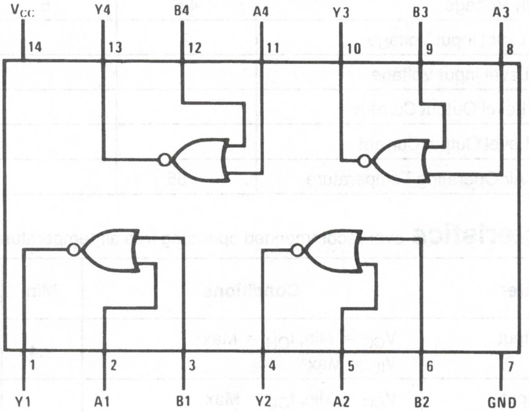
DM54L02 Quad 2-Input NOR Gates

General Description

This device contains four independent gates each of which performs the logic NOR function.

Connection Diagram

Dual-In-Line Package



V_{CC}
Y4
B4
A4
Y3
B3
A3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
Y1
A1
B1
Y2
A2
B2
GND

TL/F/6656-1

Order Number DM54L02J or DM54L02W
See NS Package Number J14A or W14B

Function Table

$Y = \overline{A + B}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range DM54L	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54L02			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−0.2	mA
I_{OL}	Low Level Output Current			2	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.15	0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−3		−15	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		1.4	2.6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	R_L = 4 kΩ C_L = 50 pF		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

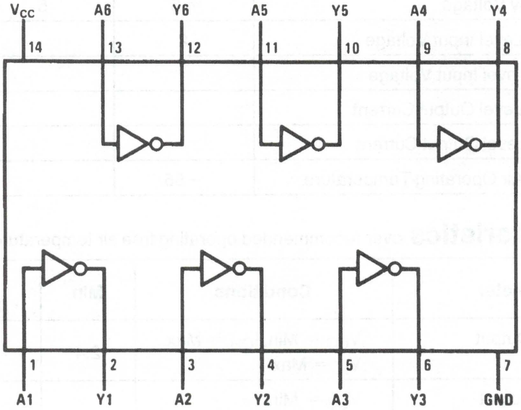
DM54L04 Hex Inverting Gate

General Description

This device contains six independent gates each of which performs the logic INVERT function.

Connection Diagram

Dual-In-Line Package



V_{CC}
A6
Y6
A5
Y5
A4
Y4
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
Y1
A2
Y2
A3
Y3
GND

TL/F/6616-1

Order Number DM54L04J or DM54L04W
See NS Package Number J14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54L04			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−0.2	mA
I_{OL}	Low Level Output Current			2	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min		0.15	0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−3		−15	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		0.6	1.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		1.7	3.06	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	R_L = 4 kΩ, C_L = 50 pF		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

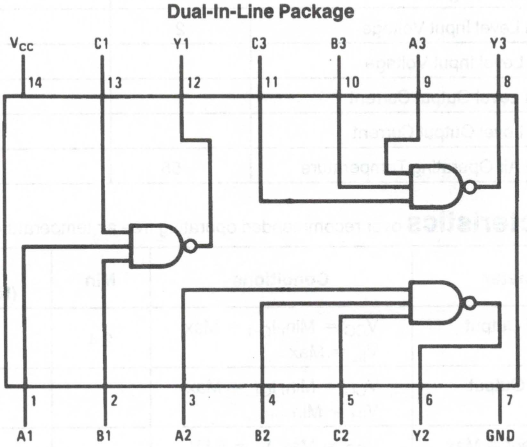
National Semiconductor

DM54L10
Triple 3-Input NAND Gates

General Description

This device contains three independent gates each of which performs the logic NAND function.

Connection Diagram


Dual-In-Line Package
V_{CC}
C1
Y1
C3
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
A2
B2
C2
Y2
GND

TL/F/6619–1

Order Number DM54L10J or DM54L10W
See NS Package Number J14A or W14B

Function Table

$$Y = \overline{ABC}$$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54L10			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−0.2	mA
I_{OL}	Low Level Output Current			2	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.15	0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−3		−15	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		0.33	0.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		0.87	1.53	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	R_L = 4 kΩ, C_L = 50 pF		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor

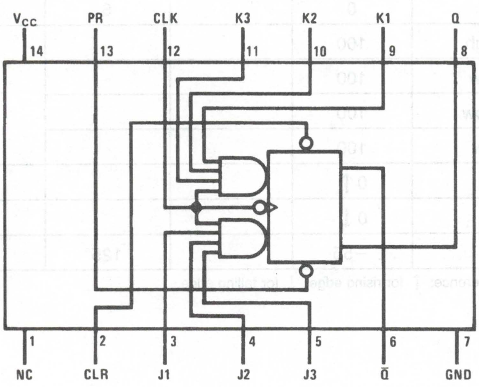
DM54L72 AND-Gated Master-Slave J-K Flip-Flop with Preset, Clear and Complementary Outputs

General Description

This device contains a positive pulse triggered master-slave J-K flip-flop with complementary outputs. Multiple J and K inputs are ANDed together to produce the internal J and K function for the flip-flop. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the AND gates is transferred to the master. While the clock is high the AND gate inputs are disabled. On the negative transition of the clock the data from the master is transferred to the slave. The logic state of the J and K inputs must not be allowed to change while the clock is in the high state. Data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs sets or resets the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6629-1

Order Number DM54L72J or DM54L72W
See NS Package Number J14A or W14B

Function Table

Inputs					Outputs	
PR	**CLR**	**CLK**	**J (Note 1)**	**K (Note 1)**	**Q**	**$\overline{Q}$**
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

Note 1: J = (J1)(J2)(J3), K = (K1)(K2)(K3)

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

⎍ = Positive pulse. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_0 = The output logic level before the indicated input conditions were established.

* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

Toggle = Each output changes to the complement of its previous level on each complete high level clock pulse.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range DM54L	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guarateed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54L72			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage	Clock			0.6	V
		Others			0.7	
I_{OH}	High Level Output Current				−0.2	mA
I_{OL}	Low Level Output Current				2	mA
f_{CLK}	Clock Frequency (Note 2)		0		6	MHz
t_W	Pulse Width (Note 2)	Clock High	100			ns
		Clock Low	100			
		Preset Low	100			
		Clear Low	100			
t_{SU}	Input Setup Time (Notes 1 & 2)		0↑			ns
t_H	Input Hold Time (Notes 1 & 2)		0↓			ns
T_A	Free Air Operating Temperature		−55		125	°C

Note 1: The symbols (↑, ↓) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

Note 2: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.15	0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 5.5V	J, K			100	µA
			Clear			200	
			Preset			200	
			Clock			200	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			10	µA
			Clear			20	
			Preset			20	
			Clock			−200	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	J, K			−0.18	mA
			Clear			−0.36	
			Preset			−0.36	
			Clock			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max		−3		−15	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			0.76	1.44	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		6		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		75	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		150	ns
t_{PLH}	Propagation Delay Level Output Low to High Level Output	Clear to $\overline{Q}$		75	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		150	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	75	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$	10	150	ns

National Semiconductor

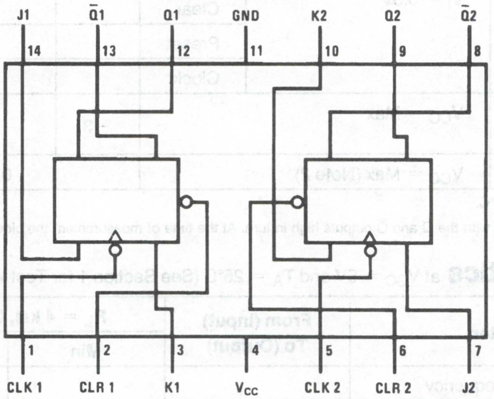
DM54L73 Dual Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high, the data from the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic states of the J and K inputs must not be allowed to change while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the clear input will reset the outputs regardless of the logic states of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6630–1

Order Number DM54L73J or DM54L73W
See NS Package Number J14A or W14B

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_O	$\overline{Q}_O$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	Toggle	

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_O = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete high level clock pulse.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54L73			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage	Clock			0.6	V
		Others			0.7	
I_{OH}	High Level Output Current				−0.2	mA
I_{OL}	Low Level Output Current				2	mA
f_{CLK}	Clock Frequency (Note 2)		0		6	MHz
t_W	Pulse Width (Note 2)	Clock High	100			ns
		Clock Low	100			
		Clear Low	100			
t_{SU}	Input Setup Time (Notes 1 & 2)		0↑			ns
t_H	Input Hold Time (Notes 1 & 2)		0↓			ns
T_A	Free Air Operating Temperature		−55		125	°C

Note 1: The symbols (↑, ↓) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

Note 2: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Voltage Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.15	0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 5.5V	J, K			100	μA
			Clear			200	
			Clock			200	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			10	μA
			Clear			20	
			Clock			−200	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	J, K			−0.18	mA
			Clear			−0.36	
			Clock			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max		−3		−15	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			1.5	2.88	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock is grounded.

Switching Characteristics V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		6		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		150	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		75	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	75	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$	10	150	ns

National Semiconductor

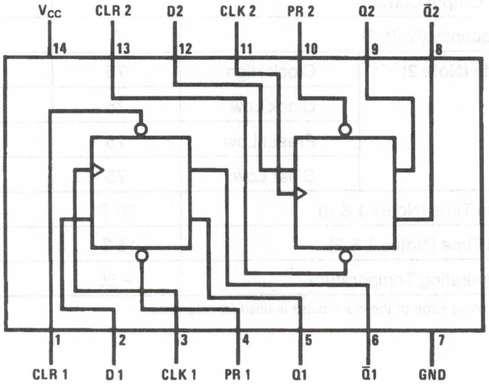
DM54L74 Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6631-1

Order Number DM54L74J or DM54L74W
See NS Package Number J14A or W14B

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_O	$\overline{Q}_O$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↑ = Positive-going transition.

Q_O = The output logic level of Q before the indicated input conditions were established.

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs returned to their inactive (high) level.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54L74			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.7	V
I_{OH}	High Level Output Current				−0.2	mA
I_{OL}	Low Level Output Current				2	mA
f_{CLK}	Clock Frequency (Note 2)		0		6	MHz
t_W	Pulse Width (Note 2)	Clock High	75			ns
		Clock Low	75			
		Preset Low	75			
		Clear Low	75			
t_{SU}	Input Setup Time (Notes 1 & 2)		50↑			ns
t_H	Input Hold Time (Notes 1 & 2)		15↑			ns
T_A	Free Air Operating Temperature		−55		125	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.15	0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 5.5V	D			100	μA
			Clear			300	
			Preset			200	
			Clock			200	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	D			10	μA
			Clear			30	
			Preset			20	
			Clock			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	D			−0.18	mA
			Clear			−0.36	
			Preset			−0.18	
			Clock			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max		−3		−15	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			1.6	3	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		6		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		120	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		120	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	90	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$	10	120	ns

National Semiconductor

DM54L93
Decade, Divide-by-12, and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

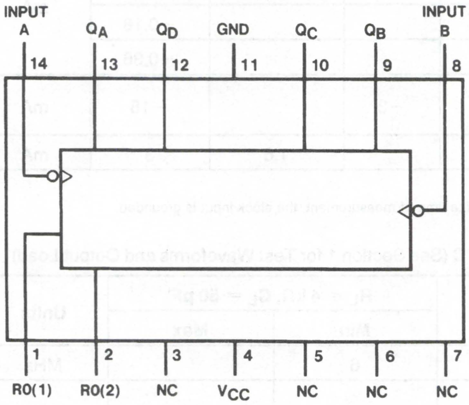
To use their maximum count length (decade, divide-by-twelve, or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table.

Features

- Typical power dissipation 16 mW
- Count frequency 15 MHz

Connection Diagram

Dual-In-Line Package



TL/F/6637-1

Order Number DM54L93J or DM54L93W
See NS Package Number J14A or W14B

Function Tables

COUNT SEQUENCE (See Note A)

Count	Output Q_D	Output Q_C	Output Q_B	Output Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

RESET/COUNT TRUTH TABLE (Note B)

Reset Inputs R0(1)	Reset Inputs R0(2)	Output Q_D	Output Q_C	Output Q_B	Output Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Note A: Output Q_A is connected to input B

Note B: H = High Level, L = Low Level, X = Don't Care.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54L93 Min	DM54L93 Nom	DM54L93 Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.7	V
I_{OH}	High Level Output Current				−0.2	mA
I_{OL}	Low Level Output Current				2	mA
f_{CLK}	Clock Frequency (Note 5)		0		6	MHz
t_W	Pulse Width (Note 5)	A	90			ns
		B	90			
		Reset	200			
t_{REL}	Reset Release time (Note 5)		200			ns
T_A	Free Air Operating Temperature		−55		125	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min (Note 4)			0.15	0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 5.5V	Reset			0.1	mA
			A			0.2	
			B			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Reset			10	μA
			A			20	
			B			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	Reset			−0.18	mA
			A			−0.36	
			B			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−3		−15	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				5.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, R0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.

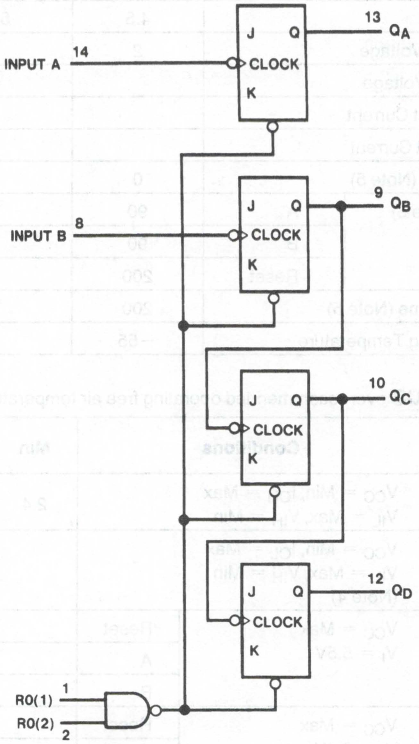
Note 4: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	6		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		400	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		400	ns

Logic Diagram


13
Q_A
14
INPUT A
J
Q
CLOCK
K
9
Q_B
8
INPUT B
J
Q
CLOCK
K
10
Q_C
Q
CLOCK
K
12
Q_D
J
Q
CLOCK
K
R0(1)
1
R0(2)
2

TL/F/6637-2

The J and K inputs shown without connection are for reference only and are functionally at a high level.

National Semiconductor

DM54L95 4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel and serial inputs, parallel output, mode control, and two clock inputs. The registers have three modes of operation.

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source.

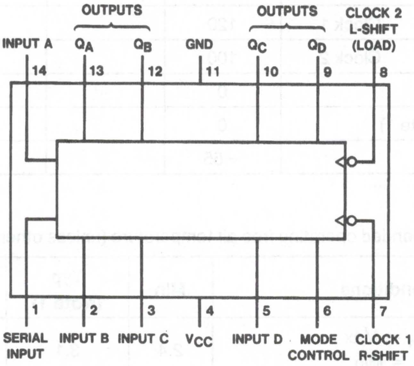
Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

Features

- Typical maximum clock frequency 14 MHz
- Typical power dissipation mW

Connection Diagram

Dual-In-Line Package



TL/F/6638-1

Order Number DM54L95J or DM54L95W
See NS Package Number J14A or W14B

Function Table

Inputs								Outputs			
Mode Control	Clocks		Serial	Parallel				Q_A	Q_B	Q_C	Q_D
	2 (L)	1 (R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{AO}	Q_{Bn}	Q_{CO}	Q_{DO}
↓	L	L	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↓	L	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↑	H	L	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↑	H	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}

†Shifting left requires external connection of Q_B to A, Q_C to B, Q_D to C. Serial data is entered at input D.
H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care (Any input, including transitions).
↓ = Transition from high to low level. ↑ = Transition from low to high level.
a, b, c, d, = The level of steady state input at inputs A, B, C, or D, respectively.
Q_{AO}, Q_{BO}, Q_{CO}, Q_{DO} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54L95 Min	DM54L95 Nom	DM54L95 Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.7	V
I_{OH}	High Level Output Current				−0.2	mA
I_{OL}	Low Level Output Current				2	mA
f_{CLK}	Clock Frequency (Note 1)		0		6	MHz
$t_{W(CLK)}$	Pulse Width of Clock (Note 1)		90			ns
t_{SU}	Data Setup Time (Note 1)		50			ns
t_{EN}	Time to Enable Clock (Note 1)	Clock 1	120			ns
		Clock 2	100			ns
t_H	Data Hold Time (Note 1)		0			ns
t_{IN}	Time to Inhibit Clock 1 or Clock 2 (Note 1)		0			ns
T_A	Free Air Operating Temperature		−55		125	°C

Note 1: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.13	0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 5.5V	Mode			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Mode			20	μA
			Others			10	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	Mode			−0.36	mA
			Others			−0.18	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−3		−15	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4.8	8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A 25°C

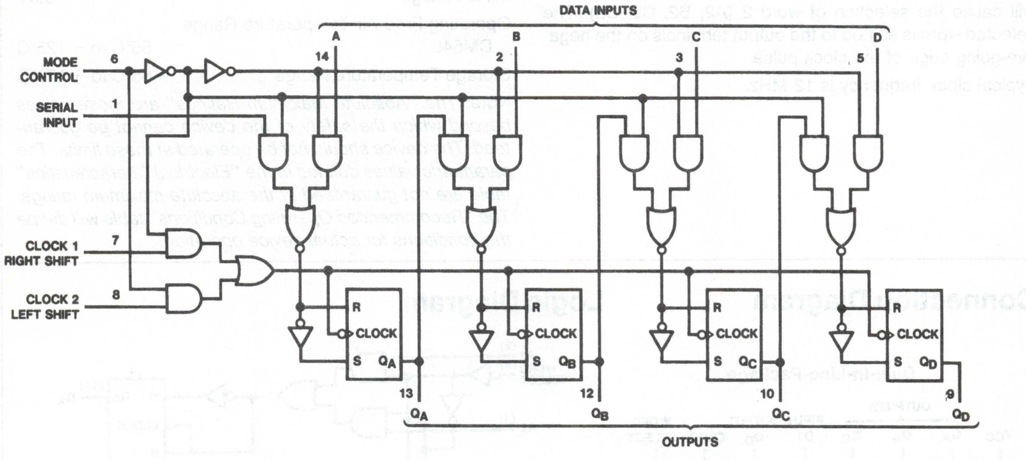
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5V; and a momentary 3V, then ground, applied to both clock inputs.

Switching Characteristics at V_{CC} = 5V and T_A 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 4\Omega$, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		6		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		90	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		90	ns

Logic Diagram



DATA INPUTS
A
B
C
D
14
2
3
5
MODE CONTROL
6
SERIAL INPUT
1
CLOCK 1 RIGHT SHIFT
7
CLOCK 2 LEFT SHIFT
8
R
CLOCK
S
Q_A
Q_B
Q_C
Q_D
13
12
10
9
OUTPUTS

TL/F/6638-2

National Semiconductor

DM54L98 4-Bit Storage Register

General Description

This data selector/storage register is composed of four S-R master-slave flip-flops, four AND-OR INVERT gates, one buffer, and six inverter/drivers.

When the word select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high level input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is shifted to the output terminals on the negative-going edge of the clock pulse.

Typical clock frequency is 12 MHz.

Absolute Maximum Ratings (Note)

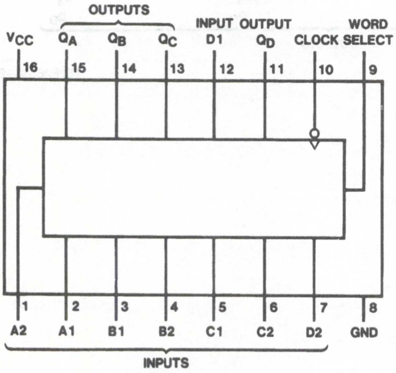
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Connection Diagram

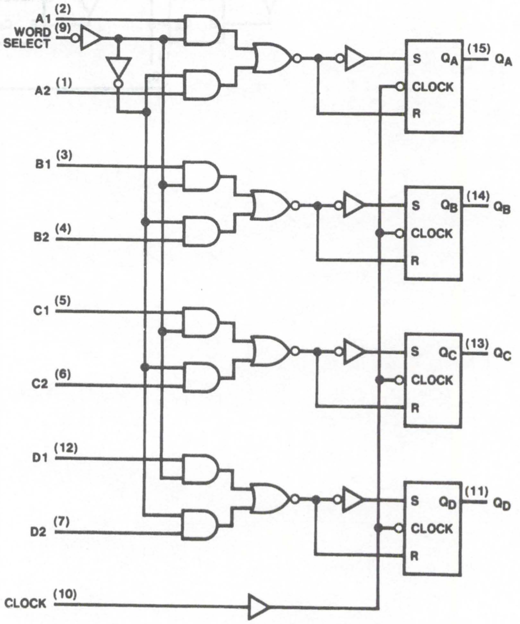
Dual-In-Line-Package


OUTPUTS
INPUT OUTPUT
WORD
VCC
QA
QB
QC
D1
QD
CLOCK
SELECT
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
A2
A1
B1
B2
C1
C2
D2
GND
INPUTS

TL/F/6639-1

Order Number DM54L98J or DM54L98W
See NS Package Number J16A or W16A

Logic Diagram


A1 (2)
WORD SELECT (9)
A2 (1)
B1 (3)
B2 (4)
C1 (5)
C2 (6)
D1 (12)
D2 (7)
CLOCK (10)
S
QA
CLOCK
R
(15) QA
S
QB
CLOCK
R
(14) QB
S
QC
CLOCK
R
(13) QC
S
QD
CLOCK
R
(11) QD

TL/F/6639-2

Recommended Operating Conditions

Symbol	Parameter		DM54L98 Min	DM54L98 Nom	DM54L98 Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.7	V
I_{OH}	High Level Output Current				−0.2	mA
I_{OL}	Low Level Output Current				2	mA
f_{CLK}	Clock Frequency (Note 4)		0		6	MHz
t_W	Clock Pulse Width (Note 4)		100	65		ns
t_{SU}	Setup Time (Note 4)	Data High	100			ns
		Data Low	120			
		Select High	150			
		Select Low	100			
T_A	Free Air Operating Temperature		−55		125	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	2.4			V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max},$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$		0.15	0.3	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5V$			0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4V$			10	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.3V$			−0.18	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 3)	−3		−15	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 2)		6	8	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: I_{CC} is measured with all outputs open and all inputs grounded.

Note 3: Not more than one output should be shorted at a time.

Note 4: $T_A = 25°C$ and $V_{CC} = 5V$.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 4\,k\Omega, C_L = 50\,pF$ Min	$R_L = 4\,k\Omega, C_L = 50\,pF$ Max	Units
f_{MAX}	Maximum Clock Frequency		6		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		80	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		100	ns

National Semiconductor

93L00
4-Bit Universal Shift Register

General Description

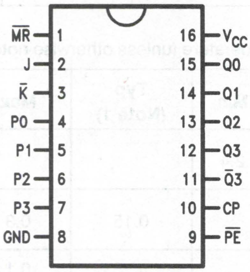
The 93L00 is a 4-bit universal shift register. As a high speed multifunctional sequential logic block, it is useful in a wide variety of register and counter applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers.

Features

- Asynchronous master reset
- J, $\overline{\text{K}}$ inputs to first stage

Connection Diagram

Dual-In-Line Package

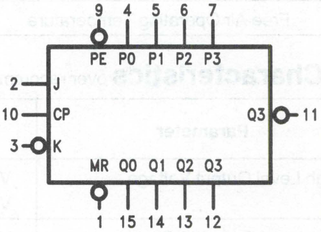


$\overline{\text{MR}}$ 1
J 2
$\overline{\text{K}}$ 3
P0 4
P1 5
P2 6
P3 7
GND 8
16 V_{CC}
15 Q0
14 Q1
13 Q2
12 Q3
11 $\overline{\text{Q3}}$
10 CP
9 $\overline{\text{PE}}$

TL/F/9576-1

Order Number 93L00DMQB or 93L00FMQB
See NS Package Number J16A or W16A

Logic Symbol



9 4 5 6 7
PE P0 P1 P2 P3
2 J
10 CP
3 K
Q3 11
MR Q0 Q1 Q2 Q3
1 15 14 13 12

TL/F/9576-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{\text{PE}}$	Parallel Enable Input (Active LOW)
P0–P3	Parallel Inputs
J	First Stage J Input (Active HIGH)
$\overline{\text{K}}$	First Stage K Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
$\overline{\text{MR}}$	Master Reset Input
Q0–Q3	Parallel Outputs
$\overline{\text{Q3}}$	Complementary Last Stage Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−65°C to +125°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L00 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Voltage			−0.4	mA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW, J, $\overline{K}$ and P0–P3 to CP	60 60			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW, J, $\overline{K}$ and P0–P3 to CP	0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW, $\overline{PE}$ to CP	68 68			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW, $\overline{PE}$ to CP	0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	38 38			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	53			ns
t_{rec}	Recovery Time, $\overline{MR}$ to CP	70			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			20	μA
			CP			40	
			$\overline{PE}$			46	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Inputs			−400	μA
			CP			−800	
			$\overline{PE}$			−920	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max				23	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	93L C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Shift Frequency	10		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		35 51	ns
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n		60	ns

Functional Description

The Logic Diagrams and Truth Table indicate the functional characteristics of the 93L00 4-bit shift register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers.

The 93L00 has two primary modes of operation, shift right (Q0 ⟶ Q1) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ input is HIGH, serial data enters the first flip-flop Q0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction Q0 ⟶ Q1 ⟶ Q2 ⟶ Q3 following each LOW-to-HIGH clock transition. The J$\overline{K}$ inputs provide the flexibility of the JK type input for special applications, and the simple D-type input for general applications by tying the two pins together.

When the $\overline{PE}$ input is LOW, the 93L00 appears as four common clocked D flip-flops. The data on the parallel inputs P0–P3 is transferred to the respective Q0–Q3 outputs following the LOW-to-HIGH clock transition. Shift left operation (Q3 ⟶ Q2) can be achieved by tying the Qn outputs to the Pn − 1 inputs and holding the $\overline{PE}$ input LOW.

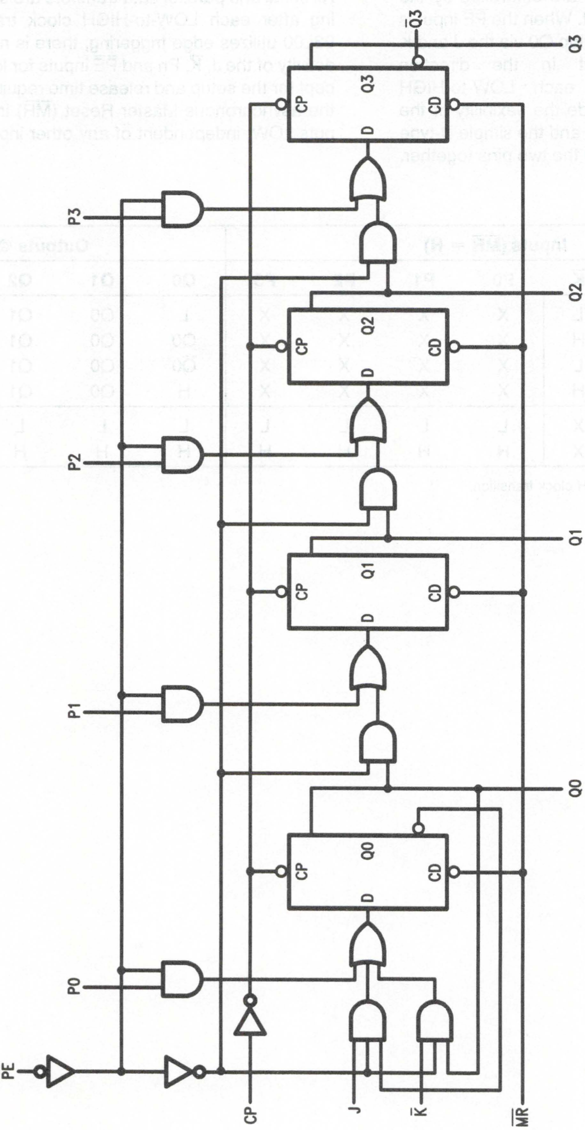
All serial and parallel data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. Since the 93L00 utilizes edge triggering, there is no restriction on the activity of the J, $\overline{K}$, Pn and $\overline{PE}$ inputs for logic operation—except for the setup and release time requirements. A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

Truth Table

Operating Mode	Inputs ($\overline{MR}$ = H)							Outputs @ t_{n+1}				
	$\overline{PE}$	J	$\overline{K}$	P0	P1	P2	P3	Q0	Q1	Q2	Q3	$\overline{Q3}$
Shift Mode	H	L	L	X	X	X	X	L	Q0	Q1	Q2	$\overline{Q2}$
	H	L	H	X	X	X	X	Q0	Q0	Q1	Q2	$\overline{Q2}$
	H	H	L	X	X	X	X	$\overline{Q0}$	Q0	Q1	Q2	$\overline{Q2}$
	H	H	H	X	X	X	X	H	Q0	Q1	Q2	$\overline{Q2}$
Parallel Entry Mode	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

*t_{n+1} = Indicates state after next LOW-to-HIGH clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram


PE
CP
J
K
MR
P0
P1
P2
P3
D
CP
CD
Q0
Q1
Q2
Q3
Q0
Q1
Q2
Q3
Q3

TL/F/9576-3

National Semiconductor

93L01
1-of-10 Decoder

General Description

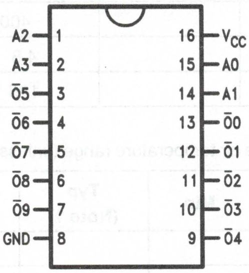
The 93L01 multipurpose decoders are designed to accept four inputs and provide ten mutually exclusive outputs.

Features

- Multifunction capability
- Mutually exclusive outputs
- Demultiplexing capability
- Typical power dissipation of 45 mW

Connection Diagram

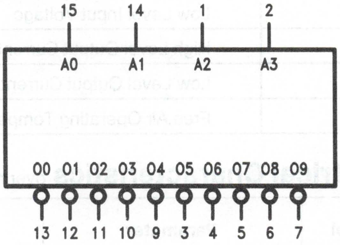
Dual-In-Line Package


A2 1
A3 2
$\overline{O5}$ 3
$\overline{O6}$ 4
$\overline{O7}$ 5
$\overline{O8}$ 6
$\overline{O9}$ 7
GND 8
16 V_{CC}
15 A0
14 A1
13 $\overline{O0}$
12 $\overline{O1}$
11 $\overline{O2}$
10 $\overline{O3}$
9 $\overline{O4}$

TL/F/9583-1

Order Number 93L01DMQB or 93L01FMQB
See Package Number J16A or W16A

Logic Symbol


15
14
1
2
A0
A1
A2
A3
00
01
02
03
04
05
06
07
08
09
13
12
11
10
9
3
4
5
6
7

TL/F/9583-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A3	Address Inputs
$\overline{O0}$–$\overline{O9}$	Decoder Outputs (Active LOW)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L01 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−400	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 3 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay An to $\overline{\text{On}}$		36 36	ns

Functional Description

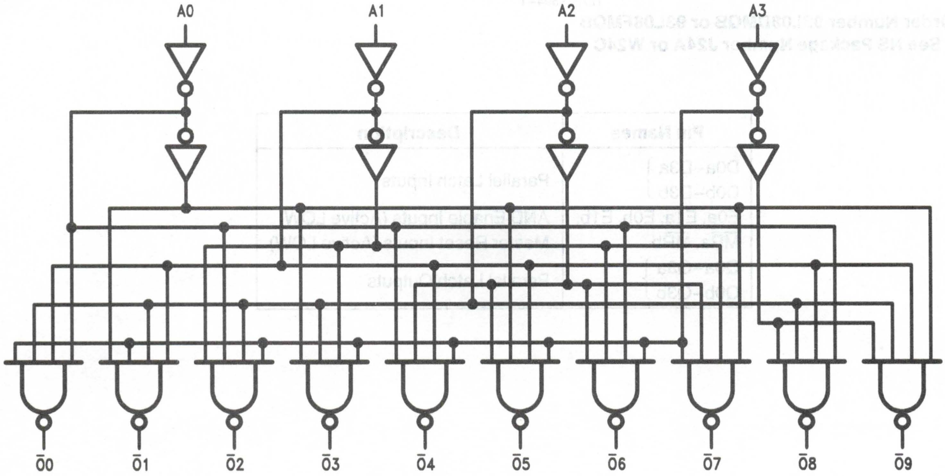
The 93L01 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables. The logic design of the 93L01 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs. The most significant input A3 produces a useful inhibit function when the 93L01 is used as a 1-of-8 decoder.

Truth Table

Inputs				Outputs									
A0	A1	A2	A3	$\overline{O0}$	$\overline{O1}$	$\overline{O2}$	$\overline{O3}$	$\overline{O4}$	$\overline{O5}$	$\overline{O6}$	$\overline{O7}$	$\overline{O8}$	$\overline{O9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram


A0
A1
A2
A3
$\overline{O0}$
$\overline{O1}$
$\overline{O2}$
$\overline{O3}$
$\overline{O4}$
$\overline{O5}$
$\overline{O6}$
$\overline{O7}$
$\overline{O8}$
$\overline{O9}$

TL/F/9583–3

National Semiconductor

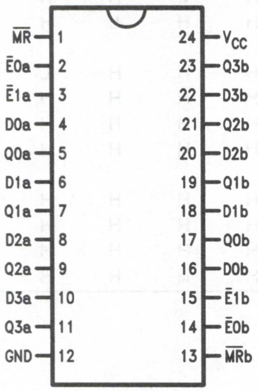
93L08
Dual 4-Bit Latch

General Description

The 93L08 is a dual 4-bit D-type latch designed for general purpose storage applications in digital systems. Each latch contains both an active LOW Master Reset input and active LOW Enable inputs.

Connection Diagram

Dual-In-Line Package

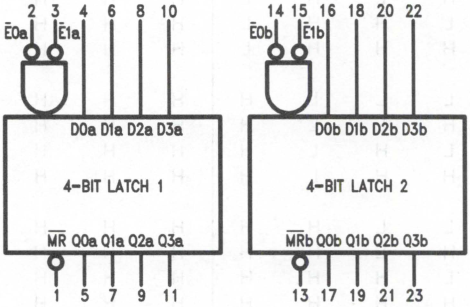


$\overline{\text{MR}}$ 1
Ē0a 2
Ē1a 3
D0a 4
Q0a 5
D1a 6
Q1a 7
D2a 8
Q2a 9
D3a 10
Q3a 11
GND 12
24 V_{CC}
23 Q3b
22 D3b
21 Q2b
20 D2b
19 Q1b
18 D1b
17 Q0b
16 D0b
15 Ē1b
14 Ē0b
13 $\overline{\text{MR}}$b

TL/F/9594-1

Order Number 93L08DMQB or 93L08FMQB
See NS Package Number J24A or W24C

Logic Symbol



2 3 4 6 8 10
Ē0a Ē1a
D0a D1a D2a D3a
4-BIT LATCH 1
$\overline{\text{MR}}$ Q0a Q1a Q2a Q3a
1 5 7 9 11
14 15 16 18 20 22
Ē0b Ē1b
D0b D1b D2b D3b
4-BIT LATCH 2
$\overline{\text{MR}}$b Q0b Q1b Q2b Q3b
13 17 19 21 23

TL/F/9594-2

V_{CC} = Pin 24
GND = Pin 12

Pin Names	Description
D0a–D3a D0b–D3b	Parallel Latch Inputs
Ē0a, Ē1a, Ē0b, Ē1b,	AND Enable Inputs (Active LOW)
$\overline{\text{MR}}$a, $\overline{\text{MR}}$b	Master Reset Inputs (Active LOW)
Q0a–Q3a Q0b–Q3b	Parallel Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H)	Setup Time HIGH, D_n to $\overline{E}_n$	8			ns
t_h (H)	Hold Time HIGH, D_n to $\overline{E}_n$	1			ns
t_s (L)	Setup Time LOW, D_n to $\overline{E}_n$	18			ns
t_h (L)	Hold Time LOW, D_n to $\overline{E}_n$	4			ns
t_w (L)	$\overline{E}_n$ Pulse Width LOW	32			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	30			ns
t_{rec}	Recovery Time, $\overline{MR}$ to $\overline{E}_n$	10			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			20	μA
			D_n			30	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Inputs			−400	μA
			D_n			−640	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				29	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 3 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15\ pF$		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay En to Qn		45 38	ns
t_{PLH} t_{PHL}	Propagation Delay Dn to Qn		27 29	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Qn		30	ns

Functional Description

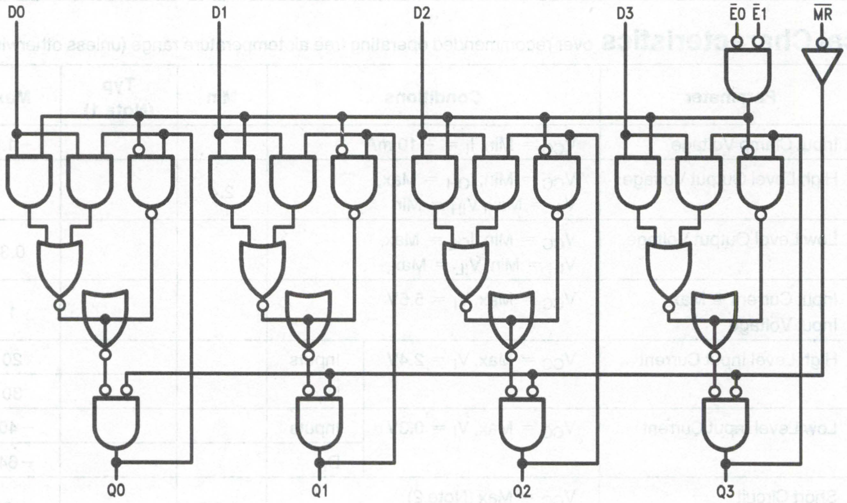
Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input. The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the Master Reset input.

Truth Table

$\overline{MR}$	$\overline{E0}$	$\overline{E1}$	D	Qn	Operation
H	L	L	L	L	Data Entry
H	L	L	H	L	Data Entry
H	L	H	X	Qn−1	Hold
H	H	L	X	Qn−1	Hold
H	H	H	X	Qn−1	Hold
L	X	X	X	L	Reset

Q_{n-1} = Previous Output State
Q_n = Present Output State
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/9594-3

National Semiconductor

93L09
Dual 4-Input Multiplexer

General Description

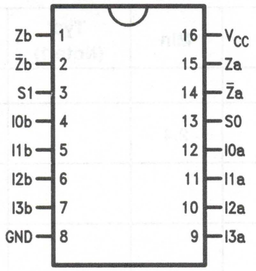
The 93L09 monolithic dual 4-input digital multiplexers consist of two multiplexing circuits with common input select logic. Each circuit contains four inputs and fully buffered complementary outputs. In addition to multiplexer operation, the 93L09 can generate any two functions of three variables. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding, the 93L09 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output bus.

Features

- Multifunction capability
- On-chip select logic decoding
- Fully buffered complementary outputs

Connection Diagram

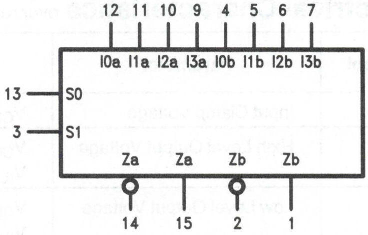
Dual-In-Line Package


Zb 1
$\overline{\text{Zb}}$ 2
S1 3
I0b 4
I1b 5
I2b 6
I3b 7
GND 8
16 V_{CC}
15 Za
14 $\overline{\text{Za}}$
13 S0
12 I0a
11 I1a
10 I2a
9 I3a

TL/F/9602-1

Order Number 93L09DMQB or 93L09FMQB
See NS Package Number J16A or W16A

Logic Symbol


12 11 10 9 4 5 6 7
I0a I1a I2a I3a I0b I1b I2b I3b
13 S0
3 S1
Za Za Zb Zb
14 15 2 1

TL/F/9602-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
S0, S1	Common Select Inputs
I0a–I3a	Multiplexer A Inputs
Za	Multiplexer A Output
$\overline{\text{Za}}$	Complementary Multiplexer A Output
I0b–I3b	Multiplexer B Inputs
Zb	Multiplexer B Output
$\overline{\text{Zb}}$	Complementary Multiplexer B Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L09 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, II = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.3	V
II	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
IIH	High Level Input Current	V_{CC} = Max, V_I = 2.4V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−400	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−10		−40	mA
I_{CC}	Supply Current	V_{CC} = Max			11.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay S_0 to Z_a		70 60	ns
t_{PLH} t_{PHL}	Propagation Delay S_0 to $\overline{Z}_a$		55 50	ns
t_{PLH} t_{PHL}	Propagation Delay I_0 to Z_a		70 65	ns
t_{PLH} t_{PHL}	Propagation Delay S_0 to Z_a		40 60	ns

Functional Description

The 93L09 dual 4-input multiplexers are able to select two bits of either HIGH or LOW data or control from up to four sources, in one package. The 93L09 is the logical implementation of two-pole, four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

$$Za = I0a \bullet \overline{S1} \bullet \overline{S0} + I1a \bullet \overline{S1} \bullet S0 + I2a \bullet S1 \bullet \overline{S0} + I3a \bullet S1 \bullet S0$$

$$Zb = I0b \bullet \overline{S1} \bullet \overline{S0} + I1b \bullet \overline{S1} \bullet S0 + I2a \bullet S1 \bullet \overline{S0} + I3b \bullet S1 \bullet S0$$

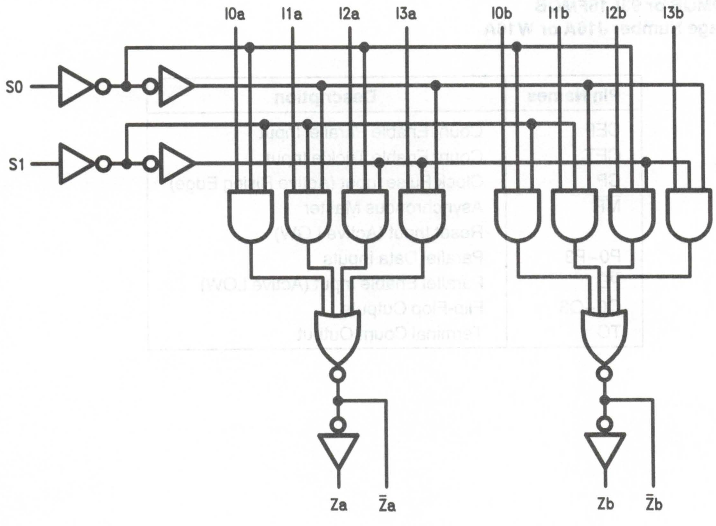
The 93L09 is frequently used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the select inputs. A less obvious application is as a function generator. The 93L09 can generate two functions of three variables. This is useful for implementing random gating functions.

Truth Table

Select Inputs		Inputs (a or b)				Outputs (a or b)	
S0	S1	I0	I1	I2	I3	Z	$\overline{Z}$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Immaterial

Logic Diagram



TL/F/9602-3

National Semiconductor

93L10/93L16
BCD Decade Counter/4-Bit Binary Counter

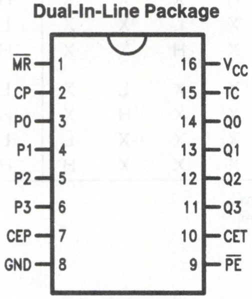
General Description

The 93L10 is a high speed synchronous BCD decade counter and the 93L16 is a high speed synchronous 4-bit binary counter. They are synchronously presettable, multifunctional MSI building blocks useful in a large number of counting, digital integration and conversion applications. Several states of synchronous operation are obtainable with no external gating packages required through an internal carry lookahead counting technique.

Features

- Synchronous counting and parallel entry
- Decoded terminal count
- Built-in Carry Circuitry
- Easy interfacing with DTL, LPDTL, and TTL families

Connection Diagram

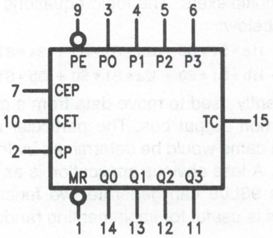


Dual-In-Line Package
MR 1
CP 2
P0 3
P1 4
P2 5
P3 6
CEP 7
GND 8
16 VCC
15 TC
14 Q0
13 Q1
12 Q2
11 Q3
10 CET
9 PE

TL/F/9603-1

Order Number 93L10DMQB, 93L10FMQB, 93L16DMQB or 93L16FMQB
See NS Package Number J16A or W16A

Logic Symbol



9
3
4
5
6
PE
P0
P1
P2
P3
7
CEP
10
CET
TC
15
2
CP
MR
Q0
Q1
Q2
Q3
1
14
13
12
11

TL/F/9603-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{\text{MR}}$	Asynchronous Master Reset Input (Active LOW)
P0–P3	Parallel Data Inputs
$\overline{\text{PE}}$	Parallel Enable Input (Active LOW)
Q0–Q3	Flip-Flop Outputs
TC	Terminal Count Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L10/93L16 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Voltage			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW P_n to CP	75 75			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW P_n to CP	10 10			ns
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW $\overline{PE}$ to CP	(Note 2) 53			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW $\overline{PE}$ to CP	7.0 (Note 2)			ns
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW CEP or CET to CP	26 (Note 1)			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW CEP or CET to CP	(Note 1) 10			ns
$t_w(H)$ $t_w(L)$	CP Pulse Width	25 25			ns
$t_w(L)$	$\overline{MR}$ Pulse Width LOW	65			ns
t_{rec}	Recovery Time, $\overline{MR}$ to CP	30			ns

Note 1: The Setup Time "$t_s(L)$" and Hold Time "$t_h(H)$" between the Count Enable (CEP and CET) and the Clock (CP) indicate that the HIGH-to-LOW transition of the CEP and CET must occur only while the Clock is HIGH for conventional operation.

Note 2: The Setup Time "$t_s(H)$" and Hold Time "$t_h(L)$" between the Parallel Enable ($\overline{PE}$) and Clock (CP) indicate that the LOW-to-HIGH transition of the $\overline{PE}$ must occur only while the Clock is HIGH for conventional operation.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			20	μA
			CET, CP, PE			40	
			P_n			13.3	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Inputs			−400	μA
			CET, CP, PE			−800	
			P_n			−267	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max				27.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Count Frequency	13		MHz
t_{PLH}	Propagation Delay		32	ns
t_{PHL}	CP to Q		39	
t_{PLH}	Propagation Delay		66	ns
t_{PHL}	CP to TC		30	
t_{PLH}	Propagation Delay		35	ns
t_{PHL}	CET to TC		30	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q		72	ns

Functional Description

The 93L10 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it increments to state 0 (LLLL). The 93L16 counts modulo-16 in binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, parallel load, count-up and hold. Four control inputs—Master Reset ($\overline{MR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 93L10 and 93L16 contain masterslave flip-flops which are "next-state catching" because of the JK feedback. This means that when CP is LOW, information that would change the state of a flip-flop, whether from the counting logic or the parallel entry logic if either mode is momentarily enabled, enters the master and is locked in. Thus to avoid inadvertently changing the state of a master latch, and the subsequent transfer of the erroneous information to the slave when the clock rises, it is necessary to insure that neither the counting mode, nor the parallel entry mode is momentarily enabled while CP is LOW.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state (9 for the decade counters, 15 for the binary counters—fully decoded in both types). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. These two schemes are shown in *Figures a* and *b*. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the state diagrams.

MULTISTAGE COUNTING

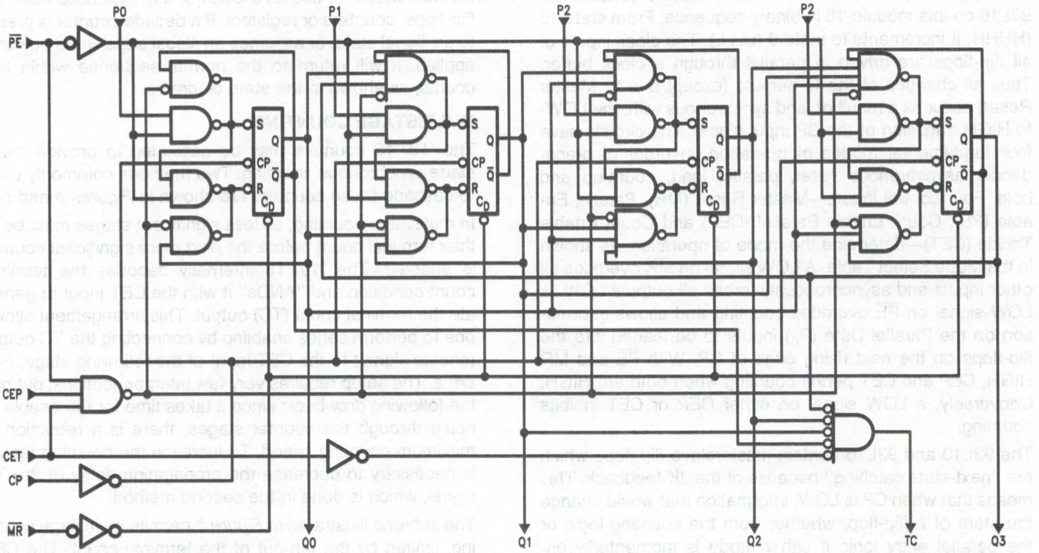
The '10/'16 counters may be cascaded to provide multistage synchronous counting. Two methods commonly used to cascade these counters are shown in *Figures a* and *b*.

In multistage counting, all less significant stages must be at their terminal count before the next more significant counter is enabled. The '10/'16 internally decodes the terminal count condition and "ANDs" it with the CET input to generate the terminal count (TC) output. This arrangement allows one to perform series enabling by connecting the TC output (enable signal) to the CET input of the following stage, *Figure a*. The setup requires very few interconnections, but has the following drawback: since it takes time for the enable to ripple through the counter stages, there is a reduction in maximum counting speed. To increase the counting rate, it is necessary to decrease the propagation delay of the TC signal, which is done in the second method.

The scheme illustrated in *Figure b* permits multistage counting, limited by the fan-out of the terminal count. The CEP input of the '10/'16 is internally "ANDed" with the CET input and as a result, both must be HIGH for the counter to be enabled. The CET inputs are connected as before except for the second stage. There the CET input is left floating and is therefore HIGH. Also, all CEP inputs are connected to the terminal output of the first stage. The advantage of this method is best seen by assuming all stages except the second and last are in their terminal condition. As the second stage advances to its terminal count, an enable is allowed to trickle down to the last counter stage, but has the full cycle time of the first counter to reach it. Then as the TC of the first stage goes active (HIGH), all CEP inputs are activated, allowing all stages to count on the next clock.

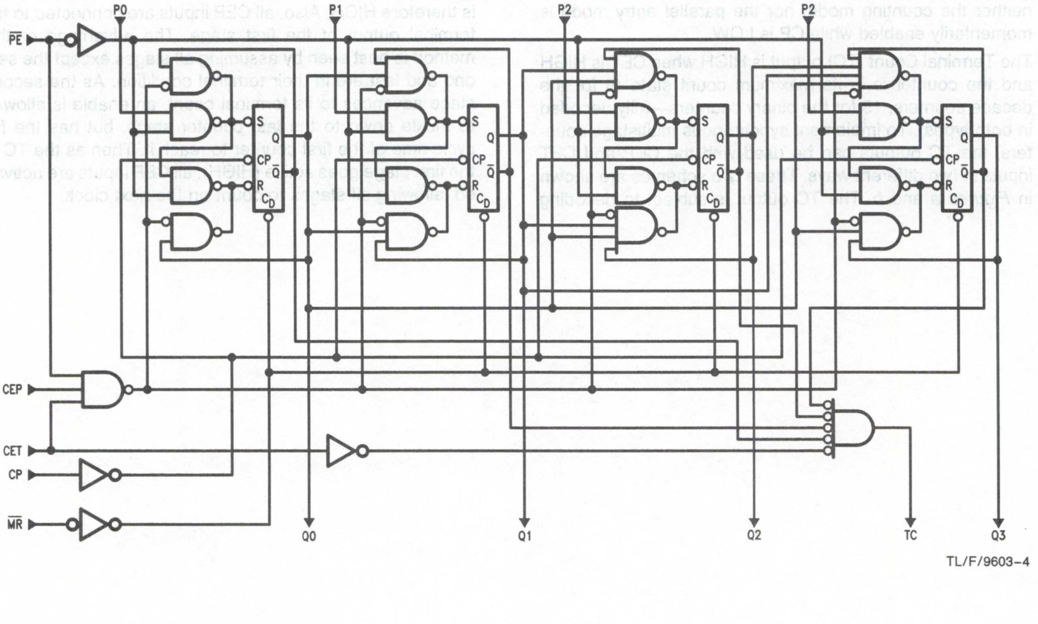
Logic Diagrams

93L10


P0
P1
P2
P2
PE
CEP
CET
CP
MR
S
Q
CP
Q̄
R
C_D
Q0
Q1
Q2
TC
Q3

TL/F/9603-3

93L16


P0
P1
P2
P2
PE
CEP
CET
CP
MR
S
Q
CP
Q̄
R
C_D
Q0
Q1
Q2
TC
Q3

TL/F/9603-4

Mode Select Table

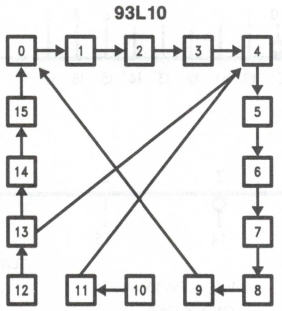
Inputs					Response
$\overline{MR}$	$\overline{PE}$	CEP	CET	CP	
L	X	X	X	X	Clear; All Outputs LOW
H	L	X	X	↑	Parallel Load; $P_n \rightarrow Q_n$
H	H	L	X	X	Hold
H	H	X	L	X	Hold; TC = LOW
H	H	H	H	↑	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

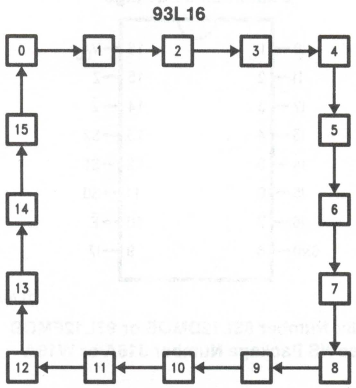
Logic Equations

Count Enable = MR • PE • CEP • CET
Terminal Count = CET • Q0 • Q1 • Q2 • Q3 ('16)
Terminal Count = CET • Q0 • $\overline{Q}$1 • $\overline{Q}$2 • Q3 ('10)

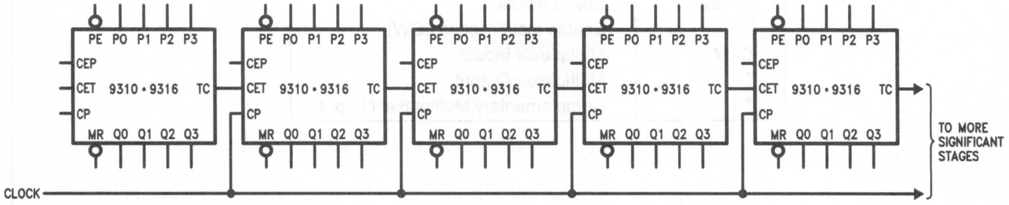
State Diagrams


93L10
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

TL/F/9603-5

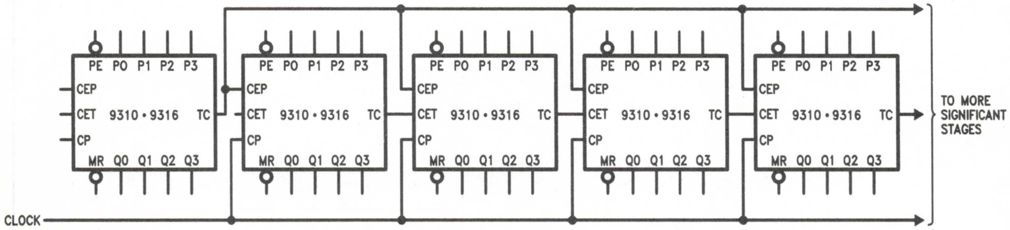

93L16
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

TL/F/9603-6


PE P0 P1 P2 P3
CEP
CET 9310 • 9316 TC
CP
MR Q0 Q1 Q2 Q3
CLOCK
TO MORE SIGNIFICANT STAGES

TL/F/9603-7

FIGURE a. Synchronous Multistage Counting Scheme (Slow)


PE P0 P1 P2 P3
CEP
CET 9310 • 9316 TC
CP
MR Q0 Q1 Q2 Q3
CLOCK
TO MORE SIGNIFICANT STAGES

TL/F/9603-8

FIGURE b. Synchronous Multistage Counting Scheme (Fast)

National Semiconductor

93L12
8-Input Multiplexer

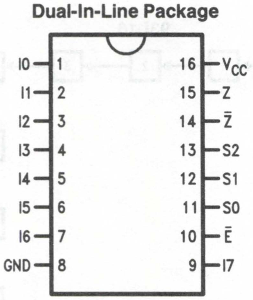
General Description

The 93L12 is a monolithic, high speed, 8-input digital multiplexer circuit. It provides, in one package, the ability to select one bit of data from up to eight sources. The 93L12 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

Features

- Multifunction capability
- On-chip select logic decoding
- Fully buffered complementary outputs

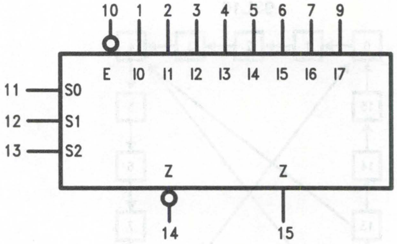
Connection Diagram


Dual-In-Line Package
I0 1
I1 2
I2 3
I3 4
I4 5
I5 6
I6 7
GND 8
16 VCC
15 Z
14 $\overline{Z}$
13 S2
12 S1
11 S0
10 $\overline{E}$
9 I7

TL/F/9610-1

Order Number 93L12DMQB or 93L12FMQB
See NS Package Number J16A or W16A

Logic Symbol


10
1
2
3
4
5
6
7
9
E
I0
I1
I2
I3
I4
I5
I6
I7
11
12
13
S0
S1
S2
Z
Z
14
15

TL/F/9610-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
S0–S2	Select Inputs
$\overline{E}$	Enable Input (Active LOW)
I0–I7	Multiplexer Inputs
Z	Multiplexer Output
$\overline{Z}$	Complementary Multiplexer Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L12 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−400	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			13.3	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15$ pF Min	$C_L = 15$ pF Max	Units
t_{PLH} t_{PHL}	Propagation Delay S0 to Z		60 75	ns
t_{PLH} t_{PHL}	Propagation Delay S0 to $\overline{Z}$		70 50	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z		60 75	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$		70 45	ns
t_{PLH} t_{PHL}	Propagation Delay In to Z		70 65	ns
t_{PLH} t_{PHL}	Propagation Delay In to $\overline{Z}$		55 55	ns

Functional Description

The 93L12 is a logical implementation of a single pole, eight position switch with the switch position controlled by the state of three Select inputs, S0, S1, S2. Both assertion and negation outputs are provided. The Enable input (E) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$
\begin{aligned}
Z = E \bullet (&I0 \bullet \overline{S0} \bullet \overline{S1} \bullet \overline{S2} + I1 \bullet S0 \bullet \overline{S1} \bullet \overline{S2} \\
&+ I2 \bullet \overline{S0} \bullet S1 \bullet \overline{S2} + I3 \bullet S0 \bullet S1 \bullet \overline{S2} \\
&+ I4 \bullet \overline{S0} \bullet \overline{S1} \bullet S2 + I5 \bullet S0 \bullet \overline{S1} \bullet S2 \\
&+ I6 \bullet \overline{S0} \bullet S1 \bullet S2 \\
&+ I7 \bullet S0 \bullet S1 \bullet S2).
\end{aligned}
$$

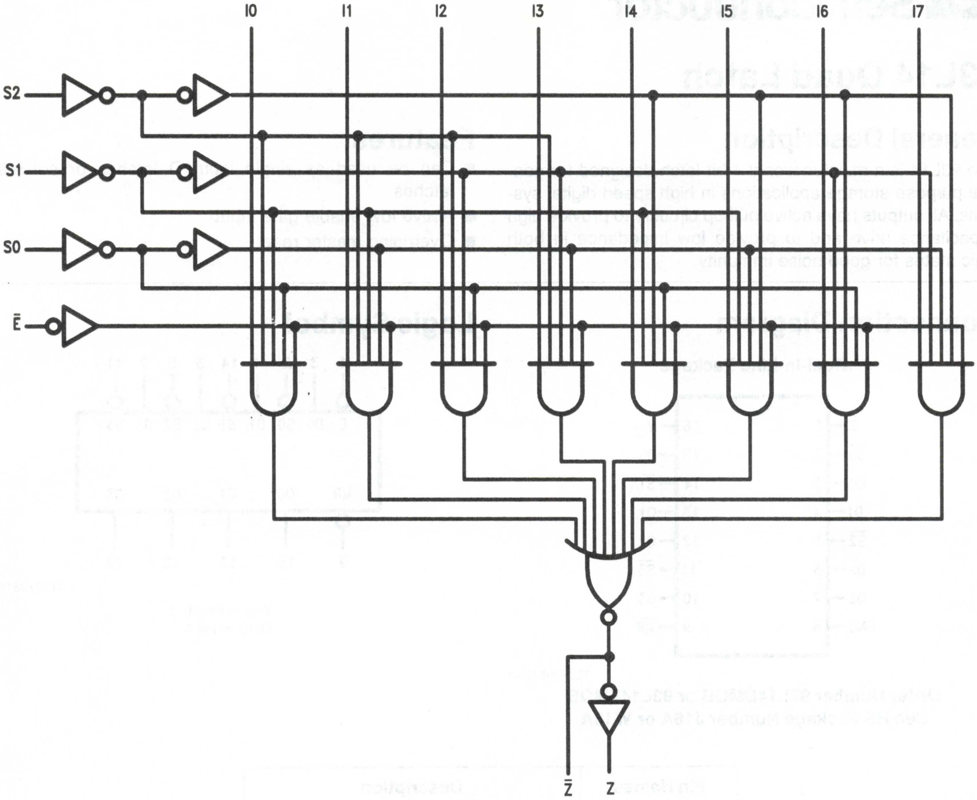
The 93L12 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 93L12 can provide any logic function of four variables and its negation. Thus any number of random logic elements used to generate unusual truth tables can be replaced by one 93L12.

Truth Table

Inputs												Outputs	
$\overline{E}$	S2	S1	S0	I0	I1	I2	I3	I4	I5	I6	I7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram


I0
I1
I2
I3
I4
I5
I6
I7
S2
S1
S0
Ē
Z̄
Z

TL/F/9610-3

National Semiconductor

93L14 Quad Latch

General Description

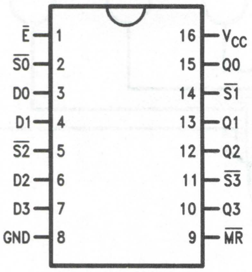
The 93L14 is a multifunctional 4-bit latch designed for general purpose storage applications in high speed digital systems. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good noise immunity.

Features

- Can be used as single input D latches or set/reset latches
- Active low enable gate input
- Overriding master reset

Connection Diagram

Dual-In-Line Package

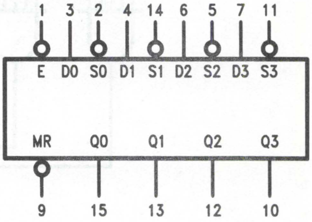


$\overline{E}$ 1
$\overline{S0}$ 2
D0 3
D1 4
$\overline{S2}$ 5
D2 6
D3 7
GND 8
16 V_{CC}
15 Q0
14 $\overline{S1}$
13 Q1
12 Q2
11 $\overline{S3}$
10 Q3
9 $\overline{MR}$

TL/F/9612-1

Order Number 93L14DMQB or 93L14FMQB
See NS Package Number J16A or W16A

Logic Symbol



1 3 2 4 14 6 5 7 11
E D0 S0 D1 S1 D2 S2 D3 S3
MR Q0 Q1 Q2 Q3
9 15 13 12 10

TL/F/9612-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{E}$	Enable Input (Active LOW)
D0–D3	Data Inputs
$\overline{S0}$–$\overline{S3}$	Set Inputs (Active LOW)
$\overline{MR}$	Master Reset Input (Active LOW)
Q0–Q3	Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L14 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Voltage			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to $\overline{E}$	10 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to $\overline{E}$	0 10			ns
t_s (H)	Setup Time HIGH, D_n to $\overline{S}_n$	15			ns
t_h (L)	Hold Time LOW, D_n to $\overline{S}_n$	5			ns
t_w (L)	$\overline{E}$ Pulse Width LOW	30			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	25			ns
t_{rec}	Recovery Time, $\overline{MR}$ to $\overline{E}$	5			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			20	μA
			D_n			30	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Inputs			−400	μA
			D_n			−600	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				16.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		45 36	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		30 30	ns
t_{PLH}	Propagation Delay, $\overline{MR}$ to Q_n		30	ns
t_{PHL}	Propagation Delay, $\overline{S}_n$ to Q_n		33	ns

Functional Description

The 93L14 consists of four latches with a common active LOW Enable input and active LOW Master Reset input. When the Enable goes HIGH, data present in the latches is stored and the state of the latch is no longer affected by the $\overline{S}_n$ and D_n inputs. The Master Reset when activated overrides all other input conditions forcing all latch outputs LOW. Each of the four latches can be operated in one of two modes:

D-TYPE-LATCH—For D-type operation the $\overline{S}$ input of a latch is held LOW. While the common Enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the Enable goes HIGH.

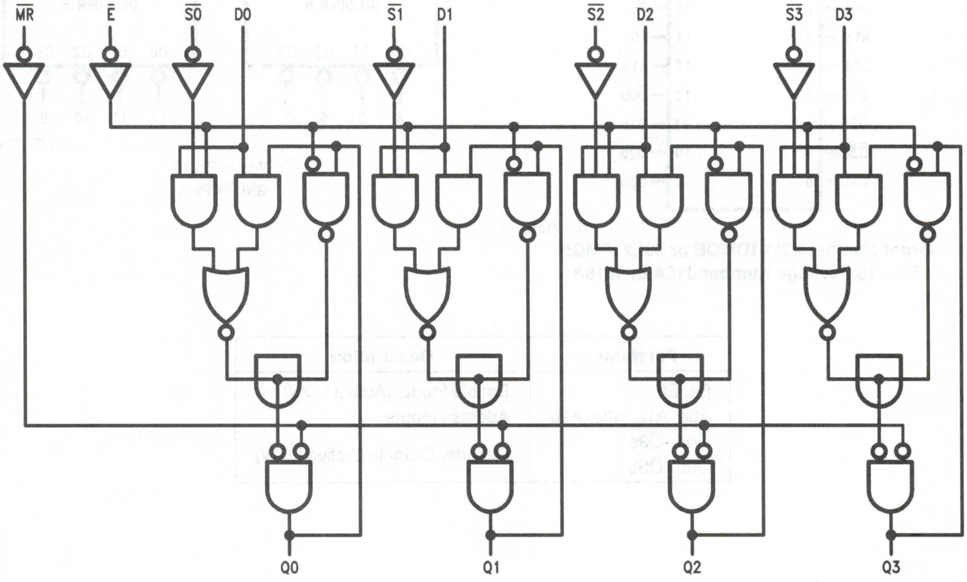
SET/RESET LATCH—During set/reset operation when the common Enable is LOW a latch is reset by a LOW on the D input, and can be set by a LOW on the $\overline{S}$ input if the D input is HIGH. If both $\overline{S}$ and D inputs are LOW, the D input will dominate and the latch wil be reset. When the Enable goes HIGH, the latch remains in the last state prior to disablement. The two modes of latch operation are shown in the Truth Table.

Truth Table

$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_n	Operation
H	L	L	L	L	D Mode
H	L	H	L	L	
H	H	X	X	Q_{n-1}	
H	L	L	L	L	R/S Mode
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{n-1}	
H	H	X	X	Q_{n-1}	
L	X	X	X	L	RESET

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Q_{n-1} = Previous Output State
Q_n = Present Output State

Logic Diagram



TL/F/9612-3

National Semiconductor

93L21
Dual 1-of-4 Decoder

General Description

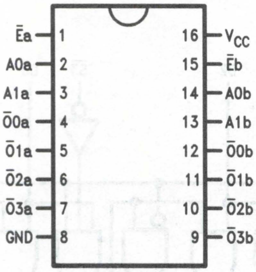
The 93L21 consists of two independent multipurpose decoders, each designed to accept two inputs and provide four mutually exclusive outputs. In addition an active LOW enable input, which gives demultiplexing capability, is provided for each decoder.

Features

- Multifunction capability
- Mutually exclusive outputs
- Demultiplexing capability
- Active low enable for each decoder

Connection Diagram

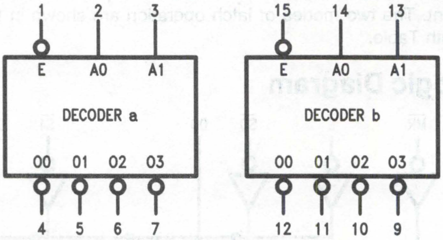
Dual-In-Line Package


Ēa 1
A0a 2
A1a 3
Ō0a 4
Ō1a 5
Ō2a 6
Ō3a 7
GND 8
16 V$_{CC}$
15 Ēb
14 A0b
13 A1b
12 Ō0b
11 Ō1b
10 Ō2b
9 Ō3b

TL/F/10197-1

Order Number 93L21DMQB or 93L21FMQB
See NS Package Number J16A or W16A

Logic Symbol


1
2
3
E
A0
A1
DECODER a
00
01
02
03
4
5
6
7
15
14
13
E
A0
A1
DECODER b
00
01
02
03
12
11
10
9

TL/F/10197-2

V$_{CC}$ = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{E}$a, $\overline{E}$b	Enable Inputs (Active LOW)
A0a, A1a, A0b, A1b	Address Inputs
$\overline{O}$0a–$\overline{O}$3a $\overline{O}$0b–$\overline{O}$3b	Decoder Outputs (Active LOW)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L12 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating	−55		125	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, II = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.3	V
II	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
IIH	High Level Input Current	V_{CC} = Max, V_I = 2.4V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−400	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			13.2	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Functional Description

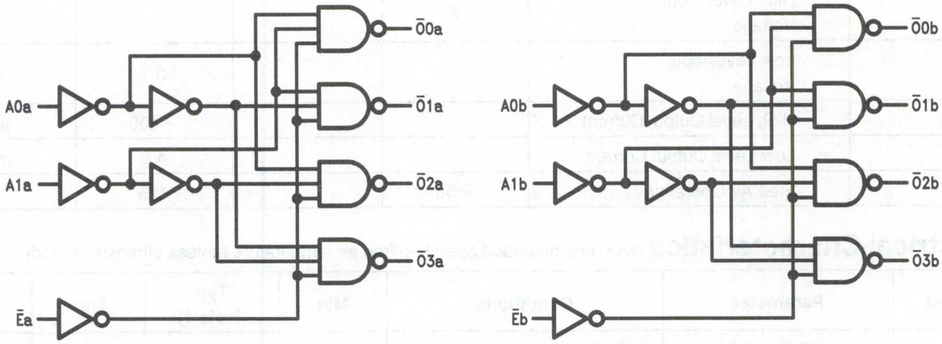
The 93L21 consists of two separate decoders each designed to accept two binary weighted inputs and provide four mutually exclusive active LOW outputs as shown in the logic symbol. Each decoder can be used as a 4-output demultiplexer by using the enable as a data input.

Truth Table (Each Decoder)

Inputs			Outputs			
$\overline{E}$	A0	A1	$\overline{O0}$	$\overline{O1}$	$\overline{O2}$	$\overline{O3}$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram


A0a
A1a
$\overline{E}$a
$\overline{O0}$a
$\overline{O1}$a
$\overline{O2}$a
$\overline{O3}$a
A0b
A1b
$\overline{E}$b
$\overline{O0}$b
$\overline{O1}$b
$\overline{O2}$b
$\overline{O3}$b

TL/F/10197-3

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load.)

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
tPLH tPHL	Propagation Delay An to $\overline{O}$n		50 65	ns
tPLH tPHL	Propagation Delay $\overline{E}$n to $\overline{O}$n		40 52	ns

National Semiconductor

93L22
Quad 2-Input Multiplexer

General Description

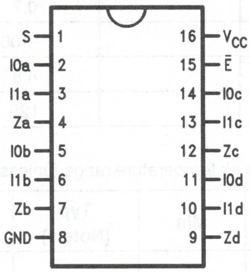
The 93L22 quad 2-input digital multiplexers consist of four multiplexing circuits with common select and enable logic; each circuit contains two inputs and one output.

Features

- Multifunction capability
- On-chip select logic decoding
- Fully buffered outputs

Connection Diagram

Dual-In-Line Package

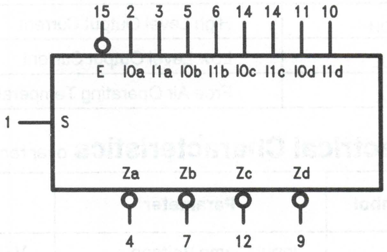

S 1
I0a 2
I1a 3
Za 4
I0b 5
I1b 6
Zb 7
GND 8
16 V_{CC}
15 Ē
14 I0c
13 I1c
12 Zc
11 I0d
10 I1d
9 Zd

TL/F/10198-1

Order Number 93L22DMQB or 93L22FMQB
See NS Package Number J16A or W16A

Pin Names	Description
S	Common Select Input
Ē	Enable Input (Active LOW)
I0a–I0d I1a–I1d	Multiplexer Inputs
Za–Zd	Multiplexer Outputs

Logic Symbol


15
2
3
5
6
14
14
11
10
E
I0a
I1a
I0b
I1b
I0c
I1c
I0d
I1d
1
S
Za
Zb
Zc
Zd
4
7
12
9

TL/F/10198-2

V_{CC} = Pin 16
GND = Pin 8

Truth Table

Inputs				Output
Ē	S	I0n	I1n	Zn
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L22 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.3	V
II	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
IIH	High Level Input Current	V_{CC} = Max, V_I = 2.4V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−400	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, (Note 2)	−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max			13.2	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for test waveforms and output load)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
tPLH tPHL	Propagation Delay S to Zn		36 49	ns
tPLH tPHL	Propagation Delay I0 or I1 to Zn		30 22	ns
tPLH tPHL	Propagation Delay $\overline{E}$ to Zn		27 27	ns

Functional Description

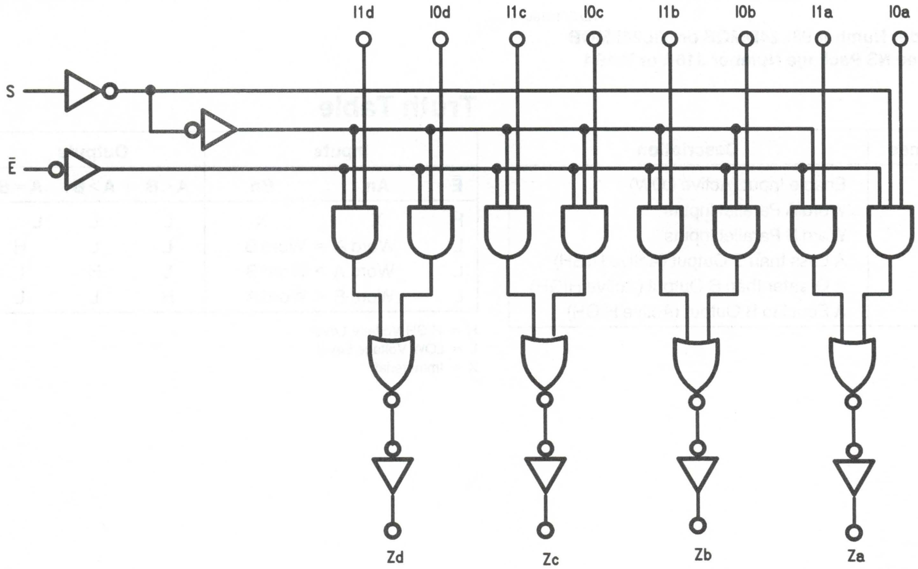
The 93L22 quad 2-input multiplexer provides the ability to select four bits of either data or control from two sources, in one package. The Enable input ($\overline{E}$) is active LOW. When not activated all outputs (Z_n) are LOW regardless of all other inputs.

The 93L22 quad 2-input multiplexer is the logical implementation of a four-pole, two position switch, with the position of the switch being set by the logic levels supplied to the one select input. The logic equations for the outputs are shown below:

$Za = E \bullet (I1a \bullet S + I0a \bullet \overline{S})$ $Zb = E \bullet (I1b \bullet S + I0b \bullet \overline{S})$
$Zc = E \bullet (I1c \bullet S + I0c \bullet \overline{S})$ $Zd = E \bullet (I1d \bullet S + I0d \bullet \overline{S})$

A common use of the 93L22 is the moving of data from a group of registers to four common output busses. The particular register from which the data comes is determined by the state of the select input. A less obvious use is as a function generator. The 93L22 can generate four functions of two variables with one variable common. This is useful for implementing random gating functions.

Logic Diagram



TL/F/10198-3

National Semiconductor

93L24
5-Bit Comparator

General Description

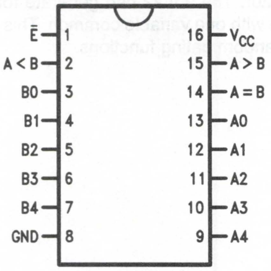
The 93L24 expandable comparator provides comparison between two 5-bit words and gives three outputs—"less than", "greater than" and "equal to". A HIGH on the active LOW Enable Input forces all three outputs LOW.

Features

- Three separate outputs: A<B, A>B, A=B
- Easily expandable
- Active low enable input

Connection Diagram

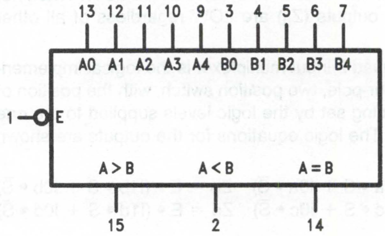
Dual-In-Line Package


Ē 1
A<B 2
B0 3
B1 4
B2 5
B3 6
B4 7
GND 8
16 VCC
15 A>B
14 A=B
13 A0
12 A1
11 A2
10 A3
9 A4

TL/F/10199-1

Order Number 93L24DMQB or 93L24FMQB
See NS Package Number J16A or W16A

Logic Symbol


13 12 11 10 9 3 4 5 6 7
A0 A1 A2 A3 A4 B0 B1 B2 B3 B4
1
E
A>B
A<B
A=B
15
2
14

TL/F/10199-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
Ē	Enable Input (Active LOW)
A0–A4	Word A Parallel Inputs
B0–B4	Word B Parallel Inputs
A<B	A Less than B Output (Active HIGH)
A>B	A Greater than B Output (Active HIGH)
A=B	A Equal to B Output (Active HIGH)

Truth Table

Inputs			Outputs		
Ē	An	Bn	A<B	A>B	A=B
H	X	X	L	L	L
L	Word A =	Word B	L	L	H
L	Word A >	Word B	L	H	L
L	Word B <	Word A	H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L24 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	µA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max			21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to A=B; $\overline{E}$ to A<B, A>B		32 35	ns
t_{PLH} t_{PHL}	Propagation Delay An to A>B; Bn to A>B		54 75	ns
t_{PLH} t_{PHL}	Propagation Delay An to A<B; Bn to A<B		70 77	ns
t_{PLH} t_{PHL}	Propagation Delay An or Bn to A=B		100 102	ns

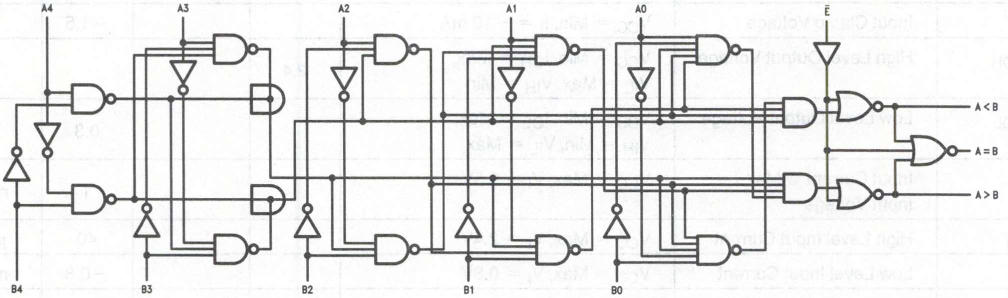
Functional Description

The 93L24 5-bit comparators use combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these ouptuts are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW Enable Input ($\overline{E}$).

Tying the A>B output from one device into an A input on another device and the A< B output into the corresponding B input permits easy expansion.

The A4 and B4 inputs are the most significant inputs and A0, B0 the least significant. Thus if A4 is HIGH and B4 is LOW, the A>B output will be HIGH regardless of all other inputs except $\overline{E}$.

Logic Diagram



TL/F/10199–3

National Semiconductor

93L28
Dual 8-Bit Shift Register

General Description

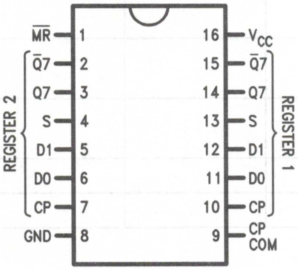
The 93L28 is a high speed serial storage element providing 16 bits of storage in the form of two 8-bit registers. The multifunctional capability of this device is provided by several features: 1) additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources; 2) the clock of each register may be provided separately or together; 3) both the true and complementary outputs are provided from each 8-bit register, and both registers may be master cleared from a common input.

Features

- 2-input multiplexer provided at data input of each register
- Gated clock input circuitry
- Both true and complementary outputs provided from last bit of each register
- Asynchronous master reset common to both registers

Connection Diagram

Dual-In-Line Package

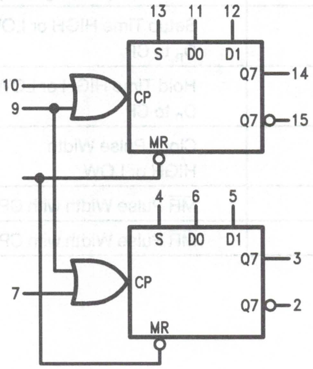


$\overline{MR}$ 1
$\overline{Q7}$ 2
Q7 3
S 4
D1 5
D0 6
CP 7
GND 8
16 V_{CC}
15 $\overline{Q7}$
14 Q7
13 S
12 D1
11 D0
10 CP
9 CP COM
REGISTER 2
REGISTER 1

TL/F/10200-1

Order Number 93L28DMQB or 93L28FMQB
See NS Package Number J16A or W16A

Logic Symbol



13
11
12
S
D0
D1
Q7
14
10
9
CP
$\overline{Q7}$
15
MR
4
6
5
S
D0
D1
Q7
3
7
CP
$\overline{Q7}$
2
MR

TL/F/10200-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
S	Data Select Input
D0, D1	Data Inputs
CP	Clock Pulse Input (Active HIGH)
	Common (Pin 9)
	Separate (Pins 7 and 10)
$\overline{MR}$	Master Reset Input (Active LOW)
Q7	Last Stage Output
$\overline{Q7}$	Complementary Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L28 (MIL)			Units
		Min	**Nom**	**Max**	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW D_n to CP	30 30			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW D_n to CP	0 0			ns
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	55 55			ns
$t_w(L)$	$\overline{MR}$ Pulse Width with CP HIGH	60			ns
$t_w(L)$	$\overline{MR}$ Pulse Width with CP LOW	70			ns

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V	$\overline{MR}$, Dx			20	µA
			CP (7, 10)			30	
			S			40	
			CP Com			60	
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.3V	$\overline{MR}$, Dx			−400	µA
			CP (7, 10)			−600	
			S			−800	
			CP Com			−1200	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max				25.3	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for test waveforms and output load)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Shift Right Frequency	5.0		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_7 or $\overline{Q}_7$		45 80	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_7		110	ns

Functional Description

The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW-to-HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH-to-LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal.

Each 8-bit shift register has a 2-input multiplexer in front of the serial data input. The two data inputs D0 and D1 are controlled by the data select input (S) following the Boolean expression:

Serial data in: $S_D = \overline{S}D0 + SD1$

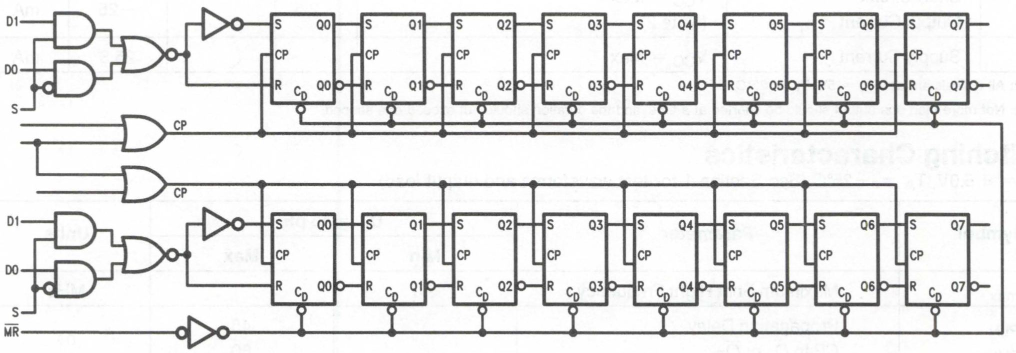
An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all 16 stages independently of any other input signal.

Shift Select Table

Inputs			Output
S	**D0**	**D1**	**Q7 (t_{n+8})**
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
n+8 = Indicates state after eight clock pulse

Logic Diagram



TL/F/10200-3

National Semiconductor

93L34
8-Bit Addressable Latch

General Description

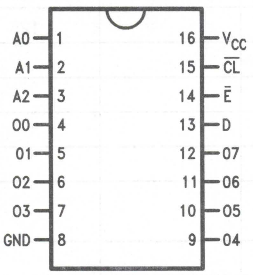
The 93L34 is an 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level HIGH outputs. The device also incorporates an active LOW common clear for resetting all latches, as well as, an active LOW enable.

Features

- Serial to parallel capability
- Eight bits of storage with output of each bit available
- Random (addressable) data entry
- Active high demultiplexing or decoding capability
- Easily expandable
- Common conditional clear

Connection Diagram

Dual-In-Line Package

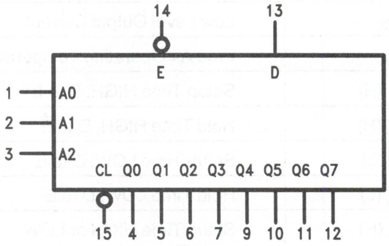


A0 1
A1 2
A2 3
O0 4
O1 5
O2 6
O3 7
GND 8
16 V_{CC}
15 $\overline{CL}$
14 $\overline{E}$
13 D
12 O7
11 O6
10 O5
9 O4

TL/F/10201-1

Order Number 93L34DMQB or 93L34FMQB
See NS Package Number J16A or W16A

Logic Symbol



14
13
E
D
1
2
3
A0
A1
A2
CL
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
15
4
5
6
7
9
10
11
12

TL/F/10201-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A3	Address Inputs
D	Data Input
$\overline{E}$	Enable Input (Active LOW)
$\overline{CL}$	Clear Input (Active LOW)
Q0–Q7	Parallel Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L34 (Mil) Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Voltage			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H)	Setup Time HIGH, D to $\overline{E}$	45			ns
t_h (H)	Hold Time HIGH, D to $\overline{E}$	−5			ns
t_s (L)	Setup Time LOW, D to $\overline{E}$	45			ns
t_h (L)	Hold Time LOW, D to $\overline{E}$	−7			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to $\overline{E}$	10 10			ns
t_w (L)	$\overline{E}$ Pulse Width LOW	26			ns
t_w (L)	$\overline{CL}$ Pulse Width LOW	35			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			20	μA
			$\overline{E}$			30	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Inputs			−0.4	mA
			$\overline{E}$			−0.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		45 42	ns
t_{PLH} t_{PHL}	Propagation Delay D to Q_n		65 45	ns
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n		66 66	ns
t_{PHL}	Propagation Delay $\overline{CL}$ to Q_n		55	ns

Functional Description

The 93L34 has four modes of operation which are shown in the Mode Select Table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the Data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the Enable should be held HIGH while the Address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the 93L34 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

Mode Select Table

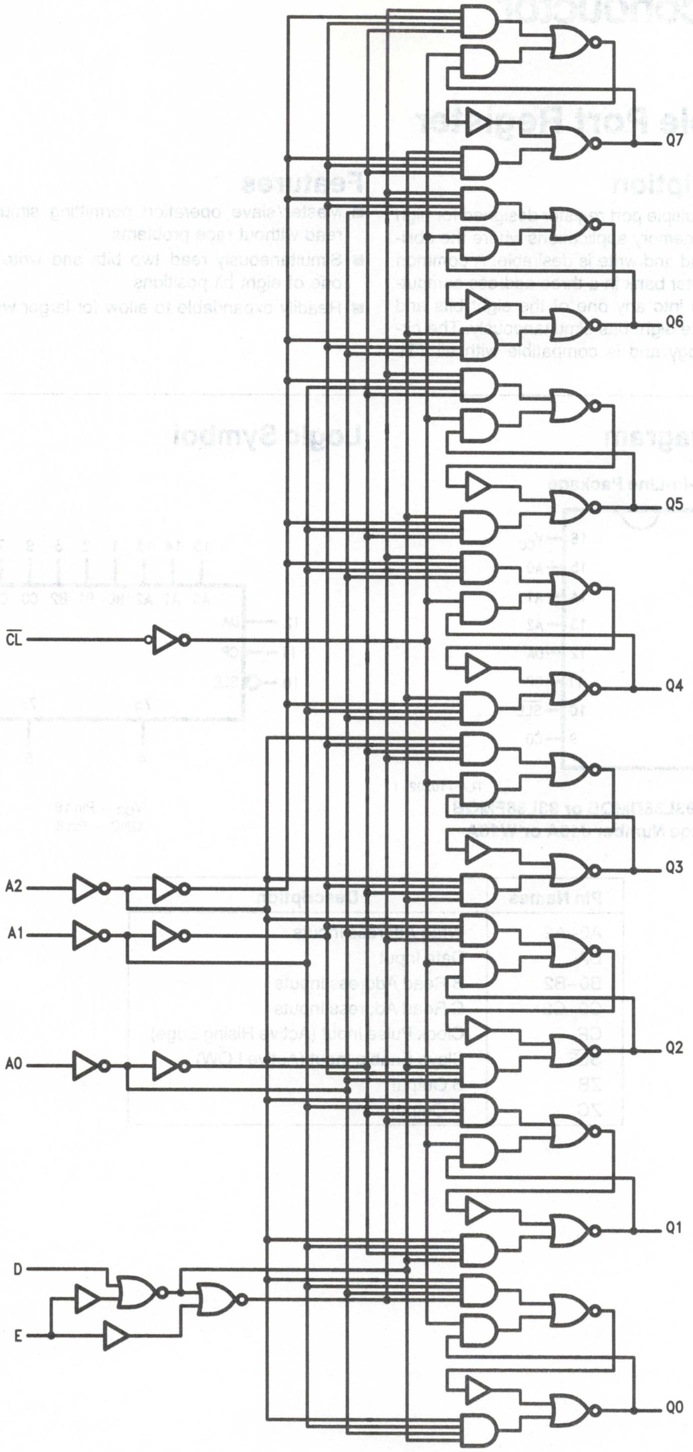
$\overline{E}$	$\overline{CL}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

Truth Table

Inputs					Outputs								Mode
$\overline{CL}$	$\overline{E}$	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	H	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	D	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	D	L	L	L	L	L	L	
L	L	L	H	L	L	L	D	L	L	L	L	L	
•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	
L	L	H	H	H	L	L	L	L	L	L	L	L	
H	H	X	X	X	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Memory
H	L	L	L	L	D	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Addressable
H	L	H	L	L	Qt−1	D	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Latch
H	L	L	H	L	Qt−1	Qt−1	D	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	
•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	
H	L	H	H	H	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	D	

H = HIGH Voltage Level   L = LOW Voltage Level   X = Immaterial   Qt−1 = Previous Output State

Logic Diagram


Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
$\overline{CL}$
A2
A1
A0
D
E

TL/F/10201-3

National Semiconductor

93L38
8-Bit Multiple Port Register

General Description

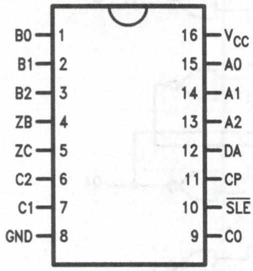
The 93L38 is an 8-bit multiple port register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the eight bits and read from any two of the eight bits simultaneously. The circuit uses TTL technology and is compatible with all TTL families.

Features

- Master/slave operation permitting simultaneous write/read without race problems
- Simultaneously read two bits and write one bit in any one of eight bit positions
- Readily expandable to allow for larger word sizes

Connection Diagram

Dual-In-Line Package

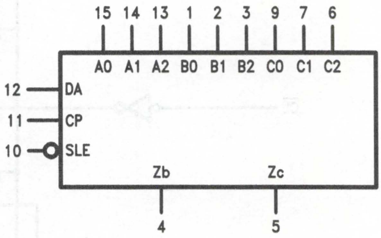


B0 1
B1 2
B2 3
ZB 4
ZC 5
C2 6
C1 7
GND 8
16 V_CC
15 A0
14 A1
13 A2
12 DA
11 CP
10 SLE
9 C0

TL/F/10202-1

Order Number 93L38DMQB or 93L38FMQB
See NS Package Number J16A or W16A

Logic Symbol



15
14
13
1
2
3
9
7
6
A0
A1
A2
B0
B1
B2
C0
C1
C2
12 DA
11 CP
10 SLE
Zb
Zc
4
5

TL/F/10202-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A2	Write Address Inputs
DA	Data Input
B0–B2	B Read Address Inputs
C0–C2	C Read Address Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{\text{SLE}}$	Slave Enable Input (Active LOW)
ZB	B Output
ZC	C Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range Military	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L38 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_A to CP	30 22			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_A to CP	0 −4.0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to CP	0 0			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to CP	0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	40 30			ns

Electrical Characteristics over recommended operating free air temperature (unless othewise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			70	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all input grounded.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for Test Waveforms and Output Load

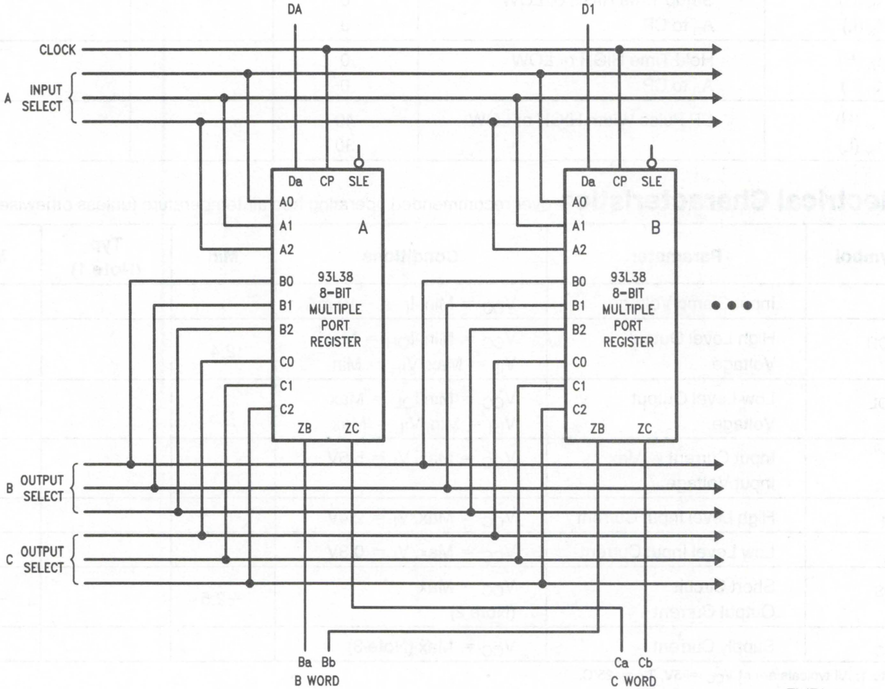
Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH}	Propagation Delay		68	ns
t_{PHL}	B_n or C_n or Z_n		95	
t_{PLH}	Propagation Delay		70	ns
t_{PHL}	D_A to Z_n		92	
t_{PLH}	Propagation Delay		65	ns
t_{PHL}	CP to Z_n		57	

Functional Description

The 93L38 8-bit multiple port register can be considered a 1-bit slice of eight high speed working registers. Data can be written into any one and read from any two of the eight locations simultaneously. Master/slave operation eliminates all race problems associated with simultaneous read/write activity from the same location. When the clock input (CP) is LOW data applied to the data input line (D_A) enters the selected master. This selection is accomplished by coding the three write input select lines (A0–A2) appropriately. Data is stored synchronously with the rising edge of the clock pulse.

The information for each of the two slaved (output) latches is selected by two sets of read address inputs (B0–B2 and C0–C2). The information enters the slave while the clock is HIGH and is stored while the clock is LOW. If Slave Enable is LOW ($\overline{SLE}$), the slave latches are continuously enabled. The signals are available on the output pins (Z_B and Z_C). The input bit selection and the two output bit selections can be accomplished independently or simultaneously. The data flows into the device, is demultiplexed according to the state of the write address lines and is clocked into the selected latch. The eight latches function as masters and store the input data. The two output latches are slaves and hold the data during the read operation. The state of each slave is determined by the state of the master selected by its associated set of read address inputs.

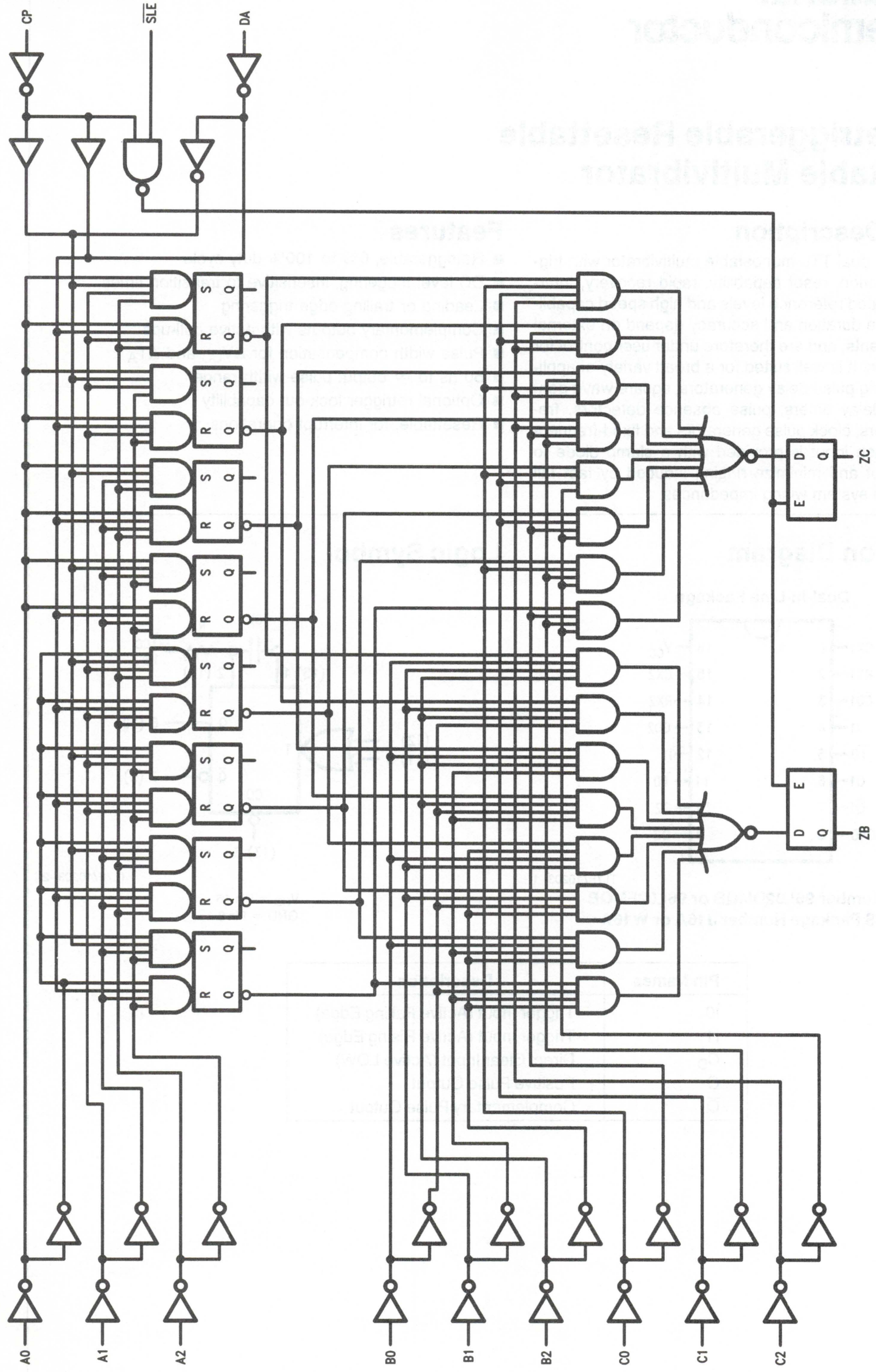
The method of parallel expansion is shown in *Figure A*. One 93L38 is needed for each bit of the required word length. The read and write input lines should be connected in common on all of the devices. This register configuration provides two words of n-bits each at one time, where n devices are connected in parallel.



TL/F/10202-4

FIGURE A. Parallel Expansion

Logic Diagram


CP
$\overline{\text{SLE}}$
DA
S
R
Q
D
E
ZC
ZB
A0
A1
A2
B0
B1
B2
C0
C1
C2

TL/F/10202-3

National Semiconductor

96L02
Dual Retriggerable Resettable Monostable Multivibrator

General Description

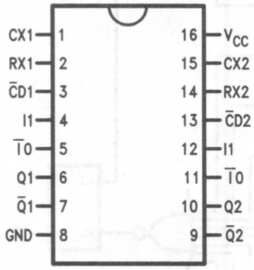
The 96L02 is a dual TTL monostable multivibrator with trigger mode selection, reset capability, rapid recovery, internally compensated reference levels and high speed capability. Output pulse duration and accuracy depend on external timing components, and are therefore under user control for each application. It is well suited for a broad variety of applications, including pulse delay generators, square wave generators, long delay timers, pulse absence detectors, frequency detectors, clock pulse generators and fixed-frequency dividers. Each input is provided with a clamp diode to limit undershoot and minimize ringing induced by fast fall times acting on system wiring impedances.

Features

- Retriggerable, 0% to 100% duty cycle
- DC level triggering, insensitive to transition times
- Leading or trailing-edge triggering
- Complementary outputs with active pull-ups
- Pulse width compensation for ΔV_{CC} and ΔT_A
- 50 ns to ∞ output pulse width range
- Optional retrigger lock-out capability
- Resettable, for interrupt operations

Connection Diagram

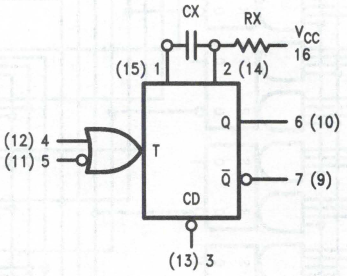
Dual-In-Line Package



TL/F/10203-1

Order Number 96L02DMQB or 96L02FMQB
See NS Package Number J16A or W16A

Logic Symbol



TL/F/10203-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{I}$0	Trigger Input (Active Falling Edge)
I1	Trigger Input (Active Rising Edge)
$\overline{C}_D$	Direct Clear Input (Active LOW)
Q	Positive Pulse Output
$\overline{Q}$	Complementary Pulse Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range Military	−55°C to +125°C
Storage Temperature Range	−65°C to +150°

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Conditions	96L02 (Mil)			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.7	V
I_{OH}	High Level Output Current				0.36	mA
I_{OL}	Low Level Output Current				4.8	mA
T_A	Free Air Operating Temperature		−55		125	°C
t_w (L) t_w (H)	Minimum Input Pulse Width, I1, $\overline{I0}$	$V_{CC} = 5.0V$			50	ns
t_w (min)	Minimum Output Pulse Width at Q, $\overline{Q}$	$V_{CC} = 5.0V$, $R_X = 20\ k\Omega$ $C_X = 0$, $C_L = 15\ pF$	10		300	ns
t_w	Output Pulse Width, Q, $\overline{Q}$	$V_{CC} = 5.0V$, $R_X = 39\ k\Omega$ $C_X = 1000\ pF$	11.5		14.2	µs
R_X	Timing Resistor Range				100	kΩ

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = $ Min, $I_I = -10\ mA$			−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = $ Min, $I_{OH} = $ Max, $V_{IL} = $ Max, $V_{IH} = $ Min	2.4			V
V_{OL}	Low Level Output Voltage	$V_{CC} = $ Min, $I_{OL} = $ Max, $V_{IL} = $ Min, $V_{IL} = $ Max			0.3	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = $ Max, $V_I = 5.5V$			1	mA
I_{IH}	High Level Input Current	$V_{CC} = $ Max, $V_I = 2.4V$			20	µA
I_{IL}	Low Level Input Current	$V_{CC} = $ Max, $V_I = 0.3V$			−0.4	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = $ Max (Note 2)	−2.0		−13.0	mA
I_{CC}	Supply Current	$V_{CC} = $ Max (Note 3)			16	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

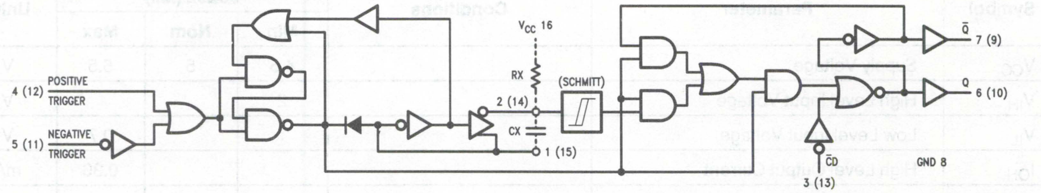
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics $V_{CC} = +5.0V, T_A = +25°C$

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay $\overline{\text{I}}$0 to Q, I1 to Q	$V_{CC} = 5.0V, R_X = 20\ k\Omega$ $C_X = 0, C_L = 15\ pF$		75	ns
t_{PHL}	Propagation Delay $\overline{\text{I}}$0 to $\overline{Q}$, I1 to $\overline{Q}$	$V_{CC} = 5.0V, R_X = 20\ k\Omega$ $C_X = 0, C_L = 15\ pF$		62	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CD}$ to $\overline{Q}$, $\overline{CD}$ to Q	$V_{CC} = 5.0V, R_X = 39\ k\Omega$ $C_X = 1000\ pF$		100	ns

Functional Block Diagram



TL/F/10203-3

Operation Notes

1. TRIGGERING—can be accomplished by a positive-going transition on pin 4 (12) or a negative-going transition on pin 5 (11). Triggering begins as a signal crosses the input $V_{IL}:V_{IH}$ threshold region; this activates an internal latch whose unbalanced cross-coupling causes it to assume a preferred state. As the latch output goes LOW it disables the gates leading to the Q output and, through an inverter, turns on the capacitor discharge transistor. The inverted signal is also fed back to the latch input to change its state and effectively end the triggering action; thus the latch and its associated feed-back perform the function of a differentiator.

   The emitters of the latch transistors return to ground through an enabling transistor which must be turned off between successive triggers in order for the latch to proceed through the proper sequence when triggering is desired. Pin 5 (11) must be HIGH in order to trigger at pin 4 (12); conversely, pin 4 (12) must be LOW in order to trigger at pin 5 (11).

2. RETRIGGERING—In a normal cycle, triggering initiates a rapid discharge of the external timing capacitor, followed by a ramp voltage run-up at pin 2 (14). The delay will time out when the ramp voltage reaches the upper trigger point of a Schmitt circuit, causing the outputs to revert to the quiescent state. If another trigger occurs before the ramp voltage reaches the Schmitt threshold, the capacitor will be discharged and the ramp will start again without having disturbed the output. The delay period can therefore be extended for an arbitrary length of time by insuring that the interval between triggers is less than the delay time, as determined by the external capacitor and resistor.

3. NON-RETRIGGERABLE OPERATION—Retriggering can be inhibited logically, by connecting pin 6 (10) back to pin 4 (12) or by connecting pin 7 (9) back to pin 5 (11). Either hook-up has the effect of keeping the latch-enabling transistor turned on during the delay period, which prevents the input latch from cycling as discussed above in the section on triggering.

4. OUTPUT PULSE WIDTH—An external resistor R_X and an external capacitor C_X are required, as shown in the functional block diagram. To minimize stray capacitance and noise pickup, R_X and C_X should be located as close as possible to the circuit. In applications which require remote trimming of the pulse width, as with a variable resistor, R_X should consist of a fixed resistor in series with the variable resistor; the fixed resistor should be located as close as possible to the circuit. The output pulse width t_w is defined as follows, where R_X is in kΩ, C_X is in pF and t_w is in ns.

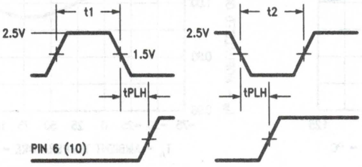
   $$t_w = 0.33\ R_X C_X (1 + 3/R_X) \text{ for } C_X \geq 10^3\ pF$$

   $$20\ k\Omega \leq R_X \leq 100\ k\Omega \text{ for } -55°C \text{ to } +125°C$$

   C_X may vary from 0 to any value. For pulse widths with C_X less than 10^3 pF see *Figure a.*

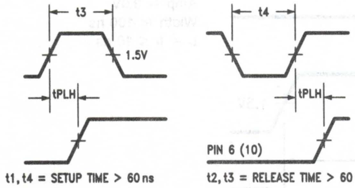
Operation Notes (Continued)

5. SETUP AND RELEASE TIMES—The setup times listed below are necessary to allow the latch-enabling transistor to turn off and the node voltages within the input latch to stabilize, thus insuring proper cycling of the latch when the next trigger occurs. The indicated release times (equivalent to trigger duration) allow time for the input latch to cycle and its signal to propagate.



TL/F/10203-4

Input to Pin 5 (11)
Pin 4 (12) = L
Pin 3 (13) = H

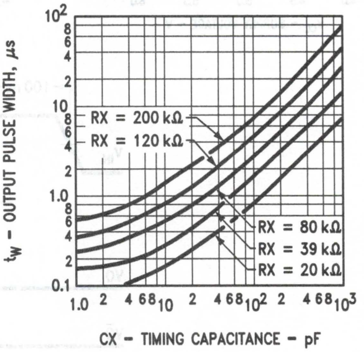


TL/F/10203-5

Input to Pin 4 (12)
Pins 5 (11) and 3 (13) = H

6. RESET OPERATION—A LOW signal on $\overline{C}_D$, pin 3 (13), will terminate an output pulse, causing Q to go LOW and $\overline{Q}$ to go HIGH. As long as $\overline{C}_D$ is held LOW, a delay period cannot be initiated nor will attempted triggering cause spikes at the outputs. A reset pulse duration, in the LOW state, of 25 ns is sufficient to insure resetting. If the reset input goes LOW at the same time that a trigger transition occurs, the reset will dominate and the outputs will not respond to the trigger. If the reset input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.

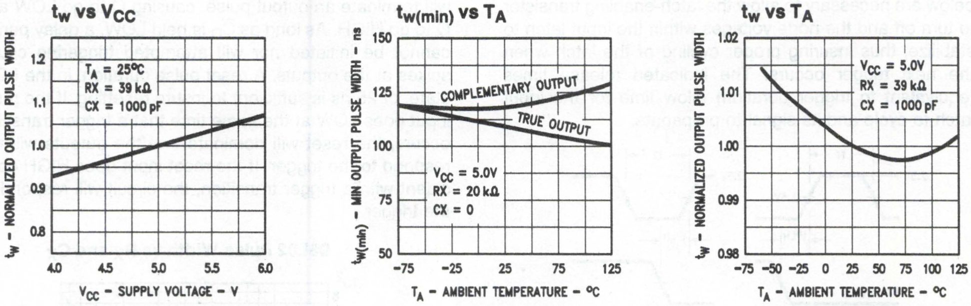
96L02 Pulse Width vs R_X and C_X



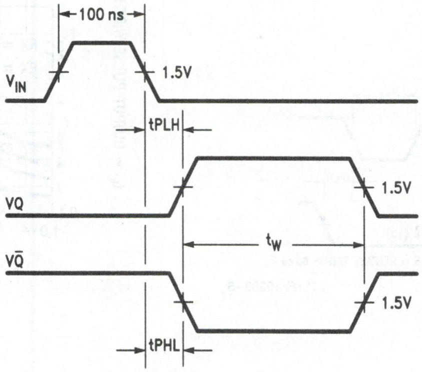
TL/F/10203-6

FIGURE a

Typical Characteristics



TL/F/10203–7


100 ns
1.5V
V_{IN}
tPLH
VQ
1.5V
t_W
$V\bar{Q}$
1.5V
tPHL

INPUT PULSE
f ≅ 25 kHz
Amp ≅ 3.0V
Width ≅ 100 ns
$t_r = t_f \leq 10$ ns

TL/F/10203–8

FIGURE b

Section 6

Physical Dimensions

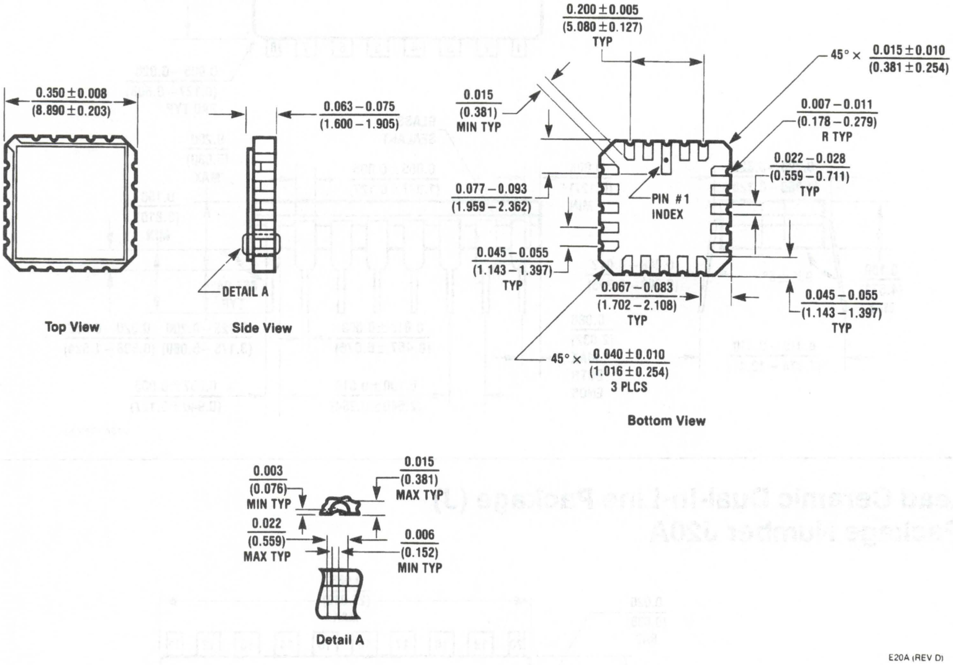
Section 6—Physical Dimensions

Physical Dimensions 6-3
Data Bookshelf
Sales and Distribution Offices

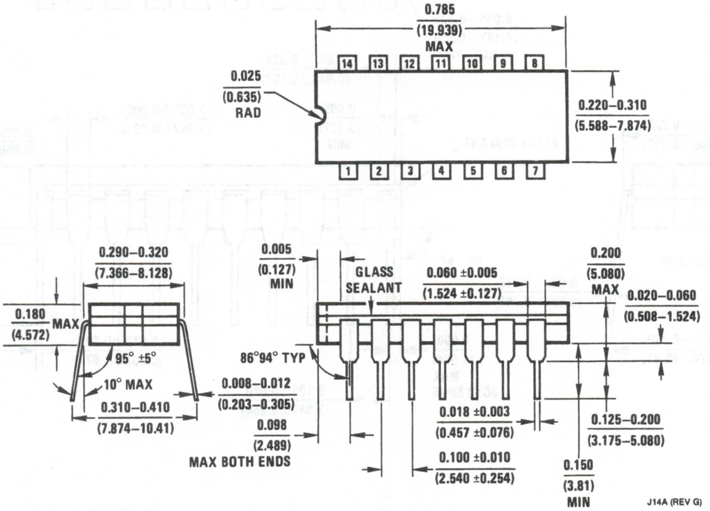
National Semiconductor

All dimensions are in inches (millimeters)

20 Terminal Ceramic Leadless Chip Carrier (E)
NS Package Number E20A

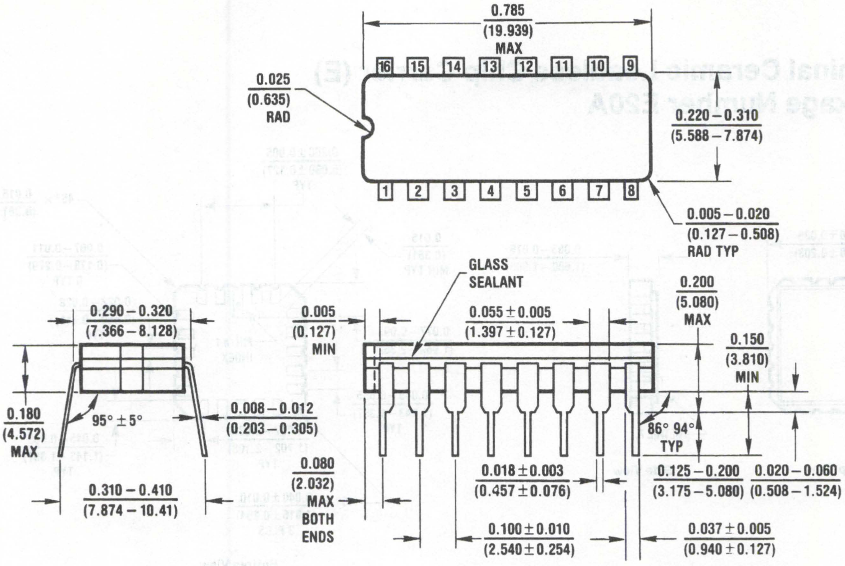

0.350 ± 0.008
(8.890 ± 0.203)
Top View
0.063 – 0.075
(1.600 – 1.905)
DETAIL A
Side View
0.200 ± 0.005
(5.080 ± 0.127)
TYP
45° × 0.015 ± 0.010
(0.381 ± 0.254)
0.015
(0.381)
MIN TYP
0.007 – 0.011
(0.178 – 0.279)
R TYP
0.022 – 0.028
(0.559 – 0.711)
TYP
0.077 – 0.093
(1.959 – 2.362)
PIN #1
INDEX
0.045 – 0.055
(1.143 – 1.397)
TYP
0.067 – 0.083
(1.702 – 2.108)
TYP
0.045 – 0.055
(1.143 – 1.397)
TYP
45° × 0.040 ± 0.010
(1.016 ± 0.254)
3 PLCS
Bottom View
0.003
(0.076)
MIN TYP
0.015
(0.381)
MAX TYP
0.022
(0.559)
MAX TYP
0.006
(0.152)
MIN TYP
Detail A
E20A (REV D)

14 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J14A


0.785
(19.939)
MAX
14
13
12
11
10
9
8
0.025
(0.635)
RAD
0.220–0.310
(5.588–7.874)
1
2
3
4
5
6
7
0.290–0.320
(7.366–8.128)
0.180
(4.572)
MAX
95° ±5°
10° MAX
0.310–0.410
(7.874–10.41)
0.005
(0.127)
MIN
GLASS
SEALANT
0.060 ±0.005
(1.524 ±0.127)
0.200
(5.080)
MAX
0.020–0.060
(0.508–1.524)
86°94° TYP
0.008–0.012
(0.203–0.305)
0.098
(2.489)
MAX BOTH ENDS
0.018 ±0.003
(0.457 ±0.076)
0.125–0.200
(3.175–5.080)
0.100 ±0.010
(2.540 ±0.254)
0.150
(3.81)
MIN
J14A (REV G)

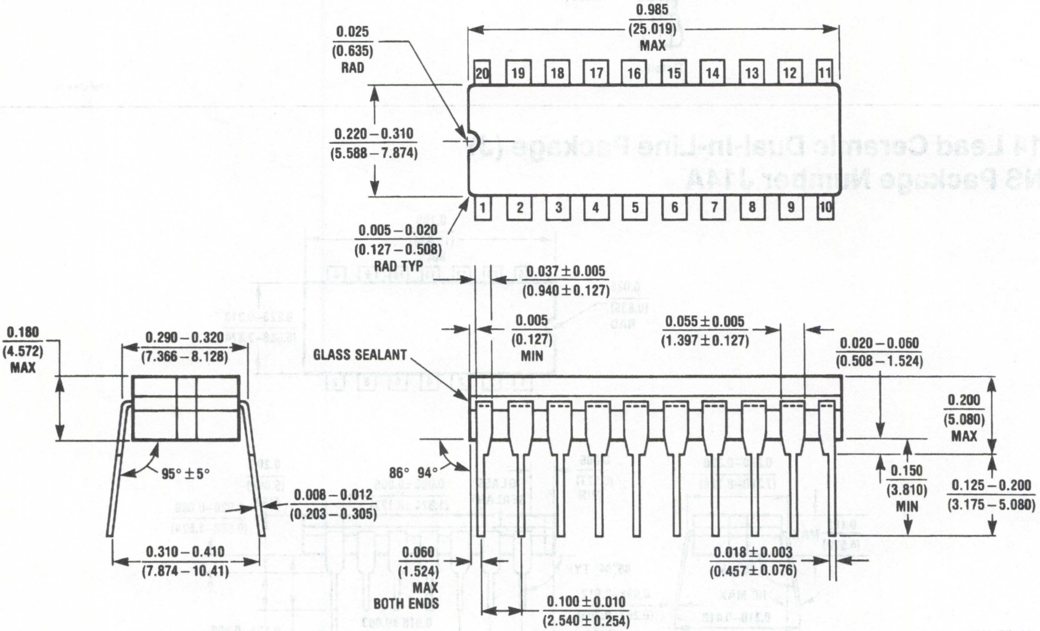
Physical Dimensions

16 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J16A


0.785
(19.939)
MAX
16
15
14
13
12
11
10
9
0.025
(0.635)
RAD
0.220 – 0.310
(5.588 – 7.874)
1
2
3
4
5
6
7
8
0.005 – 0.020
(0.127 – 0.508)
RAD TYP
GLASS
SEALANT
0.200
(5.080)
MAX
0.290 – 0.320
(7.366 – 8.128)
0.005
(0.127)
MIN
0.055 ± 0.005
(1.397 ± 0.127)
0.150
(3.810)
MIN
0.180
(4.572)
MAX
95° ± 5°
0.008 – 0.012
(0.203 – 0.305)
86° 94°
TYP
0.080
(2.032)
MAX
BOTH
ENDS
0.018 ± 0.003
(0.457 ± 0.076)
0.125 – 0.200
(3.175 – 5.080)
0.020 – 0.060
(0.508 – 1.524)
0.310 – 0.410
(7.874 – 10.41)
0.100 ± 0.010
(2.540 ± 0.254)
0.037 ± 0.005
(0.940 ± 0.127)

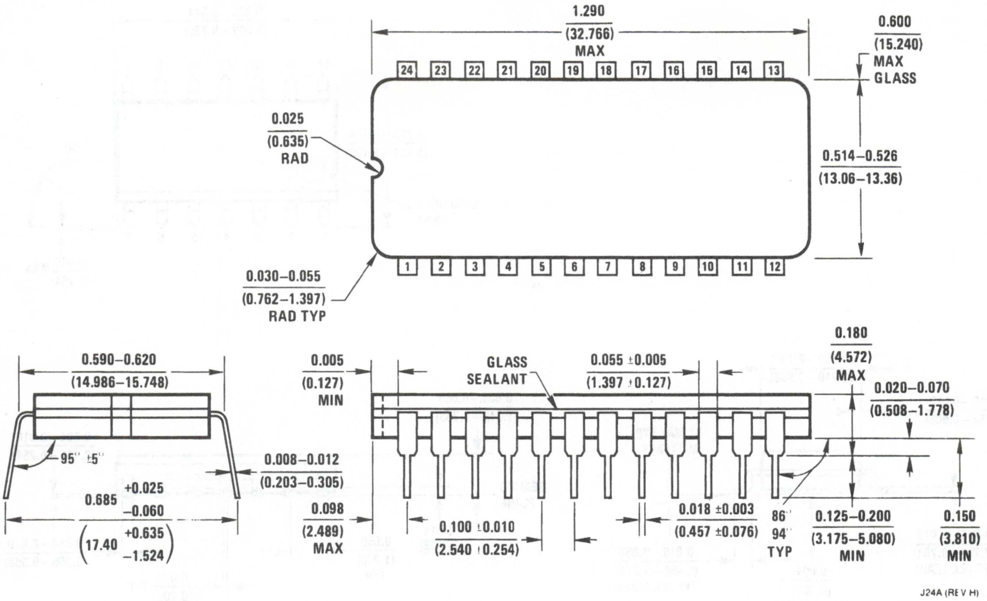
J16A (REV K)

20 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J20A

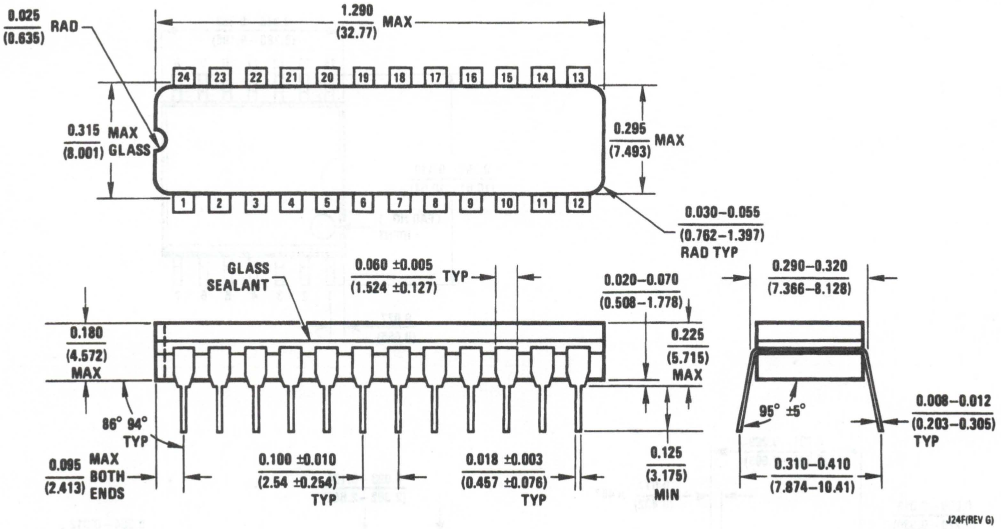

0.985
(25.019)
MAX
0.025
(0.635)
RAD
20
19
18
17
16
15
14
13
12
11
0.220 – 0.310
(5.588 – 7.874)
1
2
3
4
5
6
7
8
9
10
0.005 – 0.020
(0.127 – 0.508)
RAD TYP
0.037 ± 0.005
(0.940 ± 0.127)
0.180
(4.572)
MAX
0.290 – 0.320
(7.366 – 8.128)
GLASS SEALANT
0.005
(0.127)
MIN
0.055 ± 0.005
(1.397 ± 0.127)
0.020 – 0.060
(0.508 – 1.524)
0.200
(5.080)
MAX
95° ± 5°
86° 94°
0.008 – 0.012
(0.203 – 0.305)
0.150
(3.810)
MIN
0.125 – 0.200
(3.175 – 5.080)
0.310 – 0.410
(7.874 – 10.41)
0.060
(1.524)
MAX
BOTH ENDS
0.018 ± 0.003
(0.457 ± 0.076)
0.100 ± 0.010
(2.540 ± 0.254)

J20A (REV M)

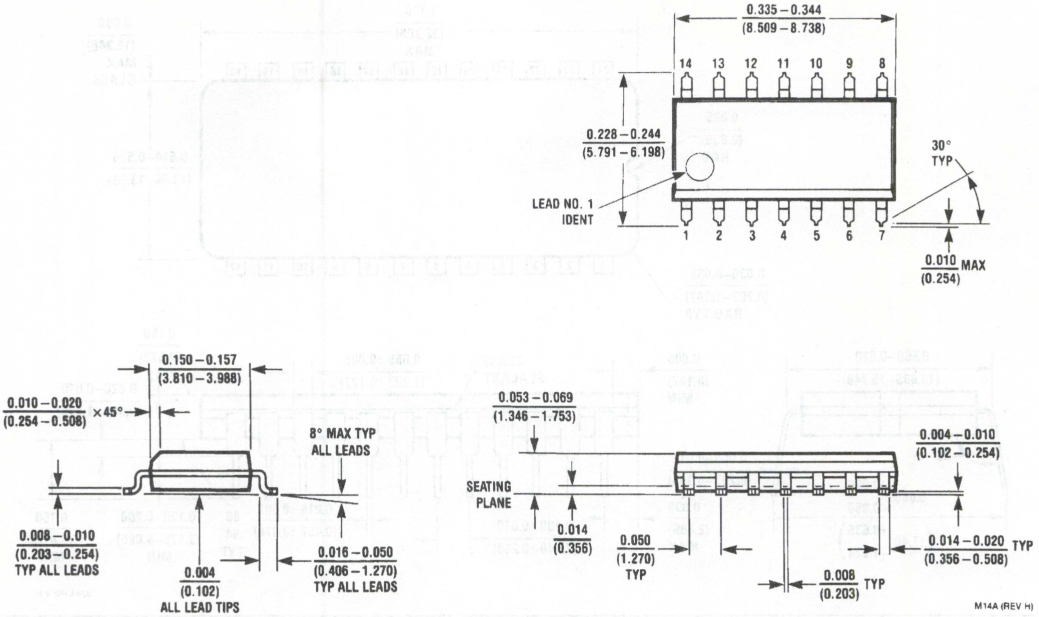
24 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J24A


1.290
(32.766)
MAX
0.600
(15.240)
MAX
GLASS
24 23 22 21 20 19 18 17 16 15 14 13
0.025
(0.635)
RAD
0.514–0.526
(13.06–13.36)
1 2 3 4 5 6 7 8 9 10 11 12
0.030–0.055
(0.762–1.397)
RAD TYP
0.590–0.620
(14.986–15.748)
95° ±5°
0.008–0.012
(0.203–0.305)
0.685 +0.025 −0.060
(17.40 +0.635 −1.524)
0.005
(0.127)
MIN
0.098
(2.489)
MAX
GLASS
SEALANT
0.055 ±0.005
(1.397 ±0.127)
0.100 ±0.010
(2.540 ±0.254)
0.018 ±0.003
(0.457 ±0.076)
86°
94°
TYP
0.180
(4.572)
MAX
0.020–0.070
(0.508–1.778)
0.125–0.200
(3.175–5.080)
MIN
0.150
(3.810)
MIN
J24A (REV H)

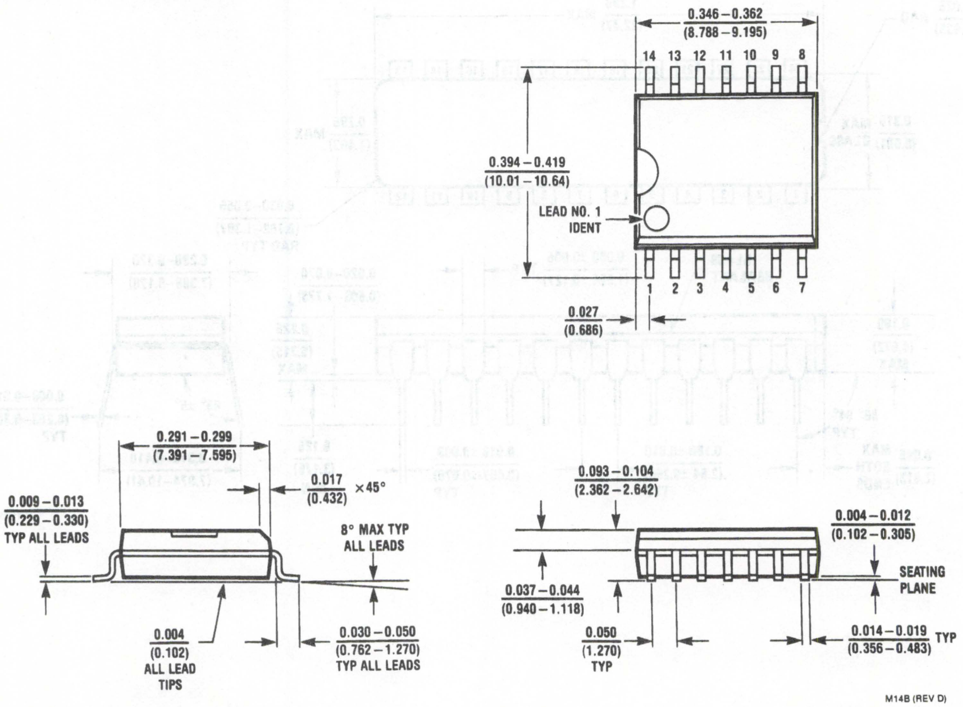
24 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J24F


0.025
(0.635)
RAD
1.290
(32.77)
MAX
24 23 22 21 20 19 18 17 16 15 14 13
0.315
(8.001)
MAX
GLASS
0.295
(7.493)
MAX
1 2 3 4 5 6 7 8 9 10 11 12
0.030–0.055
(0.762–1.397)
RAD TYP
GLASS
SEALANT
0.060 ±0.005
(1.524 ±0.127)
TYP
0.020–0.070
(0.508–1.778)
0.290–0.320
(7.366–8.128)
0.180
(4.572)
MAX
0.225
(5.715)
MAX
95° ±5°
0.008–0.012
(0.203–0.305)
TYP
86° 94°
TYP
0.095
(2.413)
MAX
BOTH
ENDS
0.100 ±0.010
(2.54 ±0.254)
TYP
0.018 ±0.003
(0.457 ±0.076)
TYP
0.125
(3.175)
MIN
0.310–0.410
(7.874–10.41)
J24F(REV G)

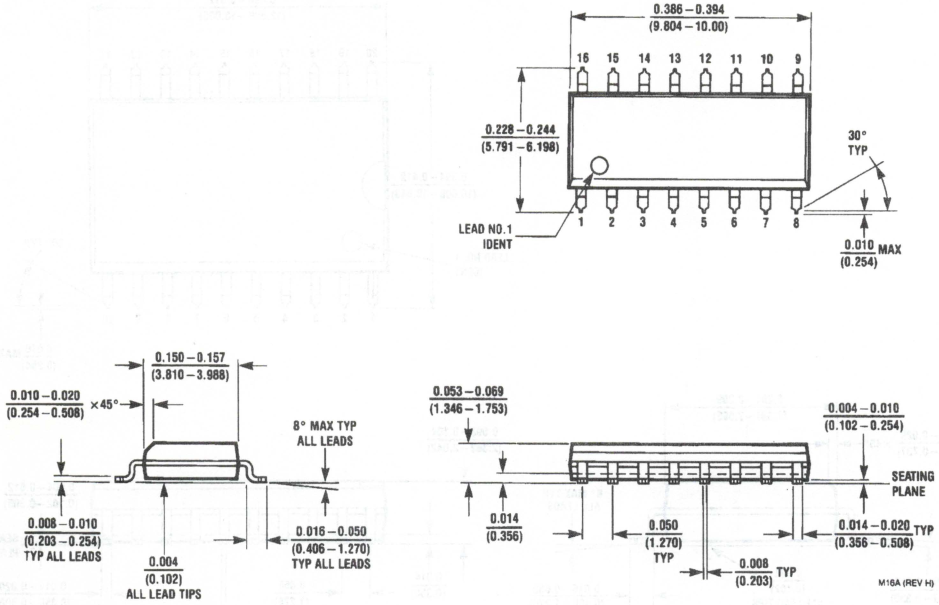
14 Lead (0.150" Wide) Molded Small Outline Package (M)
NS Package Number M14A


0.335 – 0.344
(8.509 – 8.738)
14 13 12 11 10 9 8
0.228 – 0.244
(5.791 – 6.198)
30° TYP
LEAD NO. 1 IDENT
1 2 3 4 5 6 7
0.010 MAX
(0.254)
0.150 – 0.157
(3.810 – 3.988)
0.010 – 0.020
(0.254 – 0.508) × 45°
8° MAX TYP ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
SEATING PLANE
0.014
(0.356)
0.008 – 0.010
(0.203 – 0.254)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.050
(1.270)
TYP
0.008
(0.203) TYP
0.014 – 0.020 TYP
(0.356 – 0.508)
M14A (REV H)

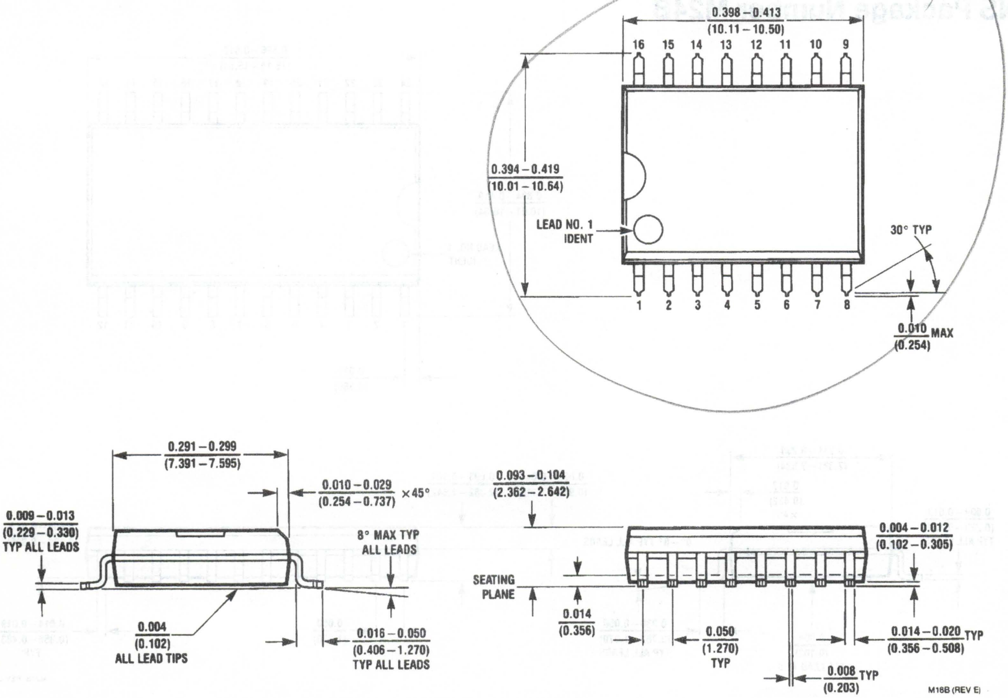
14 Lead (0.300" Wide) Molded Small Outline Package (M)
NS Package Number M14B


0.346 – 0.362
(8.788 – 9.195)
14 13 12 11 10 9 8
0.394 – 0.419
(10.01 – 10.64)
LEAD NO. 1 IDENT
1 2 3 4 5 6 7
0.027
(0.686)
0.291 – 0.299
(7.391 – 7.595)
0.017
(0.432) ×45°
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
8° MAX TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.030 – 0.050
(0.762 – 1.270)
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
SEATING PLANE
0.037 – 0.044
(0.940 – 1.118)
0.050
(1.270)
TYP
0.014 – 0.019 TYP
(0.356 – 0.483)
M14B (REV D)

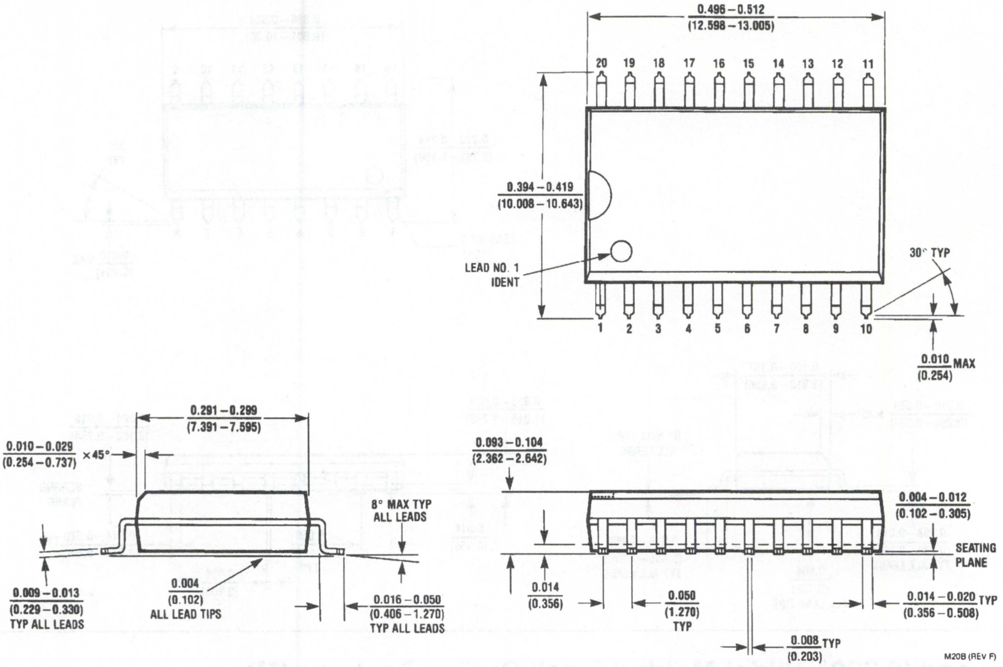
16 Lead (0.150″ Wide) Molded Small Outline Package (M)
NS Package Number M16A


0.386 – 0.394
(9.804 – 10.00)
16 15 14 13 12 11 10 9
0.228 – 0.244
(5.791 – 6.198)
30° TYP
LEAD NO. 1 IDENT
1 2 3 4 5 6 7 8
0.010 MAX
(0.254)
0.150 – 0.157
(3.810 – 3.988)
0.010 – 0.020
(0.254 – 0.508)
×45°
8° MAX TYP ALL LEADS
0.008 – 0.010
(0.203 – 0.254)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.014
(0.356)
0.050
(1.270)
TYP
0.008
(0.203)
TYP
0.004 – 0.010
(0.102 – 0.254)
SEATING PLANE
0.014 – 0.020 TYP
(0.356 – 0.508)
M16A (REV H)

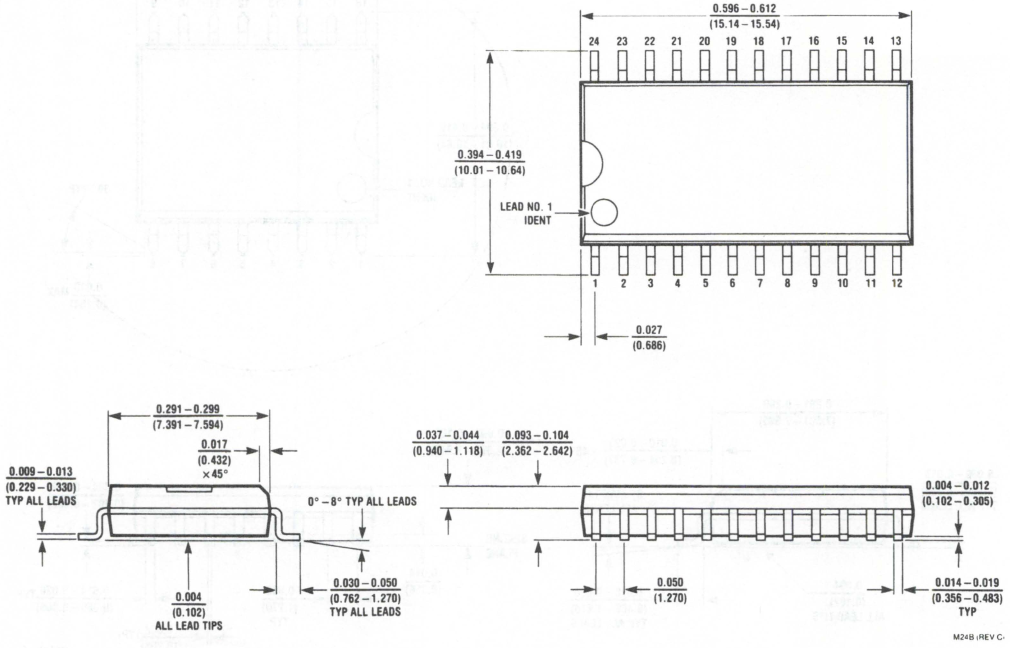
16 Lead (0.300″ Wide) Molded Small Outline Package (M)
NS Package Number M16B


0.398 – 0.413
(10.11 – 10.50)
16 15 14 13 12 11 10 9
0.394 – 0.419
(10.01 – 10.64)
LEAD NO. 1 IDENT
30° TYP
1 2 3 4 5 6 7 8
0.010 MAX
(0.254)
0.291 – 0.299
(7.391 – 7.595)
0.010 – 0.029
(0.254 – 0.737)
×45°
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
8° MAX TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
SEATING PLANE
0.014
(0.356)
0.050
(1.270)
TYP
0.008 TYP
(0.203)
0.004 – 0.012
(0.102 – 0.305)
0.014 – 0.020 TYP
(0.356 – 0.508)
M16B (REV E)

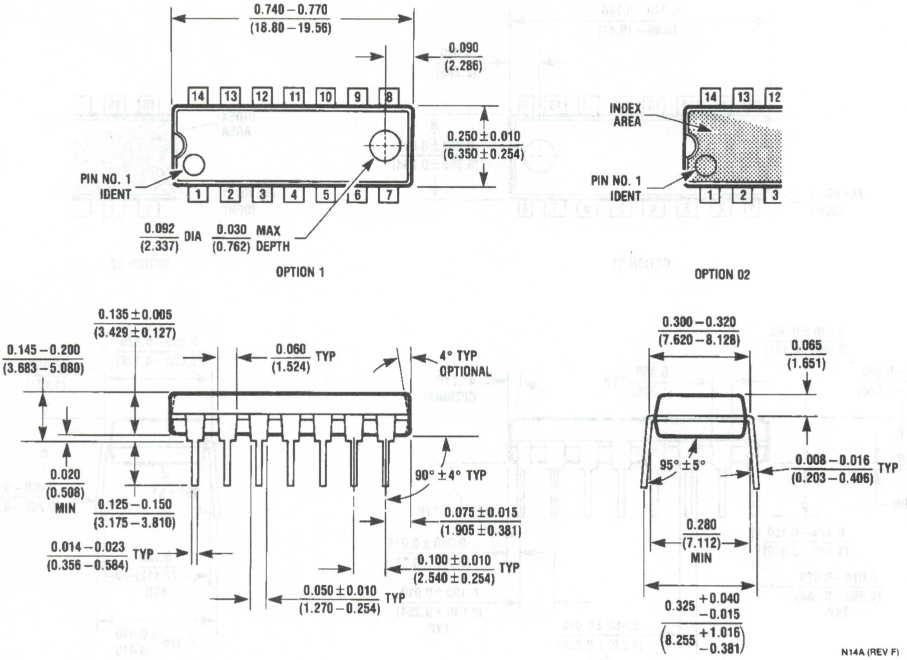
20 Lead (0.300″ Wide) Molded Small Outline Package (M) NS Package Number M20B


0.496 – 0.512
(12.598 – 13.005)
20 19 18 17 16 15 14 13 12 11
0.394 – 0.419
(10.008 – 10.643)
LEAD NO. 1 IDENT
30° TYP
1 2 3 4 5 6 7 8 9 10
0.010 MAX
(0.254)
0.291 – 0.299
(7.391 – 7.595)
0.010 – 0.029
(0.254 – 0.737) × 45°
8° MAX TYP ALL LEADS
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
SEATING PLANE
0.014
(0.356)
0.050
(1.270)
TYP
0.014 – 0.020 TYP
(0.356 – 0.508)
0.008 TYP
(0.203)
M20B (REV F)

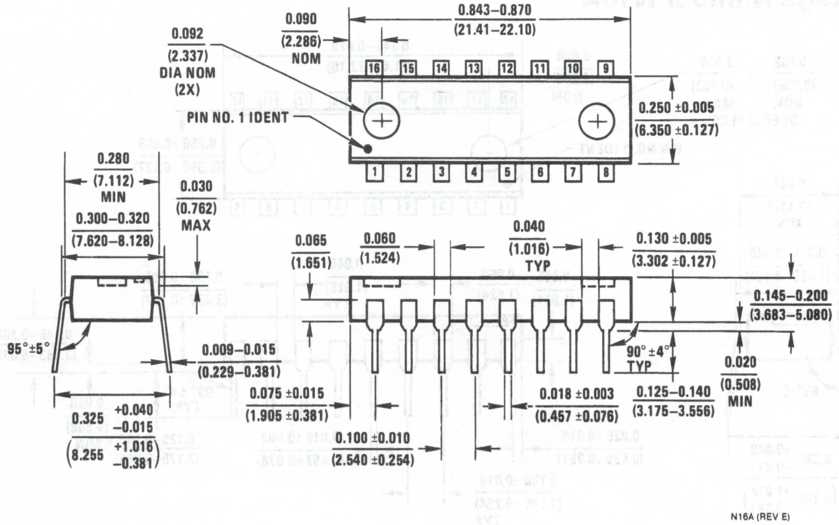
24 Lead (0.300″ Wide) Molded Small Outline Package (M) NS Package Number M24B


0.596 – 0.612
(15.14 – 15.54)
24 23 22 21 20 19 18 17 16 15 14 13
0.394 – 0.419
(10.01 – 10.64)
LEAD NO. 1 IDENT
1 2 3 4 5 6 7 8 9 10 11 12
0.027
(0.686)
0.291 – 0.299
(7.391 – 7.594)
0.017
(0.432)
× 45°
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
0° – 8° TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.030 – 0.050
(0.762 – 1.270)
TYP ALL LEADS
0.037 – 0.044
(0.940 – 1.118)
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
0.050
(1.270)
0.014 – 0.019
(0.356 – 0.483)
TYP
M24B (REV C)

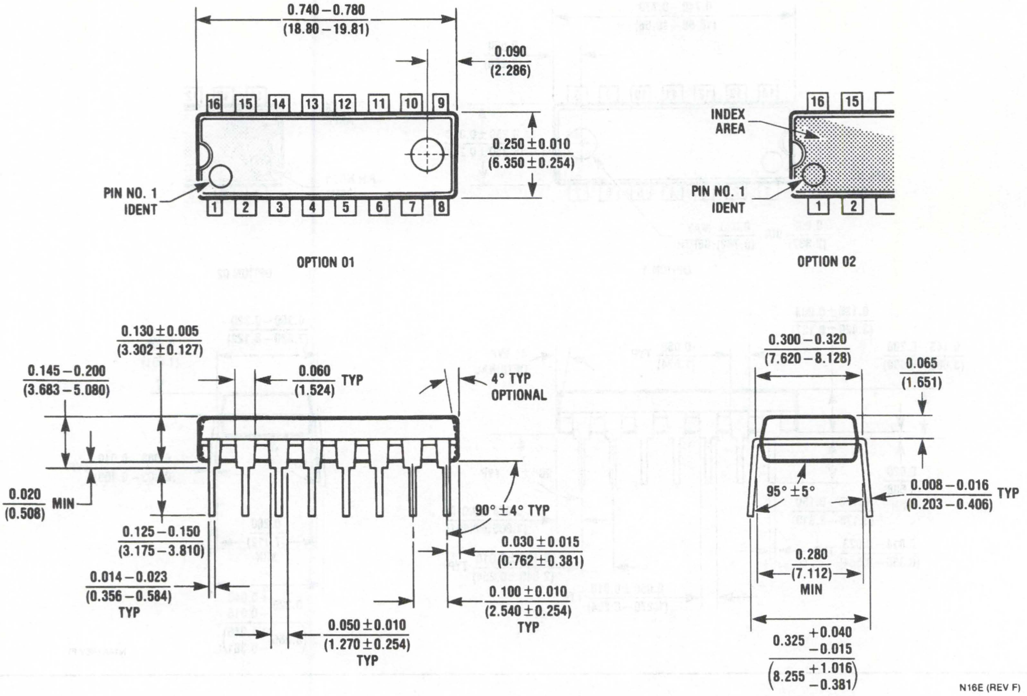
14 Lead Molded Dual-In-Line Package (N)
NS Package Number N14A


0.740 – 0.770
(18.80 – 19.56)
0.090
(2.286)
14 13 12 11 10 9 8
1 2 3 4 5 6 7
0.250 ± 0.010
(6.350 ± 0.254)
PIN NO. 1 IDENT
0.092 (2.337) DIA
0.030 (0.762) MAX DEPTH
OPTION 1
INDEX AREA
PIN NO. 1 IDENT
OPTION 02
0.135 ± 0.005
(3.429 ± 0.127)
0.145 – 0.200
(3.683 – 5.080)
0.060 (1.524) TYP
4° TYP OPTIONAL
0.020 (0.508) MIN
0.125 – 0.150
(3.175 – 3.810)
90° ± 4° TYP
0.075 ± 0.015
(1.905 ± 0.381)
0.014 – 0.023 (0.356 – 0.584) TYP
0.100 ± 0.010 (2.540 ± 0.254) TYP
0.050 ± 0.010 (1.270 – 0.254) TYP
0.300 – 0.320
(7.620 – 8.128)
0.065
(1.651)
95° ± 5°
0.008 – 0.016 (0.203 – 0.406) TYP
0.280 (7.112) MIN
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
N14A (REV F)

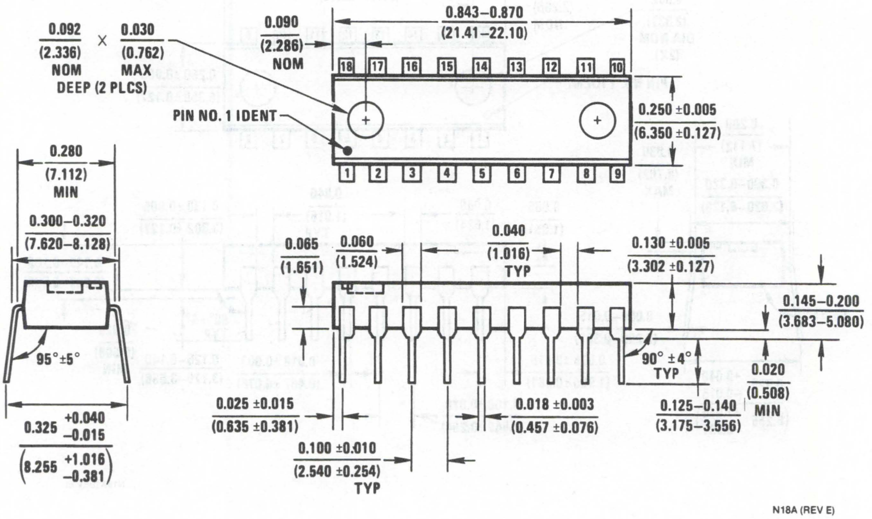
16 Lead Molded Dual-In-Line Package (N)
NS Package Number N16A


0.843–0.870
(21.41–22.10)
0.090 (2.286) NOM
0.092 (2.337) DIA NOM (2X)
PIN NO. 1 IDENT
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
0.250 ±0.005
(6.350 ±0.127)
0.280 (7.112) MIN
0.030 (0.762) MAX
0.300–0.320
(7.620–8.128)
95°±5°
0.009–0.015
(0.229–0.381)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.065 (1.651)
0.060 (1.524)
0.040 (1.016) TYP
0.130 ±0.005
(3.302 ±0.127)
0.145–0.200
(3.683–5.080)
90° ±4° TYP
0.020 (0.508) MIN
0.075 ±0.015
(1.905 ±0.381)
0.018 ±0.003
(0.457 ±0.076)
0.125–0.140
(3.175–3.556)
0.100 ±0.010
(2.540 ±0.254)
N16A (REV E)

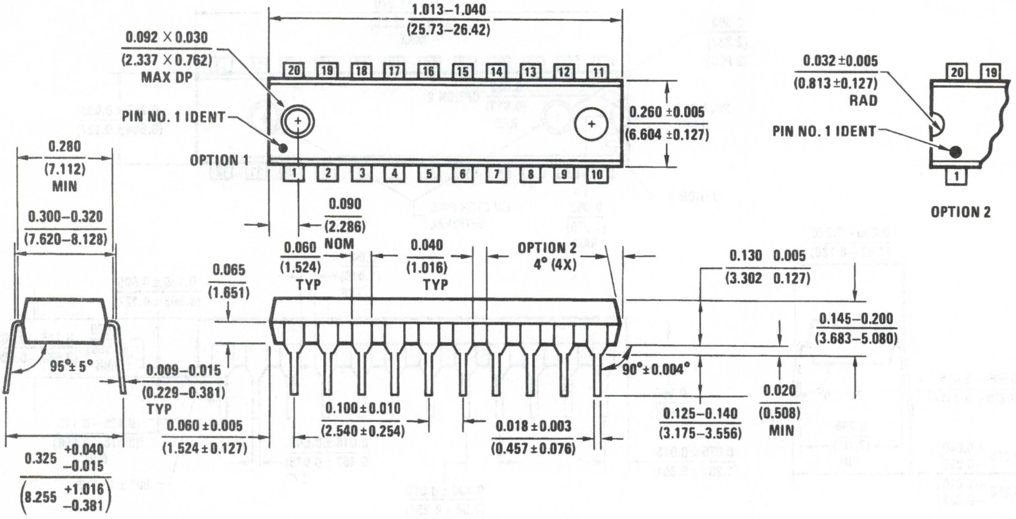
16 Lead Molded Dual-In-Line Package (N)
NS Package Number N16E


0.740 – 0.780
(18.80 – 19.81)
0.090
(2.286)
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
0.250 ± 0.010
(6.350 ± 0.254)
PIN NO. 1 IDENT
OPTION 01
INDEX AREA
PIN NO. 1 IDENT
OPTION 02
0.130 ± 0.005
(3.302 ± 0.127)
0.145 – 0.200
(3.683 – 5.080)
0.060
(1.524)
TYP
4° TYP
OPTIONAL
0.020
(0.508)
MIN
0.125 – 0.150
(3.175 – 3.810)
0.014 – 0.023
(0.356 – 0.584)
TYP
90° ± 4° TYP
0.030 ± 0.015
(0.762 ± 0.381)
0.100 ± 0.010
(2.540 ± 0.254)
TYP
0.050 ± 0.010
(1.270 ± 0.254)
TYP
0.300 – 0.320
(7.620 – 8.128)
0.065
(1.651)
95° ± 5°
0.008 – 0.016
(0.203 – 0.406)
TYP
0.280
(7.112)
MIN
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
N16E (REV F)

18 Lead Molded Dual-In-Line Package (N)
NS Package Number N18A

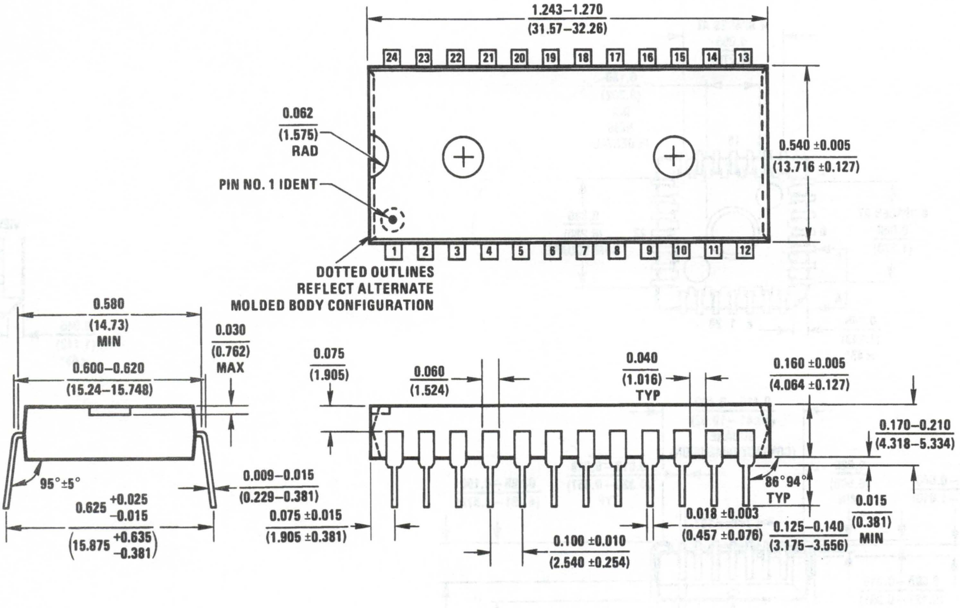

0.092
(2.336)
NOM
X
0.030
(0.762)
MAX
DEEP (2 PLCS)
0.090
(2.286)
NOM
0.843–0.870
(21.41–22.10)
18
17
16
15
14
13
12
11
10
1
2
3
4
5
6
7
8
9
PIN NO. 1 IDENT
0.250 ±0.005
(6.350 ±0.127)
0.280
(7.112)
MIN
0.300–0.320
(7.620–8.128)
95°±5°
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.065
(1.651)
0.060
(1.524)
0.040
(1.016)
TYP
0.130 ±0.005
(3.302 ±0.127)
0.145–0.200
(3.683–5.080)
90° ±4°
TYP
0.020
(0.508)
MIN
0.125–0.140
(3.175–3.556)
0.025 ±0.015
(0.635 ±0.381)
0.018 ±0.003
(0.457 ±0.076)
0.100 ±0.010
(2.540 ±0.254)
TYP
N18A (REV E)

20 Lead Molded Dual-In-Line Package (N)
NS Package Number N20A


1.013–1.040
(25.73–26.42)
0.092 × 0.030
(2.337 × 0.762)
MAX DP
PIN NO. 1 IDENT
OPTION 1
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10
0.260 ±0.005
(6.604 ±0.127)
0.032 ±0.005
(0.813 ±0.127)
RAD
PIN NO. 1 IDENT
OPTION 2
0.280
(7.112)
MIN
0.300–0.320
(7.620–8.128)
0.090
(2.286)
NOM
0.060
(1.524)
TYP
0.040
(1.016)
TYP
OPTION 2
4° (4X)
0.065
(1.651)
0.130 0.005
(3.302 0.127)
0.145–0.200
(3.683–5.080)
95° ± 5°
0.009–0.015
(0.229–0.381)
TYP
90° ± 0.004°
0.020
(0.508)
MIN
0.100 ± 0.010
(2.540 ± 0.254)
0.125–0.140
(3.175–3.556)
0.060 ± 0.005
(1.524 ± 0.127)
0.018 ± 0.003
(0.457 ± 0.076)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)

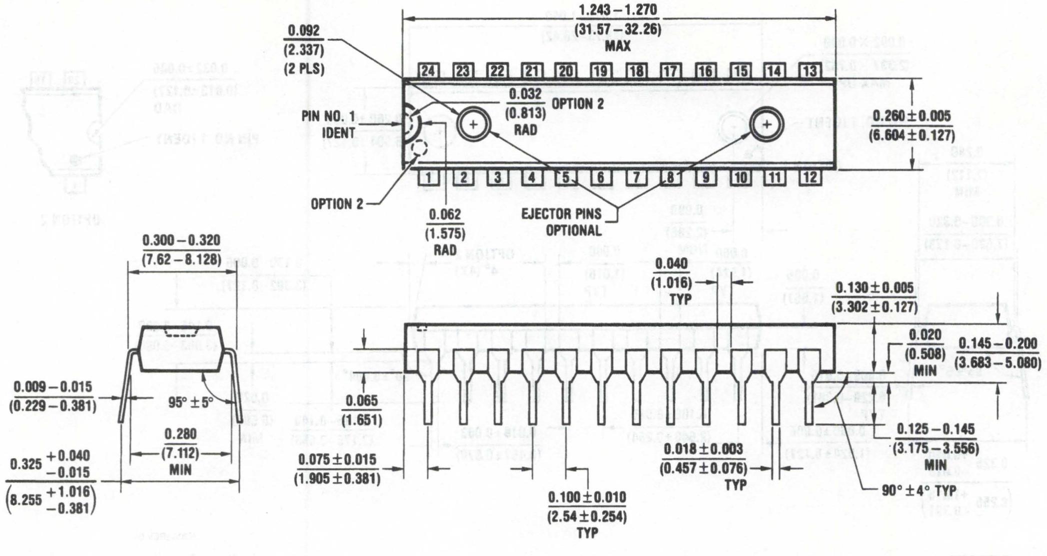
N20A (REV G)

24 Lead Molded Dual-In-Line Package (N)
NS Package Number N24A

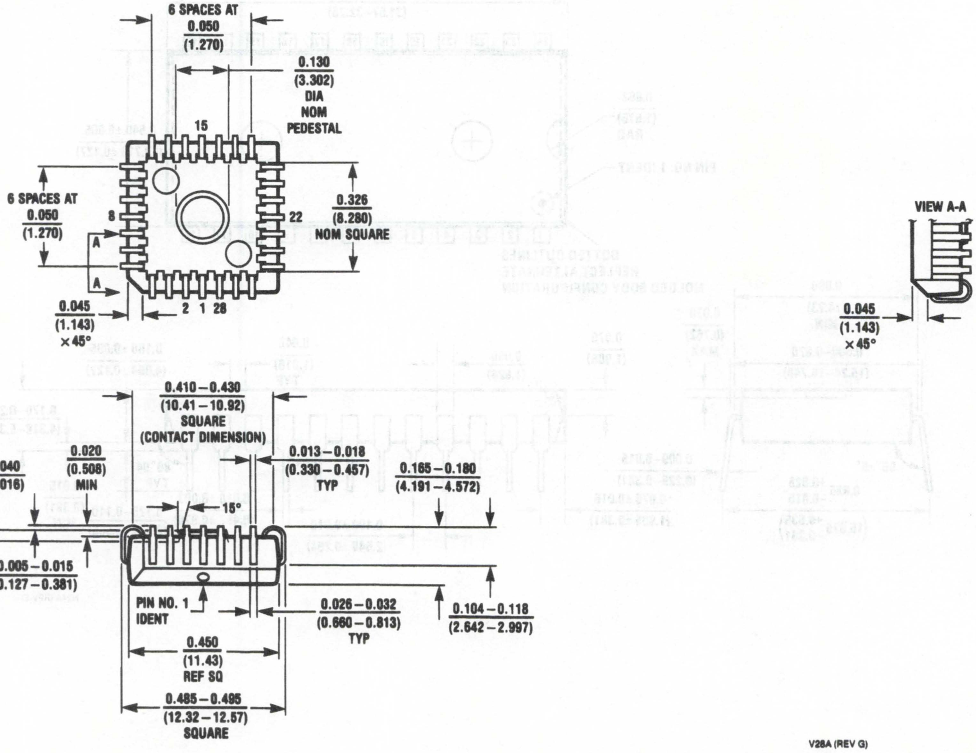

1.243–1.270
(31.57–32.26)
24 23 22 21 20 19 18 17 16 15 14 13
1 2 3 4 5 6 7 8 9 10 11 12
0.062
(1.575)
RAD
PIN NO. 1 IDENT
0.540 ±0.005
(13.716 ±0.127)
DOTTED OUTLINES
REFLECT ALTERNATE
MOLDED BODY CONFIGURATION
0.580
(14.73)
MIN
0.600–0.620
(15.24–15.748)
0.030
(0.762)
MAX
0.075
(1.905)
0.060
(1.524)
0.040
(1.016)
TYP
0.160 ±0.005
(4.064 ±0.127)
0.170–0.210
(4.318–5.334)
95° ±5°
0.009–0.015
(0.229–0.381)
86°94°
TYP
0.625 +0.025 −0.015
(15.875 +0.635 −0.381)
0.075 ±0.015
(1.905 ±0.381)
0.018 ±0.003
(0.457 ±0.076)
0.125–0.140
(3.175–3.556)
0.015
(0.381)
MIN
0.100 ±0.010
(2.540 ±0.254)

N24A (REV E)

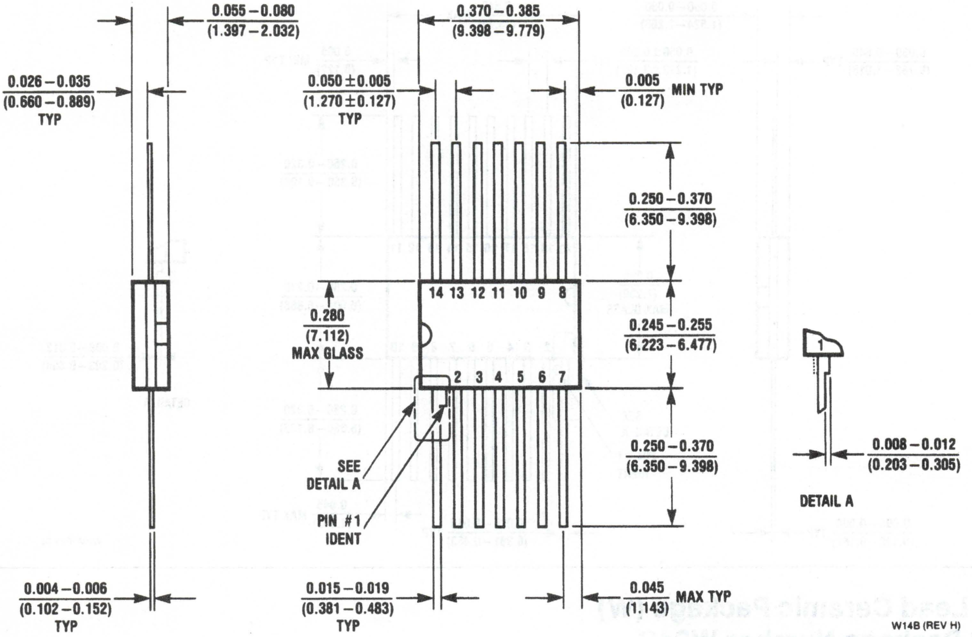
24 Lead (0.300" Wide) Dual-In-Line Package (N)
NS Package Number N24C


1.243 – 1.270
(31.57 – 32.26)
MAX
0.092
(2.337)
(2 PLS)
24 23 22 21 20 19 18 17 16 15 14 13
0.032
(0.813)
RAD
OPTION 2
PIN NO. 1
IDENT
0.260 ± 0.005
(6.604 ± 0.127)
1 2 3 4 5 6 7 8 9 10 11 12
OPTION 2
0.062
(1.575)
RAD
EJECTOR PINS
OPTIONAL
0.300 – 0.320
(7.62 – 8.128)
0.040
(1.016)
TYP
0.130 ± 0.005
(3.302 ± 0.127)
0.020
(0.508)
MIN
0.145 – 0.200
(3.683 – 5.080)
0.009 – 0.015
(0.229 – 0.381)
95° ± 5°
0.065
(1.651)
0.280
(7.112)
MIN
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.075 ± 0.015
(1.905 ± 0.381)
0.018 ± 0.003
(0.457 ± 0.076)
TYP
0.125 – 0.145
(3.175 – 3.556)
MIN
90° ± 4° TYP
0.100 ± 0.010
(2.54 ± 0.254)
TYP
N24C (REV F)

28 Lead Plastic Chip Carrier (V)
NS Package Number V28A

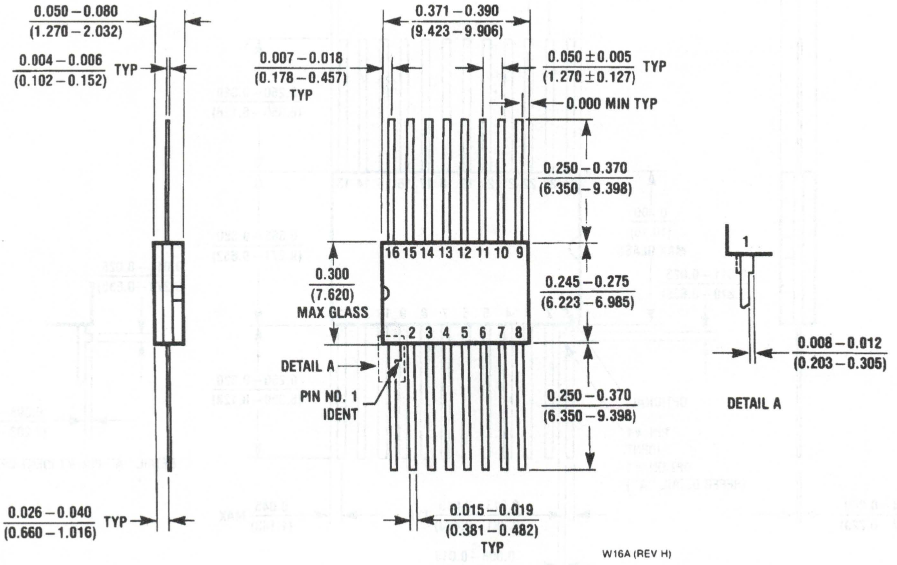

6 SPACES AT
0.050
(1.270)
0.130
(3.302)
DIA
NOM
PEDESTAL
15
6 SPACES AT
0.050
(1.270)
8
22
A
A
0.326
(8.280)
NOM SQUARE
VIEW A-A
0.045
(1.143)
× 45°
2 1 28
0.045
(1.143)
× 45°
0.410 – 0.430
(10.41 – 10.92)
SQUARE
(CONTACT DIMENSION)
0.032 – 0.040
(0.813 – 1.016)
0.020
(0.508)
MIN
0.013 – 0.018
(0.330 – 0.457)
TYP
0.165 – 0.180
(4.191 – 4.572)
15°
0.005 – 0.015
(0.127 – 0.381)
PIN NO. 1
IDENT
0.026 – 0.032
(0.660 – 0.813)
TYP
0.104 – 0.118
(2.642 – 2.997)
0.450
(11.43)
REF SQ
0.485 – 0.495
(12.32 – 12.57)
SQUARE
V28A (REV G)

14 Lead Ceramic Package (W)
NS Package Number W14B


0.055 – 0.080
(1.397 – 2.032)
0.026 – 0.035
(0.660 – 0.889)
TYP
0.370 – 0.385
(9.398 – 9.779)
0.050 ± 0.005
(1.270 ± 0.127)
TYP
0.005
(0.127)
MIN TYP
0.250 – 0.370
(6.350 – 9.398)
14 13 12 11 10 9 8
0.280
(7.112)
MAX GLASS
0.245 – 0.255
(6.223 – 6.477)
1 2 3 4 5 6 7
SEE
DETAIL A
PIN #1
IDENT
0.250 – 0.370
(6.350 – 9.398)
1
0.008 – 0.012
(0.203 – 0.305)
DETAIL A
0.004 – 0.006
(0.102 – 0.152)
TYP
0.015 – 0.019
(0.381 – 0.483)
TYP
0.045
(1.143)
MAX TYP

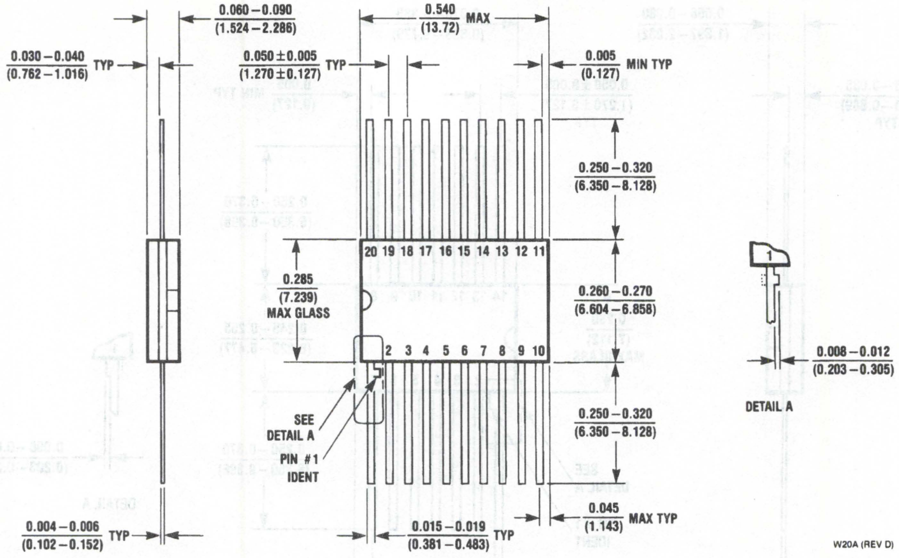
W14B (REV H)

16 Lead Ceramic Package (W)
NS Package Number W16A


0.050 – 0.080
(1.270 – 2.032)
0.004 – 0.006
(0.102 – 0.152)
TYP
0.371 – 0.390
(9.423 – 9.906)
0.007 – 0.018
(0.178 – 0.457)
TYP
0.050 ± 0.005
(1.270 ± 0.127)
TYP
0.000 MIN TYP
0.250 – 0.370
(6.350 – 9.398)
16 15 14 13 12 11 10 9
0.300
(7.620)
MAX GLASS
0.245 – 0.275
(6.223 – 6.985)
1 2 3 4 5 6 7 8
DETAIL A
PIN NO. 1
IDENT
0.250 – 0.370
(6.350 – 9.398)
1
0.008 – 0.012
(0.203 – 0.305)
DETAIL A
0.026 – 0.040
(0.660 – 1.016)
TYP
0.015 – 0.019
(0.381 – 0.482)
TYP

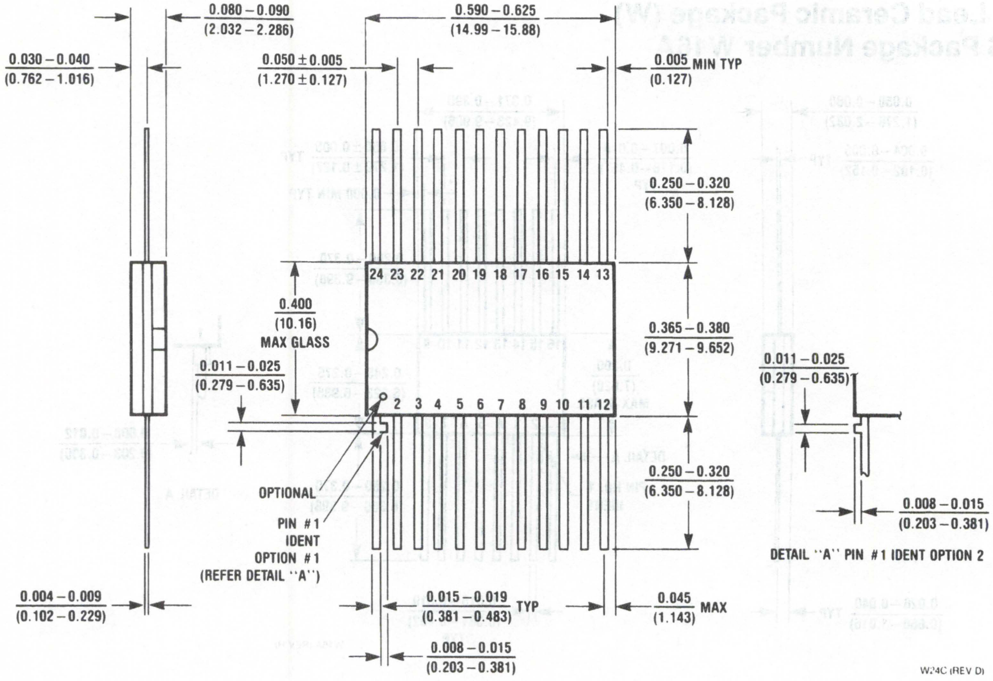
W16A (REV H)

20 Lead Ceramic Package (W)
NS Package Number W20A


0.060 – 0.090
(1.524 – 2.286)
0.540
(13.72)
MAX
0.030 – 0.040
(0.762 – 1.016)
TYP
0.050 ± 0.005
(1.270 ± 0.127)
TYP
0.005
(0.127)
MIN TYP
0.250 – 0.320
(6.350 – 8.128)
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10
0.285
(7.239)
MAX GLASS
0.260 – 0.270
(6.604 – 6.858)
0.250 – 0.320
(6.350 – 8.128)
SEE
DETAIL A
PIN #1
IDENT
0.045
(1.143)
MAX TYP
0.004 – 0.006
(0.102 – 0.152)
TYP
0.015 – 0.019
(0.381 – 0.483)
TYP
1
0.008 – 0.012
(0.203 – 0.305)
DETAIL A

W20A (REV D)

24 Lead Ceramic Package (W)
NS Package Number W24C


0.080 – 0.090
(2.032 – 2.286)
0.590 – 0.625
(14.99 – 15.88)
0.030 – 0.040
(0.762 – 1.016)
0.050 ± 0.005
(1.270 ± 0.127)
0.005
(0.127)
MIN TYP
0.250 – 0.320
(6.350 – 8.128)
24 23 22 21 20 19 18 17 16 15 14 13
2 3 4 5 6 7 8 9 10 11 12
0.400
(10.16)
MAX GLASS
0.365 – 0.380
(9.271 – 9.652)
0.011 – 0.025
(0.279 – 0.635)
0.250 – 0.320
(6.350 – 8.128)
OPTIONAL
PIN #1
IDENT
OPTION #1
(REFER DETAIL "A")
0.004 – 0.009
(0.102 – 0.229)
0.015 – 0.019
(0.381 – 0.483)
TYP
0.045
(1.143)
MAX
0.008 – 0.015
(0.203 – 0.381)
0.011 – 0.025
(0.279 – 0.635)
0.008 – 0.015
(0.203 – 0.381)

DETAIL "A" PIN #1 IDENT OPTION 2

W24C (REV D)

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